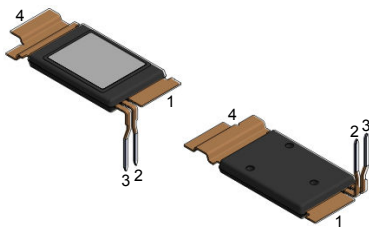
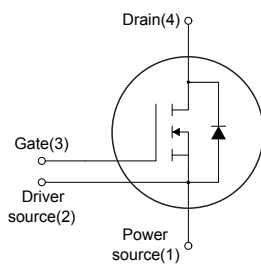


## Automotive-grade silicon carbide Power MOSFET 650 V, 8.0 mΩ typ., 250 A in a STPAK package


**STPAK**



NG3DS2PS1D4


**Product status link**
[SCTHS250N65G2G](#)
**Product summary**

<b>Order code</b>	SCTHS250N65G2G
<b>Marking</b>	SCHS250N65G2
<b>Package</b>	STPAK
<b>Packing</b>	Tray

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ typ.	$I_D$
SCTHS250N65G2G	650 V	8.0 mΩ	250 A

- AEC-Q101 qualified 
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitance
- Source sensing pin for increased efficiency

### Applications

- Main inverter (electric traction)
- DC/DC converter for EV/HEV

### Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2<sup>nd</sup> generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>GS</sub>	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating values)	-5 to 20	
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	250	A
	Drain current (continuous) at T <sub>C</sub> = 100 °C	178	
I <sub>D</sub> <sup>(1)</sup>	Drain current (pulsed)	750	A
P <sub>TOT</sub>	Total power dissipation at T <sub>C</sub> = 25 °C	790	W
V <sub>ISO</sub>	Insulation withstand voltage (DC) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)	4.3	kV
T <sub>J</sub>	Operating junction temperature range	-55 to 175	°C
T <sub>stg</sub>	Storage temperature range		°C

1. Pulse width limited by safe operating area.

**Table 2. Thermal data**

Symbol	Parameter	Min.	Typ.	Max.	Unit
R <sub>thJC</sub>	Thermal resistance, junction-to-case	-	0.14	0.19	°C/W

## 2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified.

**Table 3. On-/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}$			40	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 22\text{ V}$			100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			20	nA
		$V_{DS} = 0\text{ V}, V_{GS} = -5\text{ V}$	-20			nA
		$V_{DS} = 0\text{ V}, V_{GS} = -10\text{ V}$	-100			nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 2.5\text{ mA}$	1.5	2.9	4.0	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 20\text{ V}, I_D = 95\text{ A}$	5.8	8.0	10.9	m $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}, f = 1\text{ MHz}$	4900	7000	9100	pF
$C_{oss}$	Output capacitance		490	700	910	pF
$C_{rss}$	Reverse transfer capacitance		119	170	221	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	0.3	0.8	1.3	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}, I_D = 95\text{ A}, V_{GS} = 0\text{ to }20\text{ V}$		400		nC
$Q_{gs}$	Gate-source charge			80		nC
$Q_{gd}$	Gate-drain charge			170		nC

**Table 5. Switching energy (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}$	Turn-on switching energy	$V_{DD} = 400\text{ V}, I_D = 95\text{ A},$	-	1100	-	$\mu\text{J}$
$E_{off}$	Turn-off switching energy	$R_{G(on)} = 12\text{ }\Omega, R_{G(off)} = 10\text{ }\Omega,$ $V_{GS} = -5\text{ to }20\text{ V}, L_s = 100\text{ nH}$	-	2500	-	$\mu\text{J}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}, I_D = 95\text{ A},$ $R_G = 10\text{ }\Omega, V_{GS} = -5\text{ to }20\text{ V}$	-	140	-	ns
$t_r$	Rise time		-	350	-	ns
$t_{d(off)}$	Turn-off delay time		-	230	-	ns
$t_f$	Fall time		-	130	-	ns

**Table 7. Reverse SiC diode characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}$	Diode forward voltage	$I_{SD} = 200\text{ A}$ , $V_{GS} = -5\text{ V}$	3.0	5.7	7.0	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 95\text{ A}$ , $di/dt = 3100\text{ A}/\mu\text{s}$ , $V_{DD} = 400\text{ V}$		40		ns
$Q_{rr}$	Reverse recovery charge			1160		nC
$I_{RRM}$	Reverse recovery current			49		A

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

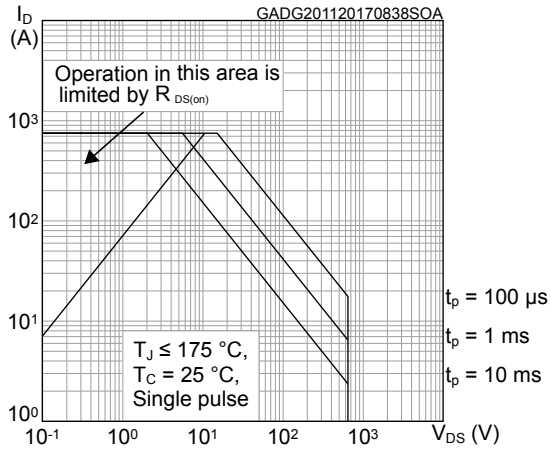


Figure 2. Normalized thermal impedance

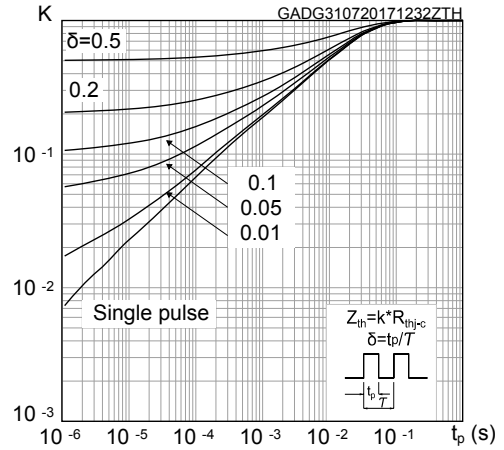


Figure 3. Output characteristics ( $T_J = 25\text{ °C}$ )

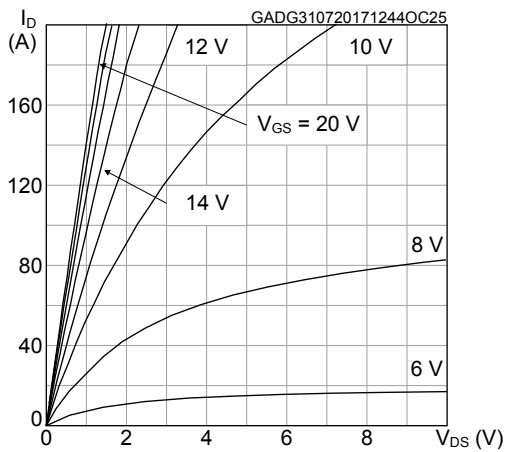


Figure 4. Output characteristics ( $T_J = 175\text{ °C}$ )

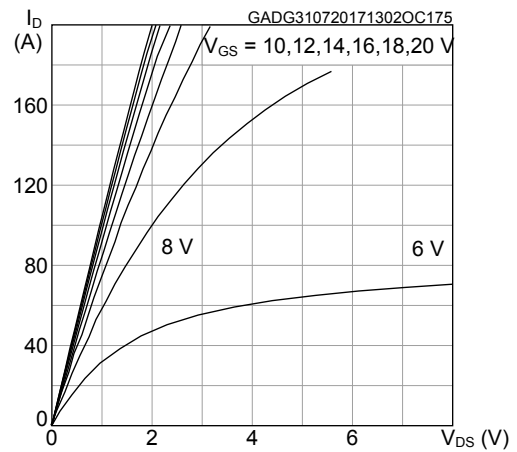


Figure 5. Transfer characteristics

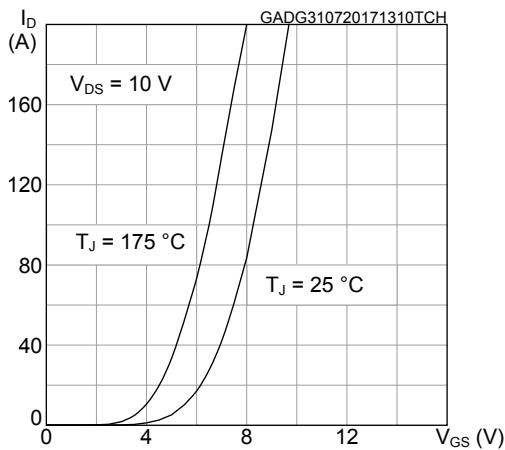
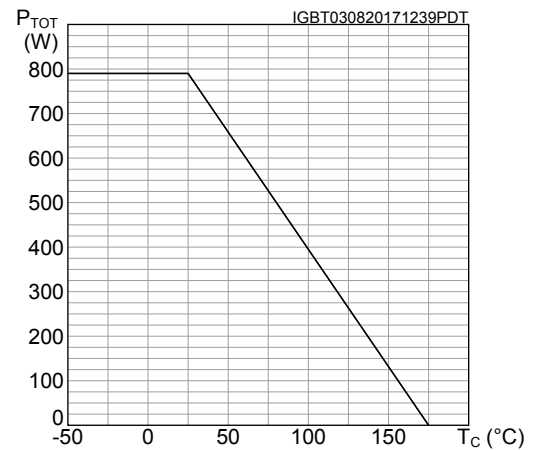
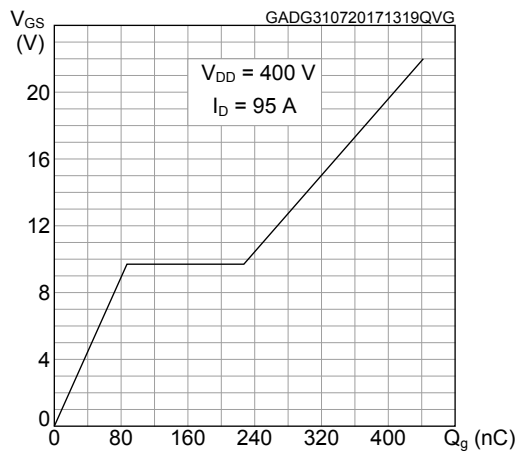


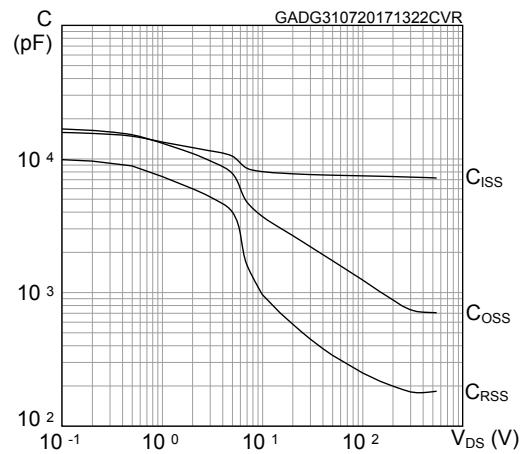
Figure 6. Power dissipation



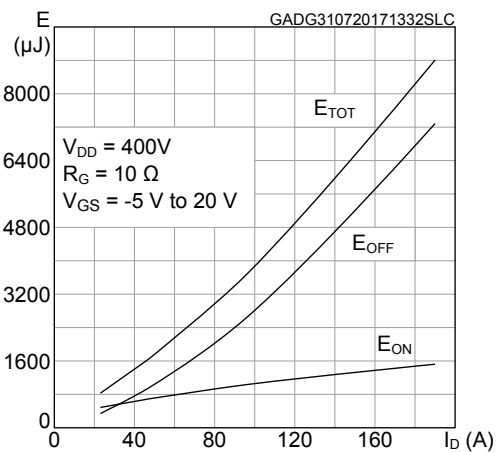
**Figure 7. Gate charge vs gate-source voltage**



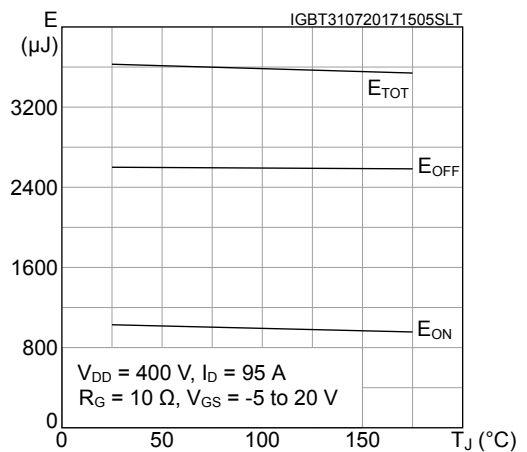
**Figure 8. Capacitance variations**



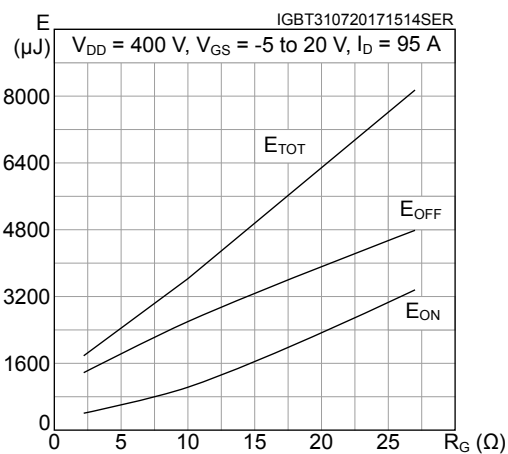
**Figure 9. Switching energy vs drain current**



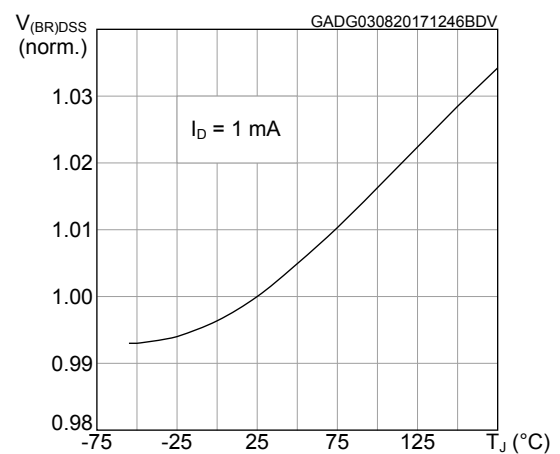
**Figure 10. Switching energy vs junction temperature**



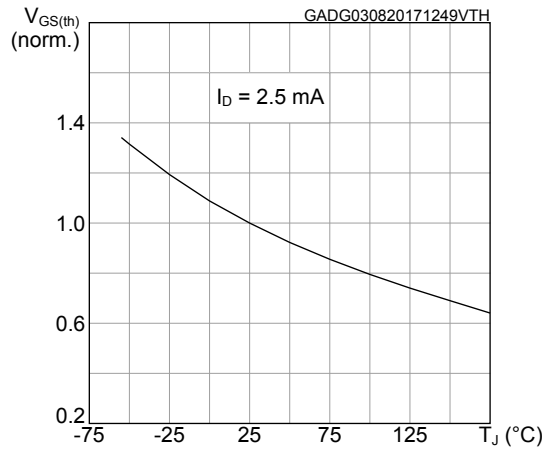
**Figure 11. Switching energy vs Rg**



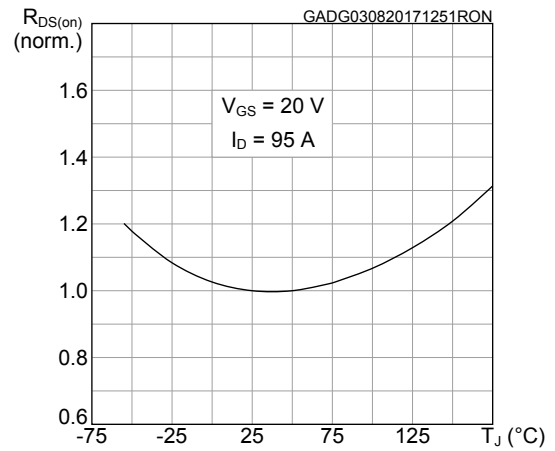
**Figure 12. Normalized V(BR)DSS vs temperature**



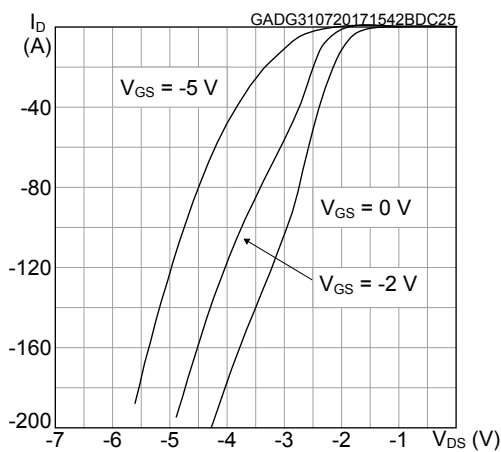
**Figure 13. Normalized gate threshold voltage vs temperature**



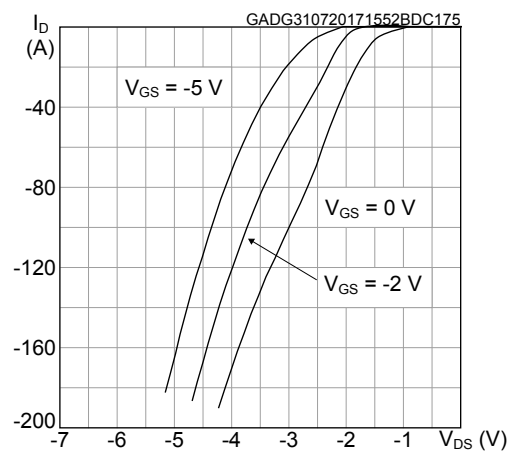
**Figure 14. Normalized on-resistance vs temperature**



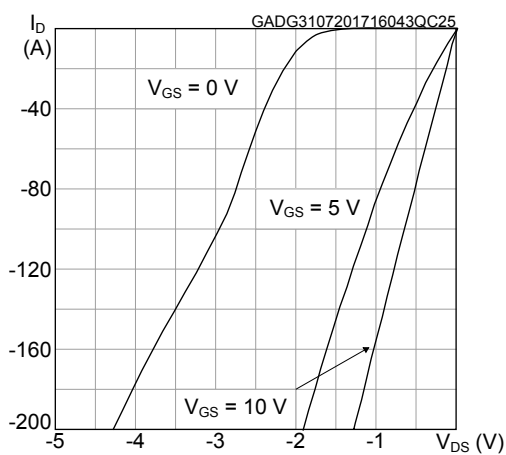
**Figure 15. Body diode characteristics (T<sub>J</sub> = 25 °C)**



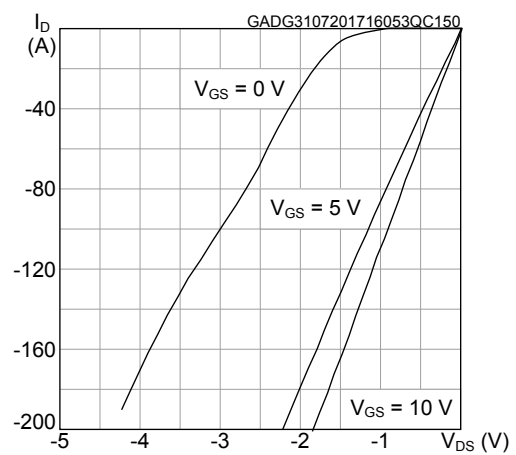
**Figure 16. Body diode characteristics (T<sub>J</sub> = 175 °C)**



**Figure 17. 3<sup>rd</sup> quadrant characteristics (T<sub>J</sub> = 25 °C)**



**Figure 18. 3<sup>rd</sup> quadrant characteristics (T<sub>J</sub> = 175 °C)**

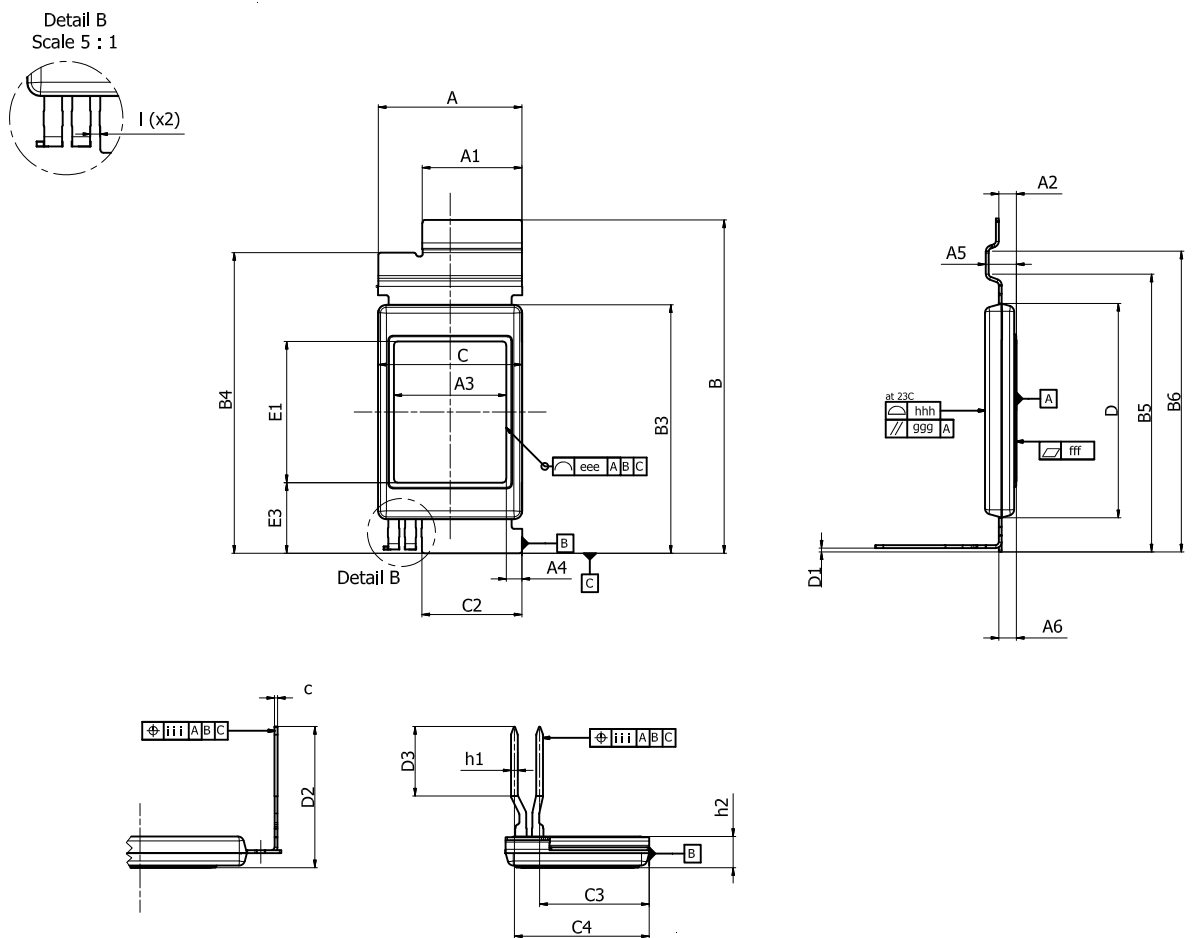


### 3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

#### 3.1 STPAK package information

Figure 19. STPAK package outline



DM00305987\_7



**Table 8. STPAK package mechanical data**

Ref.	Dimensions			Notes
	mm			
	Min.	Typ.	Max.	
A	18.60	18.80	19.00	
A1	12.85	13.05	13.25	
A2	2.00	2.30	2.60	
A3	14.20	14.70	15.20	Exposed Pad
A4	1.55	2.05	2.55	
A5	3.80	4.00	4.20	
A6	2.10	2.30	2.50	
B	43.40	43.70	44.00	
B3	32.20	32.50	32.80	
B4	39.10	39.40	39.70	
B5	36.07	36.37	36.67	
B6	39.07	39.37	39.67	
c	0.34	0.39	0.44	
C		18.55	19.10	Encompass both large and small cav.
C2	12.90	13.10	13.30	
C3		14.35		
C4		17.65		
D	27.90	28.10	28.30	
D1		0.69		
D2	18.00 (18.50)	18.50 (19.00)	19.00 (19.50)	Refer to the values in brackets for the longer pins type
D3	8.60 (9.10)	9.10 (9.60)	9.60 (10.10)	Refer to the values in brackets for the longer pins type
E1	18.00	18.50	19.00	Exposed pad
E3	8.75	9.25	9.75	
h1	0.85	0.90	0.95	x2 - Pins width
h2	4.00	4.10	4.20	
l	0.60	0.70	0.80	
eee		0.50		
fff	0.10 at 23 °C – 0.05 at 220 °C			Convex with center higher than edges
ggg		0.05		
hhh		0.10		
iii		0.60		

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
27-Apr-2023	1	First release.

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