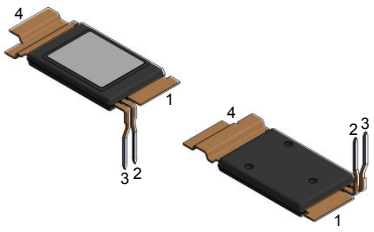
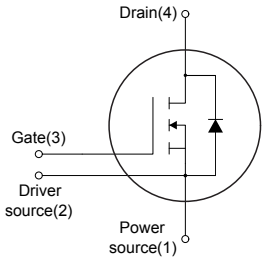
SCTHS250N65G3

Datasheet

Automotive-grade silicon carbide Power MOSFET 650 V, 6.7 mΩ typ., 237 A in a STPAK package



STPAK



NG3DS2PS1D4

Features

Order codes	V_{DS}	$R_{DS(on)}$ typ.	I_D
SCTHS250N65G3AG	650 V	6.7 mΩ	237 A
SCTHS250N65G3TAG			

- AEC-Q101 qualified
- Very low $R_{DS(on)}$ over the entire temperature range
- High speed switching performances
- Very fast and robust intrinsic body diode
- Very high operating junction temperature capability (T_J = 200 °C)
- Source sensing pin for increased efficiency

Application

- Main inverter (electric traction)

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 3rd generation SiC MOSFET technology. The device features a very low $R_{DS(on)}$ over the entire temperature range combined with low capacitances and very high switching operations, which improve application performance in frequency, energy efficiency, system size and weight reduction.

Product status link
SCTHS250N65G3

Product summary	
Order code	**SCTHS250N65G3AG**
Marking	S25N65G3PAG
Package	STPAK
Packing	Tray
Order code	**SCTHS250N65G3TAG**
Marking	S25N65G3PAG
Package	STPAK
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating values)	-5 to 18	
I_D	Drain current (continuous) at T_C = 25 °C	237	A
	Drain current (continuous) at T_C = 100 °C	179	
I_{DM}(1)	Drain current (pulsed)	717	A
P_{TOT}	Total power dissipation at T_C = 25 °C	795	W
V_{ISO}	Insulation withstand voltage applied between each pin and the heat sink plate (DC voltage, t = 1 s)	4.3	kV
T_{stg}	Storage temperature range	-55 to 200	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.22	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			40	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -10 to 22 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 2.5 mA	1.6	2.5	3.4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 18 V, I_D = 95 A		6.7	10	mΩ
		V_{GS} = 18 V, I_D = 95 A, T_J = 200 °C		9.5		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 1 MHz, V_{GS} = 0 V	-	5800	-	pF
C_{oss}	Output capacitance		-	510	-	pF
C_{rss}	Reverse transfer capacitance		-	43	-	pF
R_g	Gate input resistance	f = 1 MHz, I_D = 0 A	-	1	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, V_{GS} = 0 to 18 V, I_D = 95 A	-	208	-	nC
Q_{gs}	Gate-source charge		-	74	-	nC
Q_{gd}	Gate-drain charge		-	53	-	nC

Table 5. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	V_{DD} = 400 V, I_D = 95 A, R_G = 12 Ω, V_{GS} = -5 V to 18 V	-	1226	-	µJ
E_{off}	Turn-off switching energy		-	1368	-	µJ

Table 6. Switching times (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 95 A, R_G = 12 Ω, V_{GS} = -5 to 18 V	-	51	-	ns
t_f	Fall time		-	36	-	ns
$t_{d(off)}$	Turn-off delay time		-	133	-	ns
t_r	Rise time		-	38	-	ns

Table 7. Reverse SiC diode characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Diode forward voltage	I_{SD} = 200 A, V_{GS} = -5 V	-	5.5	7	V
t_{rr}	Reverse recovery time	I_{SD} = 95 A, di/dt = 1 kA/µs, V_{GS} = -5 V, V_{DD} = 400 V	-	33		ns
Q_{rr}	Reverse recovery charge		-	375		nC
I_{RRM}	Reverse recovery current		-	20		A

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

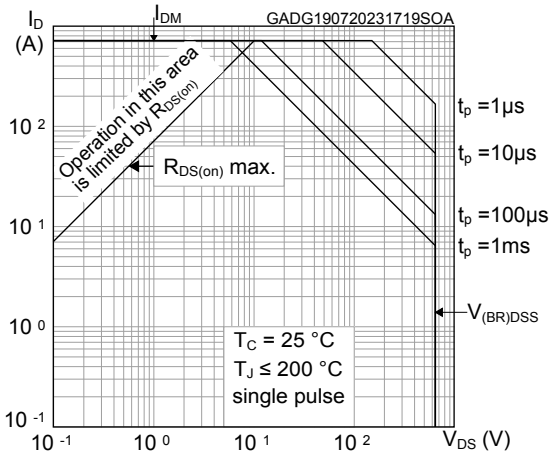


Figure 2. Maximum transient thermal impedance

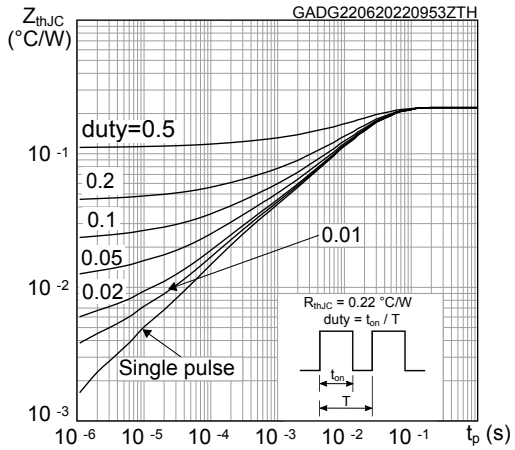


Figure 3. Typical output characteristics (T_J = 25 °C)

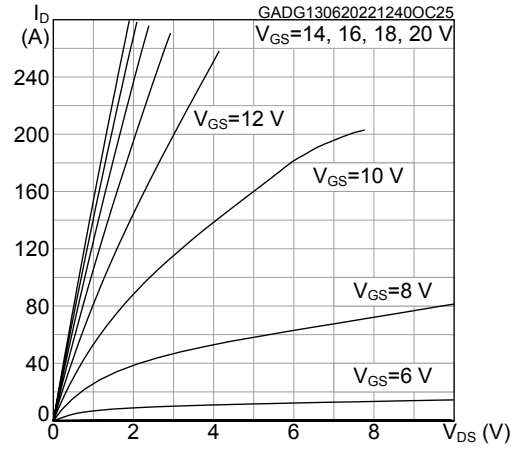


Figure 4. Typical output characteristics (T_J = 200 °C)

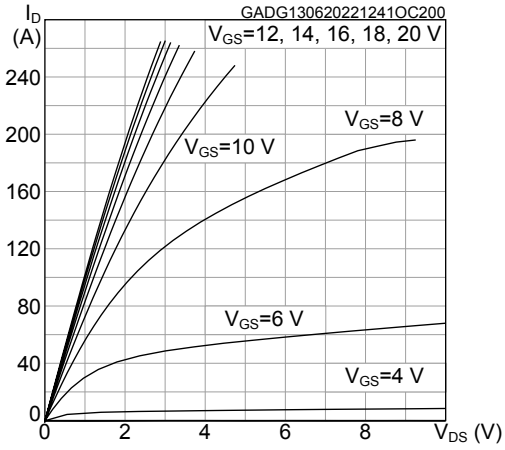


Figure 5. Typical transfer characteristics

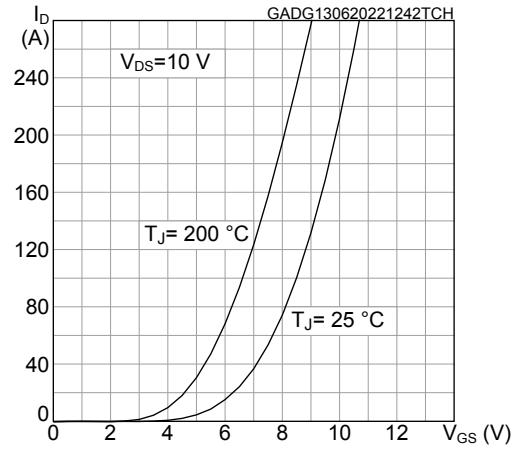


Figure 6. Total power dissipation

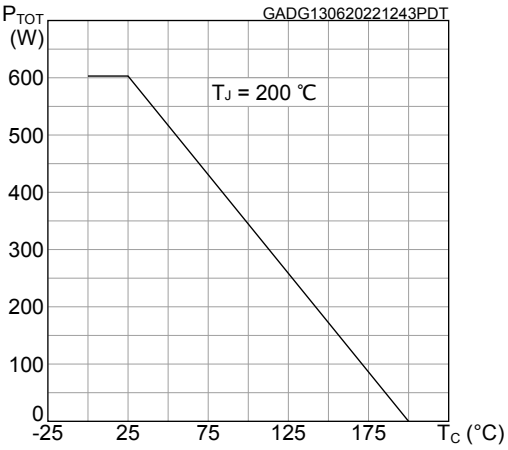


Figure 7. Typical gate charge characteristics

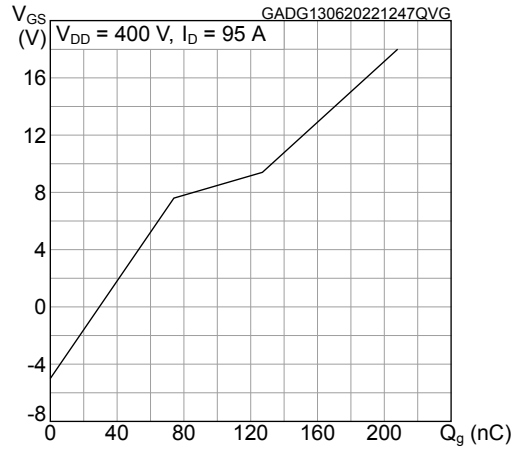


Figure 8. Typical capacitance characteristics

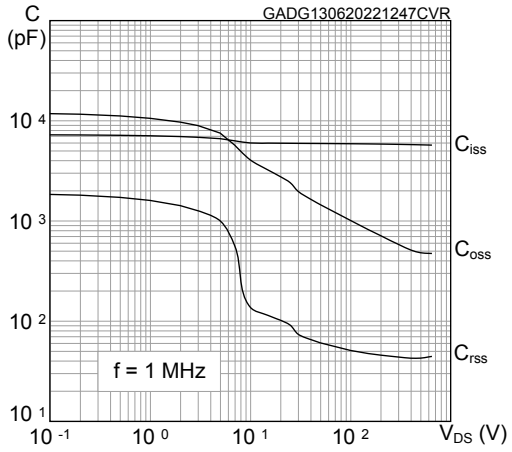


Figure 9. Typical switching energy vs drain current

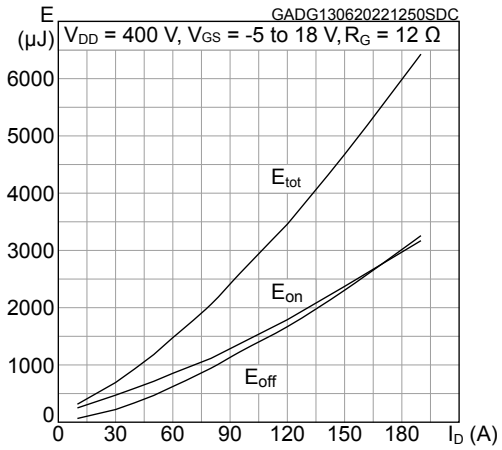


Figure 10. Typical switching energy vs temperature

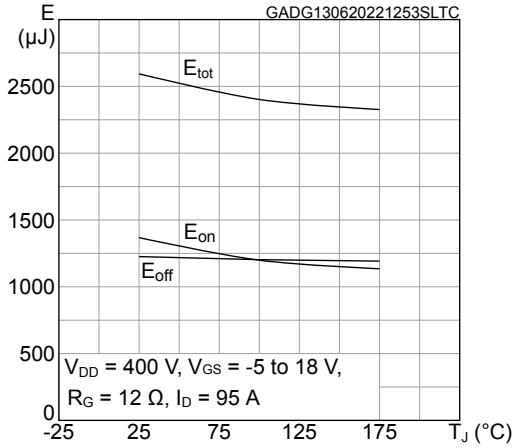


Figure 11. Normalized breakdown voltage vs temperature

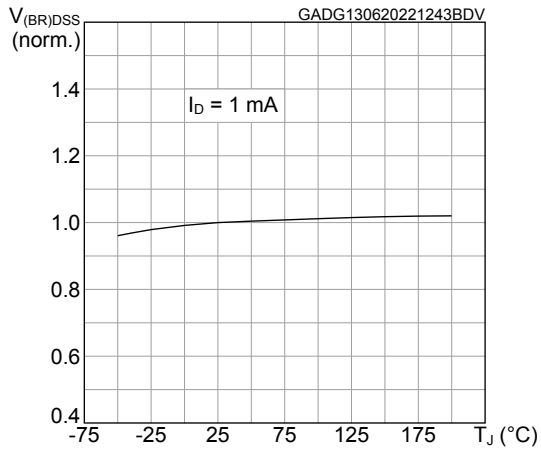


Figure 12. Normalized gate threshold vs temperature

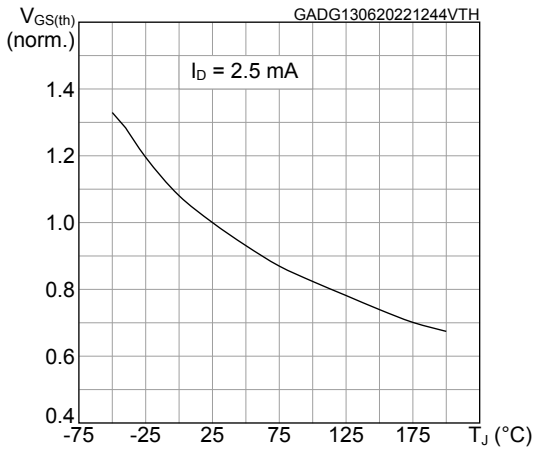


Figure 13. Normalized on-resistance vs temperature

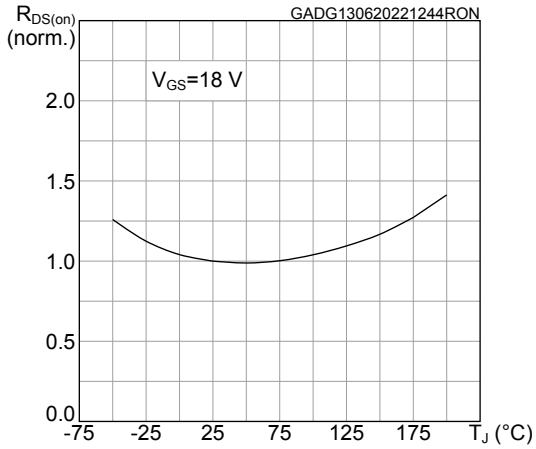


Figure 14. Typical reverse conduction characteristics (T_J = 25 °C)

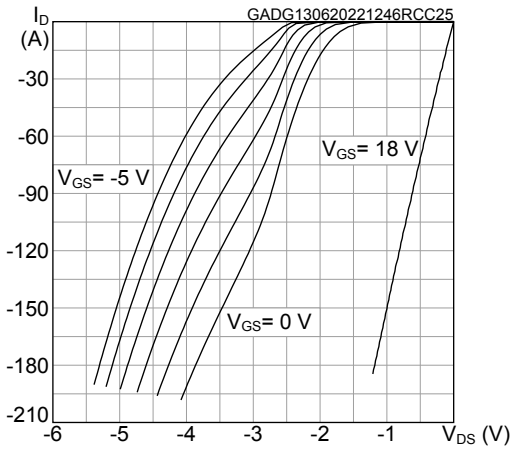
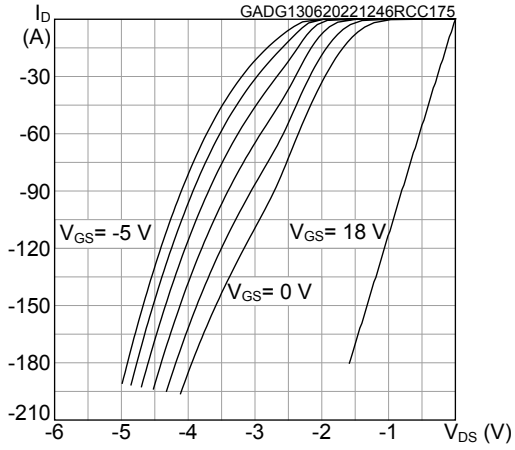


Figure 15. Typical reverse conduction characteristics (T_J = 175 °C)



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 STPAK package information

Figure 16. STPAK package outline

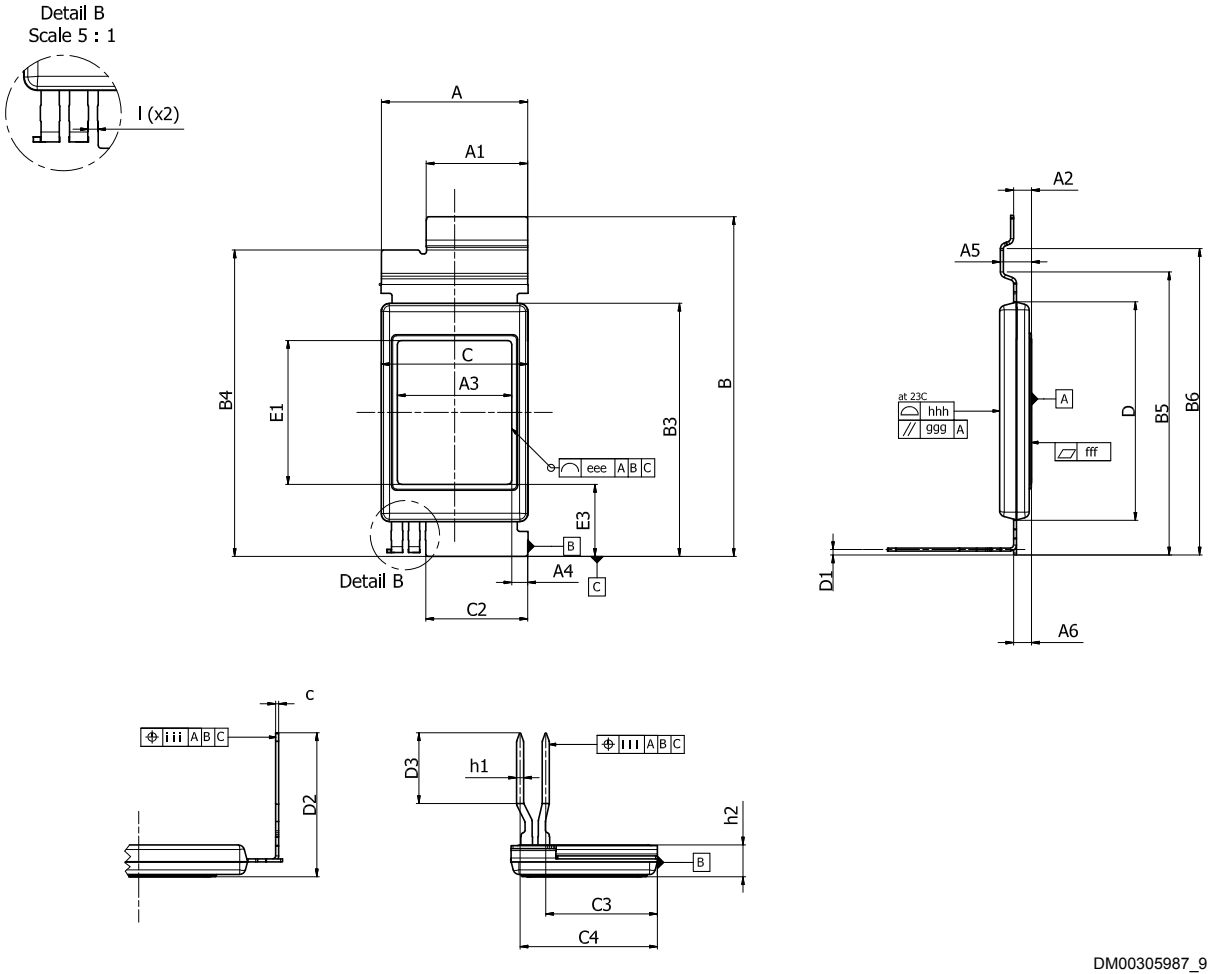


Table 8. **STPAK package mechanical data**

Ref.	Dimensions			Notes
	mm			
	Min.	Typ.	Max.	
A	18.60	18.80	19.00	
A1	12.85	13.05	13.25	
A2	2.00	2.30	2.60	
A3	13.40	13.90	14.40	Exposed Pad
A4	1.95	2.45	2.95	
A5	3.80	4.00	4.20	
A6	2.10	2.30	2.50	
B	43.40	43.70	44.00	
B3	32.20	32.50	32.80	
B4	39.10	39.40	39.70	
B5	36.07	36.37	36.67	
B6	39.07	39.37	39.67	
c	0.34	0.39	0.44	
C		18.55	19.10	Encompass both large and small cav.
C2	12.90	13.10	13.30	
C3		14.35		
C4		17.65		
D	27.90	28.10	28.30	
D1		0.69		
D2	18.00 (18.50)	18.50 (19.00)	19.00 (19.50)	Refer to the values in brackets for the longer pins type
D3	8.60 (9.10)	9.10 (9.60)	9.60 (10.10)	Refer to the values in brackets for the longer pins type
E1	17.20	17.70	18.20	Exposed pad
E3	9.15	9.65	10.15	
h1	0.85	0.90	0.95	x2 - Pins width
h2	4.00	4.10	4.20	
l	0.60	0.70	0.80	
eee	0.50			
fff	0.10 at 23 °C – 0.05 at 220 °C			Convex with center higher than edges
ggg	0.05			
hhh	0.10			
iii	0.60			

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
12-Sep-2022	1	First release.
05-Oct-2022	2	Updated Internal schematic on cover page.
21-Jul-2023	3	Updated Features on cover page. Updated Table 1. Absolute maximum ratings and Table 2. Thermal data. Updated Figure 1. Safe operating area. Updated Section 3.1 STPAK package information.

Contents

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved