Customer Specific Device from onsemi

LDO Regulator, 400 mA, Fast, Very Low Dropout, CMOS, with Bias Rail

SCY99376

The SCY99376 is a 400 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides accurate output voltage with ultra−fast dynamic response. Suitable for noise sensitive applications. In order to optimize performance for battery operated portable applications, the SCY99376 features low I_Q consumption. The WLCSP6 0.99 mm x 0.65 mm, 0.35P Chip Scale package is optimized for use in space constrained applications.

Features

- Input Voltage Range: V_{OUT} to 3.6 V
- Bias Voltage Range: 2.5 V to 3.6 V
- Fixed Voltage Version Available
- Output Voltage Range: 0.5 V to 1.8 V, Resolution 25 mV
- ±0.8% Accuracy over −5°C to 85°C Temp. Range
- Ultra−Low Dropout: 27 mV at 400 mA
- Very Low Bias Input Current of Typ. 85 μA
- Excellent Output Load Transient Performance
- Low Noise, 7.5 μV_{RMS} Typ.
- Logic Level Enable Input for ON/OFF Control
- Normal and Slow Turn−On options Available
- Output Active Discharge Option Available
- Recommended Output Capacitance 2x 4 μF 0201 size
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery−powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

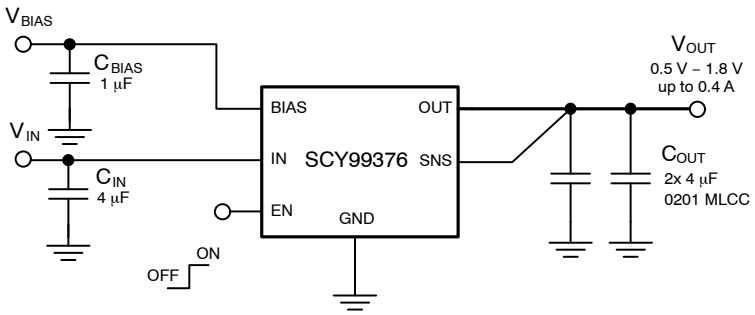
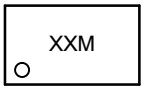


Figure 1. Typical Application Schematics

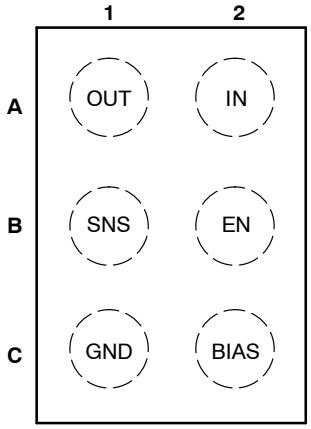
WLCSP6 0.99x0.65x0.29
CASE 567ZT

MARKING DIAGRAM



XX = Specific Device Code
M = Month Code

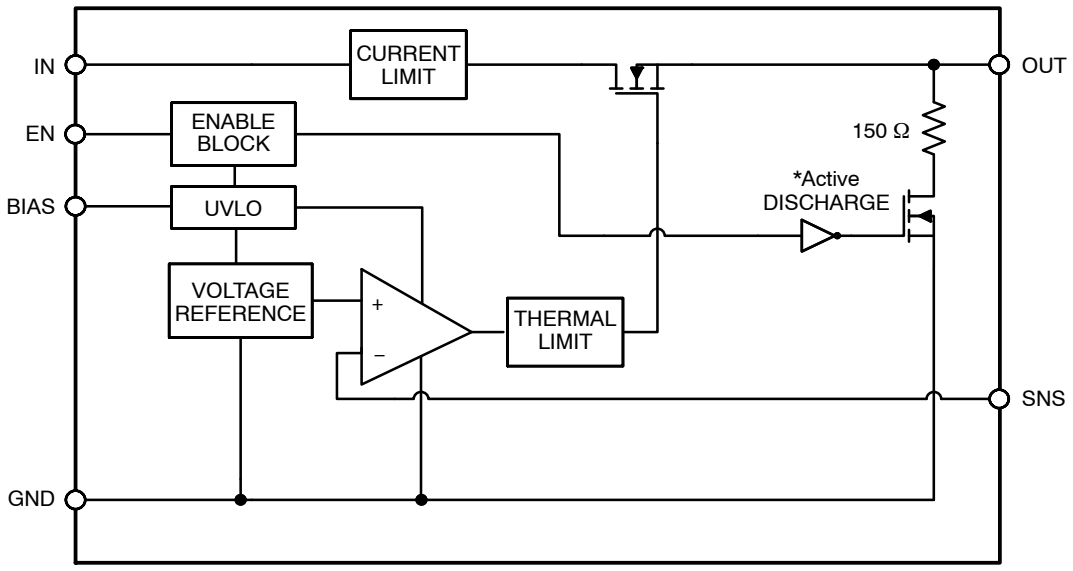
PIN CONNECTIONS



Top View

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.



*Active output discharge function is present only in SCY99376A and SCY99376C option devices.

Figure 2. Simplified Schematic Block Diagram − Fixed Version

PIN FUNCTION DESCRIPTION

Pin No. WLCSP6	Pin Name	Description
A1	OUT	Regulated Output Voltage pin
A2	IN	Input Voltage Supply pin
B1	SNS	Output voltage Sensing Input. Connect to Output on the PCB to output the voltage corresponding to the part version.
B2	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
C1	GND	Ground pin
C2	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under−Voltage Lockout Circuit.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 3.6	V
Output Voltage	V_{OUT}	−0.3 to (V_{IN}+0.3) ≤ 3.6	V
Chip Enable, Bias and SNS Input	V_{EN}, V_{BIAS}, V_{SNS}	−0.3 to 3.6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Charged Device Model tested per JS − 002 − 2018
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WLCSP6 − Case 567ZT Thermal Resistance, Junction−to−Air (Note 3)	$R_{\Theta JA}$	73	°C/W

3. This junction−to−ambient thermal resistance under natural convection was derived by thermal simulations based on the JEDEC JESD51 series standards methodology. Only a single device mounted at the center of a high_K (2s2p) 80 mm x 80 mm multilayer board with 1−ounce internal planes and 2−ounce copper on top and bottom. Top copper layer has a dedicated 1.6 mm^2 copper area.

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 85°C$; V_{BIAS} = 2.7 V or (V_{OUT} + 1.6 V), whichever is greater, $V_{IN} = V_{OUT(NOM)}$ + 0.3 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 4.7 μF, C_{OUT} = 2x 4 μF, C_{BIAS} = 1 μF, unless otherwise noted.
Typical values are at T_J = +25°C. Min/Max values are for $-40°C \le T_J \le 85°C$ unless otherwise noted. (Note 4)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range			V_{IN}	V_{OUT} + V_{DO}		3.6	V
Operating Bias Voltage Range			V_{BIAS}	(V_{OUT} + 1.50) ≥ 2.5		3.6	V
Undervoltage Lock−out	V_{BIAS} Rising Hysteresis		UVLO		2.1 0.1		V
Output Voltage Accuracy	$-5°C \le T_J \le 85°C$, $V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 3.6 V, 1 mA < I_{OUT} < 400 mA		V_{OUT}	−0.8		+0.8	%
Output Voltage Accuracy	$-40°C \le T_J \le 85°C$, $V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 3.6 V, 1 mA < I_{OUT} < 400 mA		V_{OUT}	−1.0		+1.0	%
V_{IN} Line Regulation	$V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ 3.6 V		$Line_{Reg}$		0.01		%/V
V_{BIAS} Line Regulation	2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 3.6 V		$Line_{Reg}$		0.01		%/V
Load Regulation	I_{OUT} = 1 mA to 400 mA		$Load_{Reg}$		2		mV
V_{IN} Dropout Voltage	I_{OUT} = 400 mA (Note 5)		V_{DO}		27	70	mV
V_{BIAS} Dropout Voltage	I_{OUT} = 400 mA, $V_{IN} = V_{BIAS}$ (Notes 5, 6)		V_{DO}		1.1	1.5	V
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	530	660	800	mA
SNS Pin Operating Current			I_{SNS}		0.1	0.5	μA
Bias Pin Quiescent Current	V_{BIAS} = 3.6 V, I_{OUT} = 0 mA		I_{BIASQ}		85	130	μA
Bias Pin Disable Current	V_{EN} ≤ 0.4 V		$I_{BIAS(DIS)}$		0.5	1	μA
Input Pin Disable Current	V_{EN} ≤ 0.4 V		$I_{VIN(DIS)}$		0.5	1	μA
EN Pin Threshold Voltage	EN Input Voltage “H”		$V_{EN(H)}$	0.9			V
	EN Input Voltage “L”		$V_{EN(L)}$			0.4	
EN Pull Down Current	V_{EN} = 3.6 V		I_{EN}		0.3	1	μA
Output Voltage Undershoot	I_{OUT} = 10 mA to 300 mA in 1 μs C_{OUT} = 2x 4 μF, 0201		$V_{OUT(USH)}$			−25	mV
Output Voltage Overshoot	I_{OUT} = 300 mA to 10 mA in 1 μs C_{OUT} = 2x 4 μF, 0201		$V_{OUT(OSH)}$			25	mV
Power Supply Rejection Ratio	V_{IN} to V_{OUT}, $V_{IN} = V_{OUT}$ + 0.1 V, I_{OUT} = 150 mA, C_{OUT} = 2x 4 μF, 0201	f = 100 Hz	PSRR(V_{IN})		75		dB
		f = 1 kHz			80		
		f = 10 kHz			60		
		f = 100 kHz			40		
	V_{BIAS} to V_{OUT}, $V_{IN} = V_{OUT}$ + 0.1 V	f = 1 kHz	PSRR(V_{BIAS})		80		dB
Output Noise Voltage	$V_{IN} = V_{OUT}$ + 0.1 V, f = 10 Hz to 100 kHz	I_{OUT} = 10 mA	V_N		9.9		μV_{RMS}
		I_{OUT} = 400 mA			7.5		
Thermal Shutdown Threshold	Temperature increasing				160		°C
	Temperature decreasing				140		
Output Discharge Pull−Down	V_{EN} ≤ 0.4 V, V_{OUT} = 0.5 V, SCY99376A and SCY99376C option		R_{DISCH}		150		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
6. For fixed output voltages below 1.5 V, V_{BIAS} dropout does not apply due to a minimum Bias operating voltage of 2.5 V.

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 85°C$; I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 4 μF, C_{BIAS} = 1 μF.
Typical values are at T_J = +25°C. Min/Max values are for $-40°C \le T_J \le 85°C$ unless otherwise noted. (Note 7)

Parameter	Test conditions		Symbol	Min	Typ	Max	Unit
SCY99376xFCT090T2G V_{BIAS} = 3 V, V_{IN} = 1.25 V, C_{OUT} = 2x 4 μF, 0201							
Delay time	From assertion of V_{EN} to output voltage increase	'A' option	t_{DELAY}		100		μs
		'C' option			100		
Rise time	V_{OUT} rise from 10% to 90% $V_{OUT(NOM)}$	'A' option	t_{RISE}		21		
		'C' option			80		
Turn−On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$	'A' option	t_{ON}		140		
		'C' option			230		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

TYPICAL CHARACTERISTICS

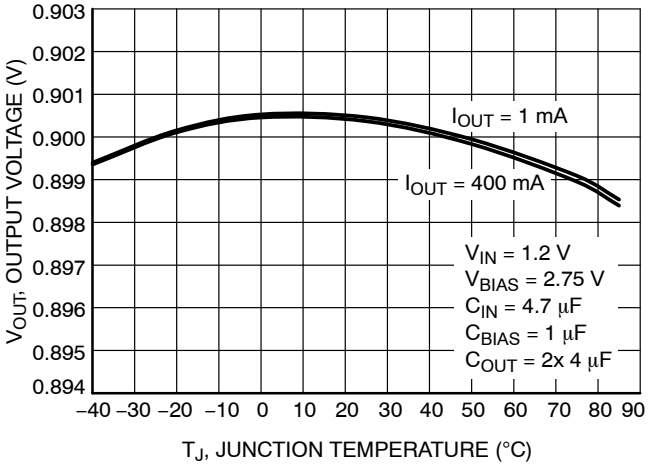


Figure 3. Output Voltage vs. Temperature

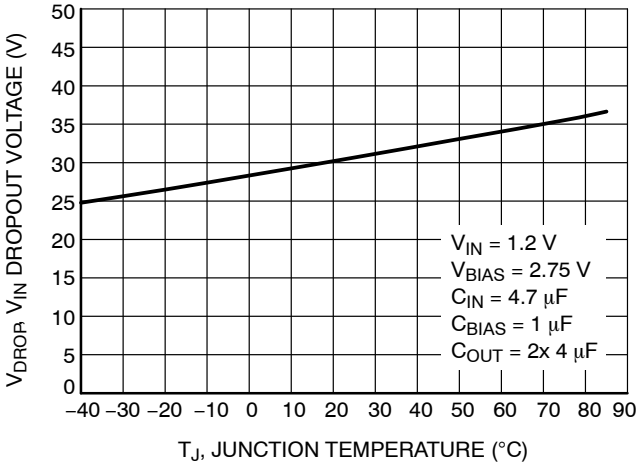


Figure 4. V_{IN} Dropout Voltage vs. Temperature

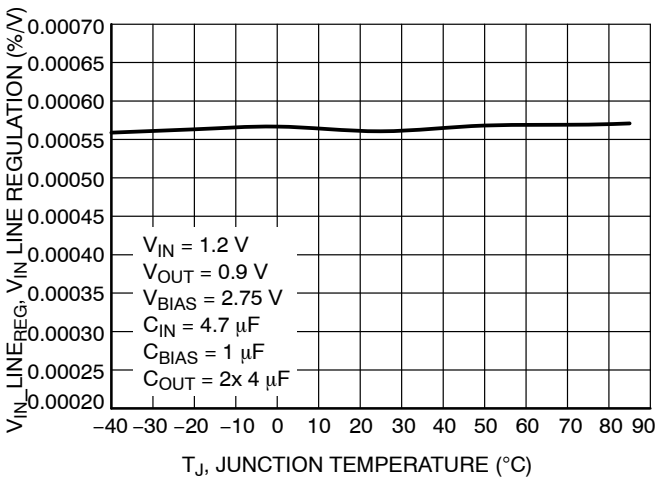


Figure 5. V_{IN} Line Regulation vs. Temperature

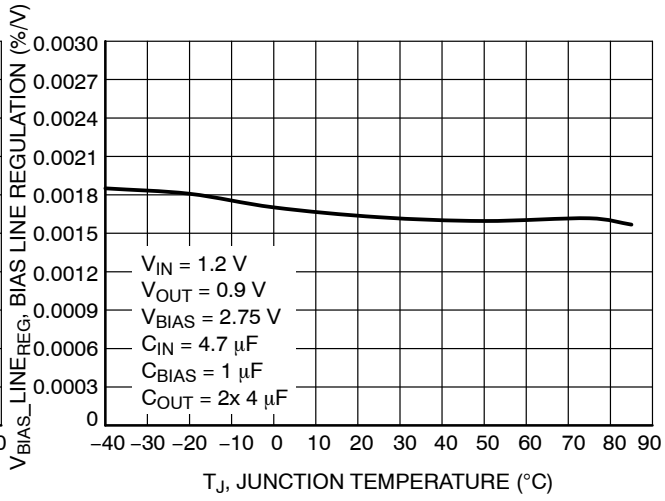


Figure 6. V_{BIAS} Line Regulation vs. Temperature

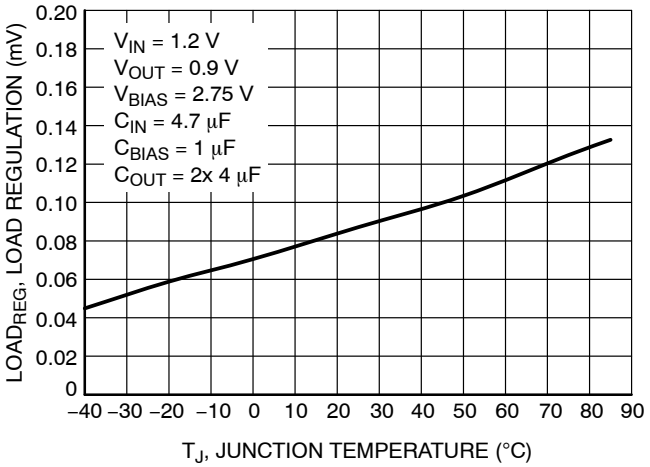


Figure 7. Load Regulation vs. Temperature

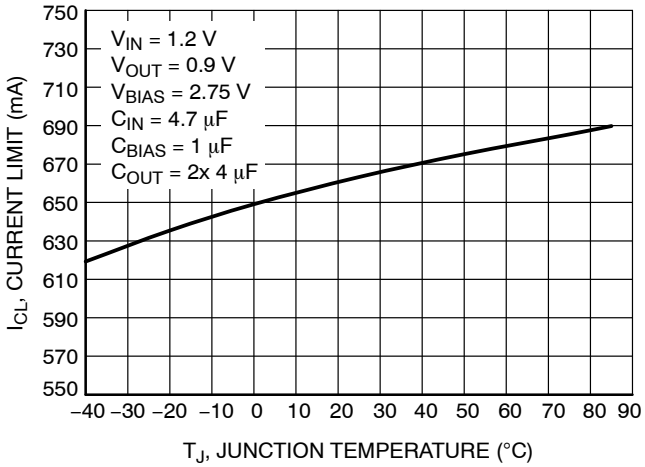


Figure 8. Current Limit vs. Temperature

TYPICAL CHARACTERISTICS

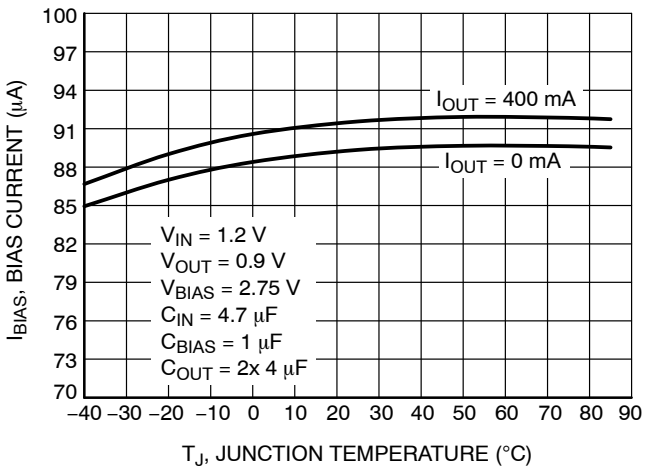


Figure 9. Bias Current vs. Temperature

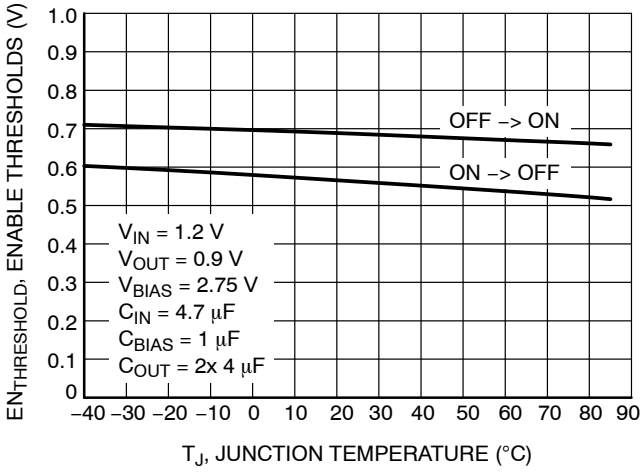


Figure 10. Enable Threshold vs. Temperature

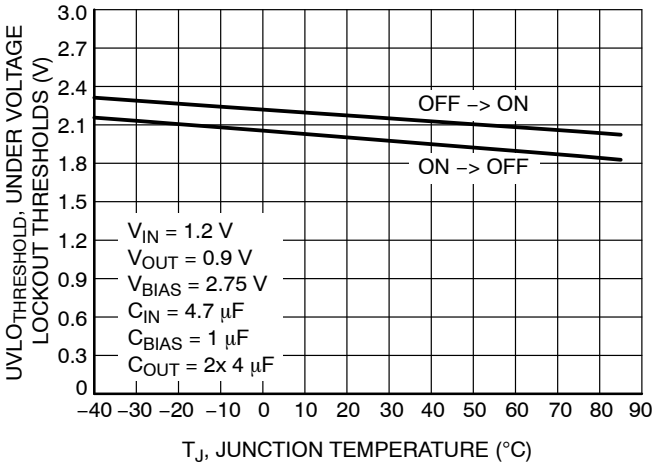


Figure 11. UVLO Thresholds vs. Temperature

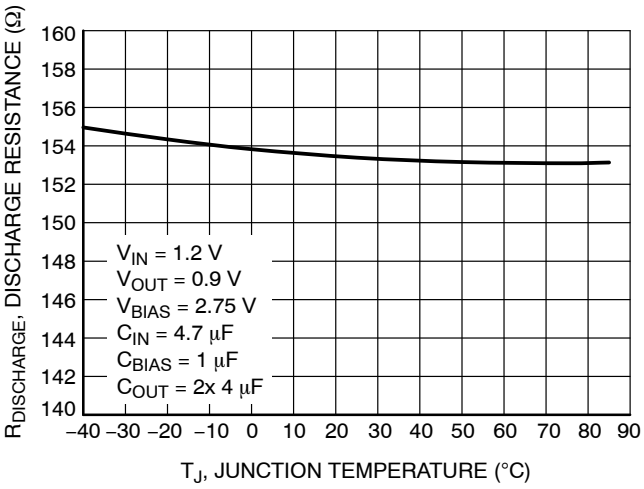


Figure 12. Discharge Resistance vs. Temperature

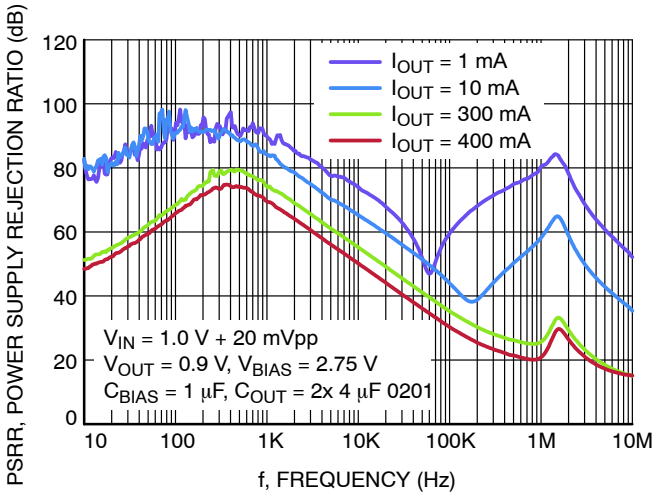


Figure 13. Power Supply Rejection Ratio – Ripple on V_{IN}

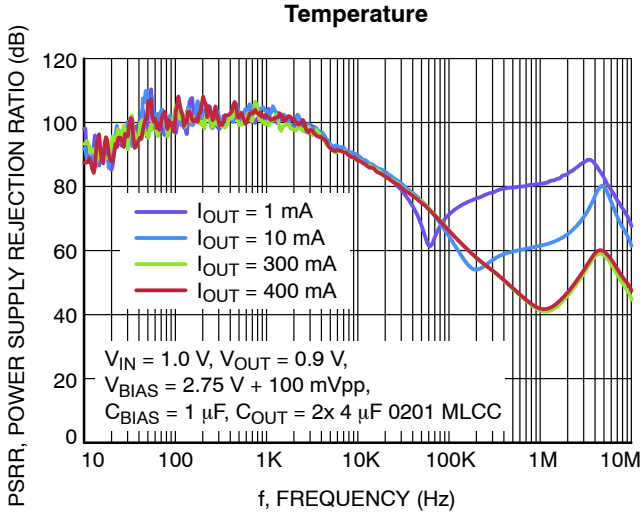


Figure 14. Power Supply Rejection Ratio – Ripple on V_{BIAS}

TYPICAL CHARACTERISTICS

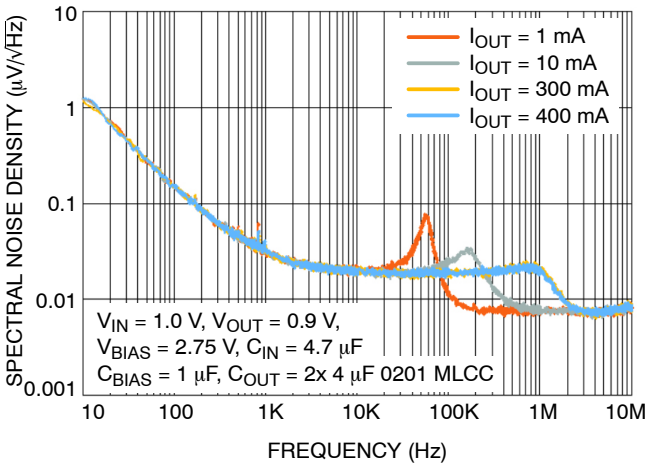


Figure 15. Output Voltage Noise Spectral Density – V_{OUT} = 0.9 V

I_{OUT}	RMS Output Noise (μV_{RMS})	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	11.8	11.0
10 mA	8.0	6.8
300 mA	7.5	6.3
400 mA	7.6	6.3

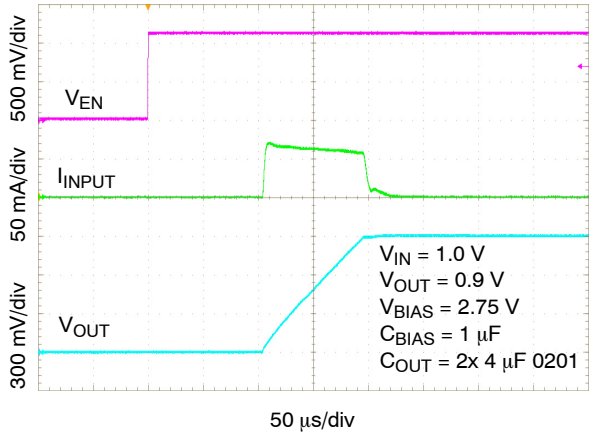


Figure 16. Enable Turn−on Response – I_{OUT} = 0 mA – “C” Option

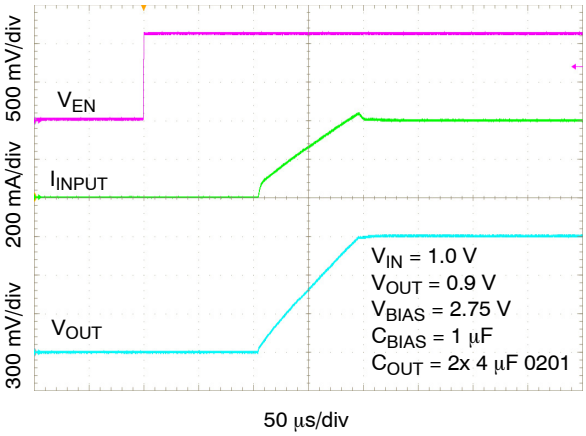


Figure 17. Enable Turn−on Response – I_{OUT} = 400 mA – “C” Option

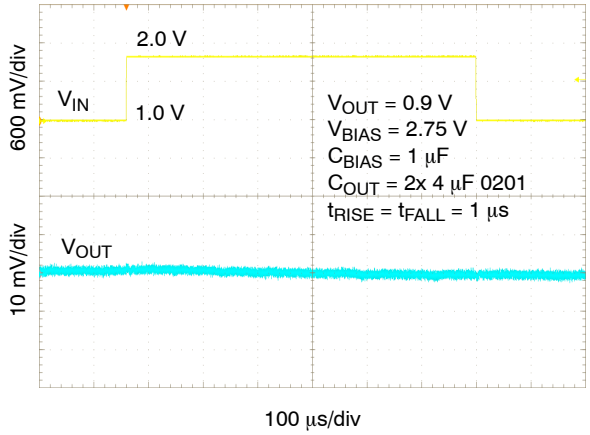


Figure 18. Line Transient Response – I_{OUT} = 1 mA

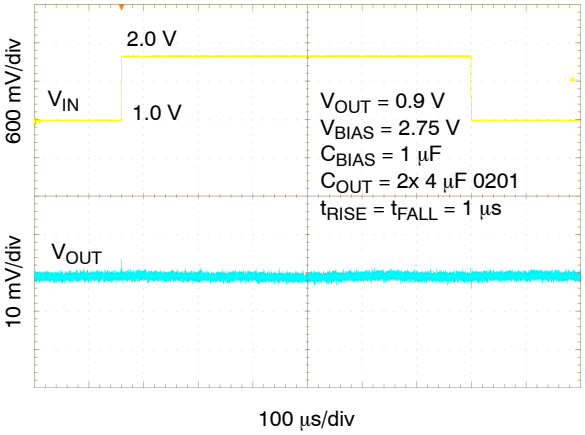


Figure 19. Line Transient Response – I_{OUT} = 100 mA

TYPICAL CHARACTERISTICS

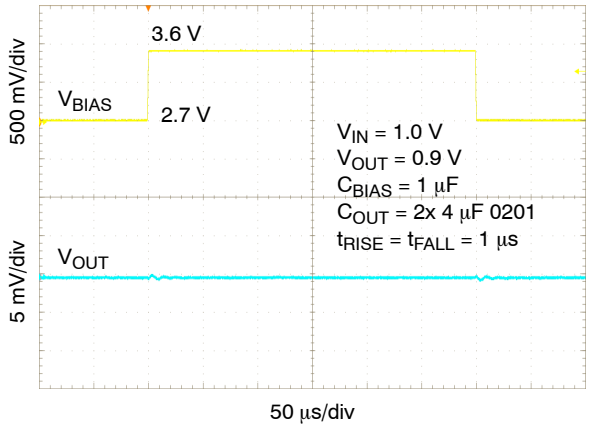


Figure 20. V_{BIAS} Line Transient Response – I_{OUT} = 1 mA

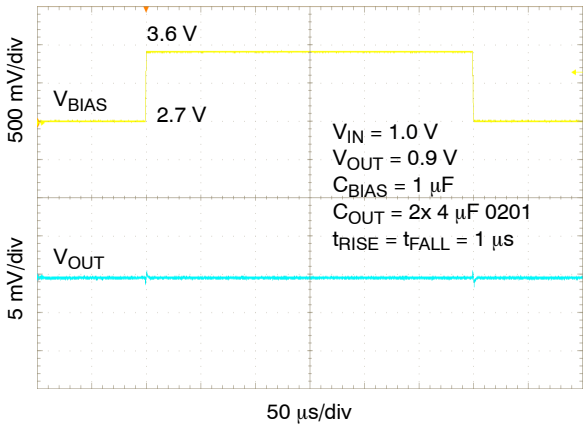


Figure 21. V_{BIAS} Line Transient Response – I_{OUT} = 300 mA

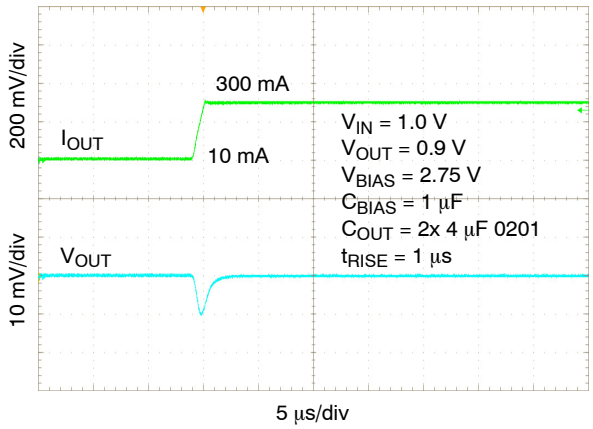


Figure 22. Load Transient Response – 10 mA to 300 mA

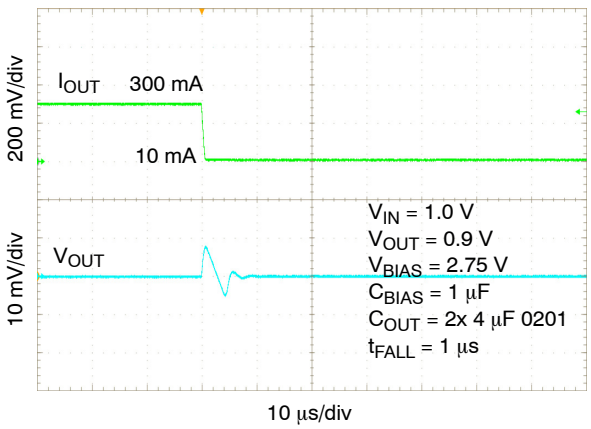


Figure 23. Load Transient Response – 300 mA to 10 mA

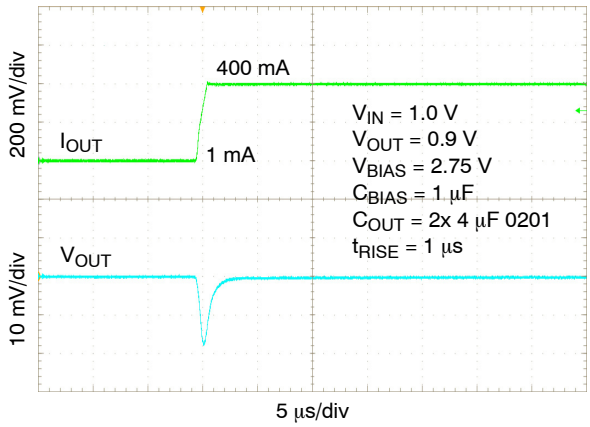


Figure 24. Load Transient Response – 1 mA to 400 mA

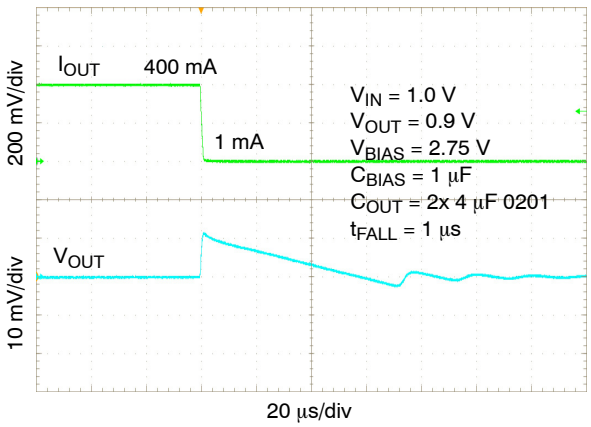


Figure 25. Load Transient Response – 400 mA to 1 mA

APPLICATIONS INFORMATION

The SCY99376 is 400 mA dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. The very low V_{IN} to V_{OUT} voltage difference is the most important factor to use NMOS topology. It allows to increase efficiency, reduce power dissipation and heating. Separate BIAS voltage allows very low output voltages like 0.5 V with just 0.6 V power input voltage while maintaining excellent dynamic performance. Tiny 6−pin WLCSP package in connection with 0201 size capacitors provide excellent solution for space constrains application like smartphones, camera modules, etc.

The SCY99376 offers smooth monotonic start−up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis.

Dropout Voltage

Because of two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output, there are two Dropout voltages specified.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN} - V_{OUT}$) when V_{OUT} starts to decrease by percent specified in the Electrical Characteristics table. V_{BIAS} is high enough.

The second, the V_{BIAS} dropout ($V_{BIAS} - V_{OUT}$) is the state when internal NMOS gate driving voltage is not enough to open pass device more and V_{OUT} drops down to specified level. The both values are published in the Electrical Characteristics table.

Under Voltage Lock−out (UVLO)

The device incorporates under voltage lockout protection (UVLO) to ensure safe start and shutdown when bias voltage rise or fall. The UVLO threshold is set to approximately 2.1 V. When V_{BIAS} is below this threshold device is disabled even EN is high. If V_{BIAS} crosses the threshold then soft start feature is activated and V_{OUT} is rising smoothly. The UVLO has built−in 100 mV hysteresis to prevent turning device ON and OFF when BIAS voltage oscillating around threshold level. If V_{BIAS} falls below $UVLO_{THRES}-UVLO_{HYST}$ the device is turned off.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. To get the full functionality of Soft Start, it is recommended to turn on the V_{IN} and V_{BIAS} supply voltages first and activate the Enable pin no sooner than V_{IN} and V_{BIAS} are on their nominal levels. If the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS}. If EN is connected to V_{IN} be careful about EN threshold.

If the EN pin voltage is < 0.4 V the device is guaranteed to be disabled. The pass transistor is turned off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active (devices with Output Active Discharge feature only) so that the output voltage V_{OUT} is pulled down to GND through a 150 Ω resistor. In the disable state the device consumes as low as typ. 0.5 μA from the V_{IN} and 0.5 μA from V_{BIAS}.

If the EN pin voltage is > 0.9 V the device is guaranteed to be enabled. The SCY99376 regulates the output voltage and the active discharge transistor is turned off.

The EN pin has internal pull−down current source with typ. value of 0.3 μA which assures that the device is turned off when the EN pin is not connected.

Slew Rate Control

The device is optimized for camera sensor application and meets all requirements for using in modern camera applications such as a smartphones, cameras and image capture devices. Power supply specification of sensors often requires output voltage slew rate limitation to protect sensor during regulator start−up. The SCY99376 incorporates soft−start feature which can assure smooth output voltage ramp without excess current spikes and voltage undershoots. The device provides two options of slew rate speed, ‘Normal’ means typical rise time approx. 20 μs and ‘Slow’ option means rise time about 100 μs. More detail about star−up timing is specified in electrical table.

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short. The device uses constant current limitation approach to protect against damage which means that output voltage drops down and output current keeps similar level specified by parameter I_{CL} in Electrical characteristic. The I_{CL} value is defined when V_{OUT} falls down to 90% nominal output voltage.

Thermal Protection

When the die temperature exceeds the Thermal Shutdown threshold (TSD − 160°C typical), Thermal Shutdown event is detected and output voltage is turned−off, immediately.

Once the device temperature falls below the 140°C regulator is turned−on again. The soft start feature is activated when output voltage is turned−on after TSD event. The internal built in hysteresis prevents excessive output OFF and ON switching and provides additional time to die cooling.

The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipation in the device increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is

dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affects the rate of junction temperature rising for the part.

The maximum power dissipation the device can handle is given by:

$$P_{D(MAX)} = \frac{85°C - T_A}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the device for given application conditions can be calculated from the following equations:

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} + V_{BIAS} \cdot I_{GND} \quad \text{(eq. 2)}$$

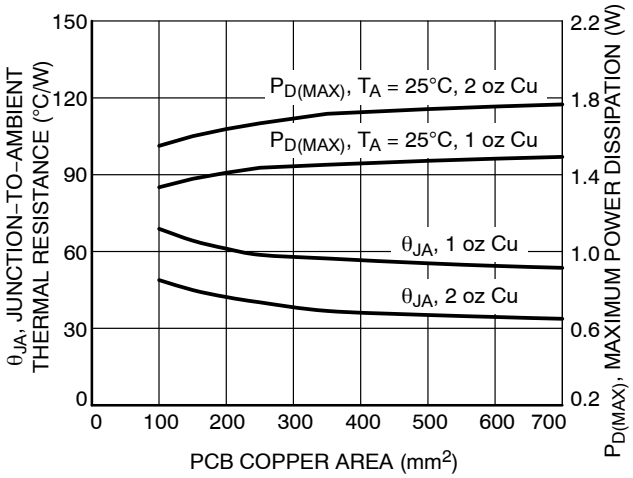


Figure 26. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area

Reverse Current

The NMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The SCY99376 is very fast device which features very good Power Supply Rejection ratio even with very small V_{IN}−V_{OUT} headroom. The lowering headroom, real input voltage must be watched carefully to avoid LDO drop out and performance degradation. If desired the PSRR at higher frequencies in the range 1 MHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Input Capacitor Selection (C_{IN})

It is recommended to connect at least a 4 μF Ceramic X5R or X7R capacitor as close as possible to the IN pin of the device. Larger input capacitor may be necessary if fast and large load transients are encountered in the application. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. or max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Bias Capacitor Selection (C_{BIAS})

The bias pin provides supply voltage for internal circuitry and could affect device performance. The 1 μF decoupling capacitor should be connected as close as possible to BIAS pin to provide low impedance path for unwanted AC signal coupled on bias line. The BIAS capacitor also provides stable voltage for internal reference and regulation loop which improve device performance. The X7R or X5R ceramic capacitor are recommended for their reliable performance over wide temperature range.

Output Decoupling Capacitors (C_{OUT})

The SCY99376 is designed to achieve the best in class dynamic response. It brings some specific requirements to output capacitor selection. The only quality X7R, X5R and better ceramics capacitors should be used.

The SCY99376 is fully stable over all conditions with nominal 2x 4 μF 0201 output capacitor or more. Capacitors of this size have significant capacitance DC−derating. This fact should be kept in mind in output capacitor selection. The Figure 27. shows capacitance derating for three different package size.

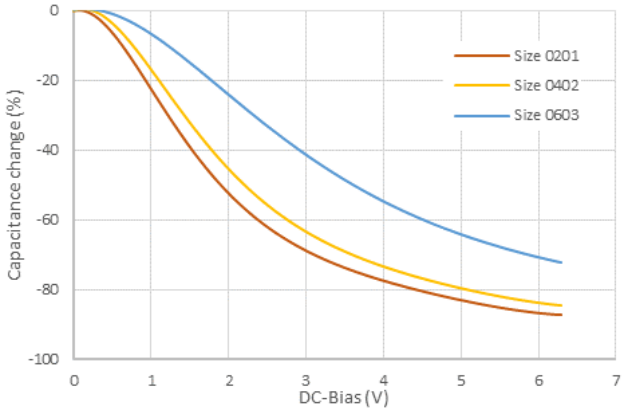


Figure 27. Capacitance Change vs. DC Voltage Applied

Capacitance change is also depended on capacitor thickness. For applications where small PCB area is limitation but height is not critical the thicker capacitor with same footprint provides better effective capacitance.

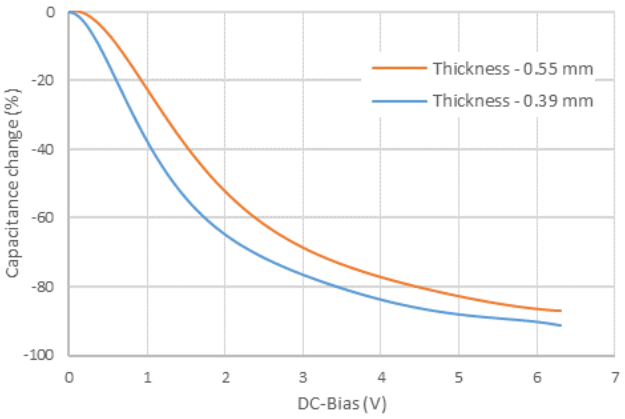


Figure 28. Capacitance Change vs. Caps Package Thickness

The minimum effective capacitance is 2 μF. The device is not sensitive to high total output capacitance and can handle capacity up to 47 μF. The SCY99376 can also handle additional capacitors spread over board.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics output capacitors should be placed as closed as possible to output pin. The SCY99376 includes dedicated SNS pin which should be connected directly to output capacitors to keep device stable and high performance. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). The Figure 29 shows recommended PCB layout.

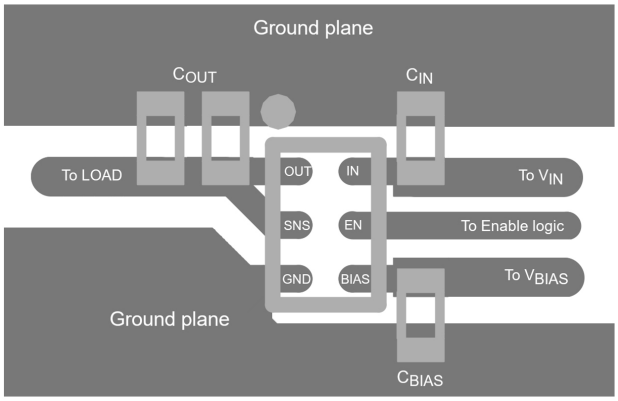


Figure 29. Recommended PCB Layout

To increase application efficiency as small as possible V_{IN}−V_{OUT} headroom is desirable. It is necessary to be very careful in PCB design because any additional PCB resistance between LDO power source and input pin causes voltage drop which further reduces voltage headroom.

ORDERING INFORMATION

Device	Output Voltage	Marking	Option	Package	Shipping†
SCY99376CFCT090T2G (In Development)	0.9 V	DA	Output Active Discharge, Slow Turn−On Slew Rate	WLCSP6 Case 567ZT (Pb−Free) UBM: 210 μm Bump Type: (98.2% Sn/1.8% Ag) Plate	10,000 / Tape & Reel
SCY99376CFCT080T2G (In Development)	0.8 V	TBD			

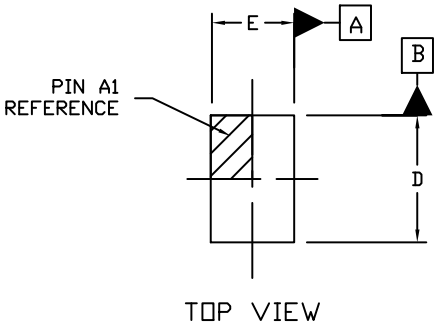
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. To order other package and voltage variants, please contact your **onsemi** sales representative.

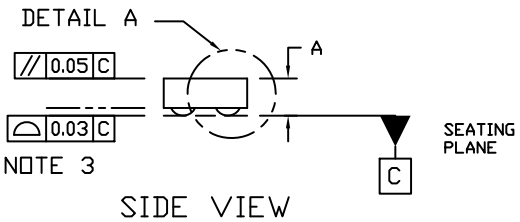
SCY99376

PACKAGE DIMENSIONS

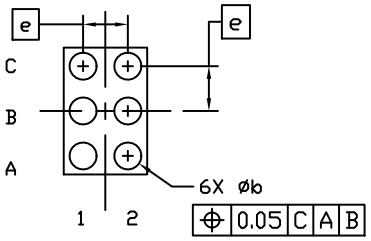
WLCSP6 0.99x0.65x0.29
CASE 567ZT
ISSUE B



TOP VIEW

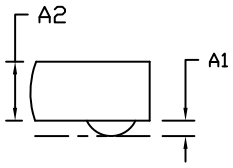


SIDE VIEW



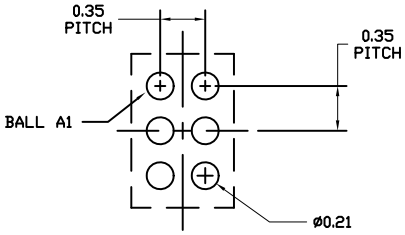
BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO DATUM C.



DETAIL A

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.250	0.290	0.330
A1	0.040	0.060	0.080
A2	0.23 REF		
b	0.180	0.210	0.240
D	0.940	0.990	1.040
E	0.600	0.650	0.700
e	0.35 BSC		



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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