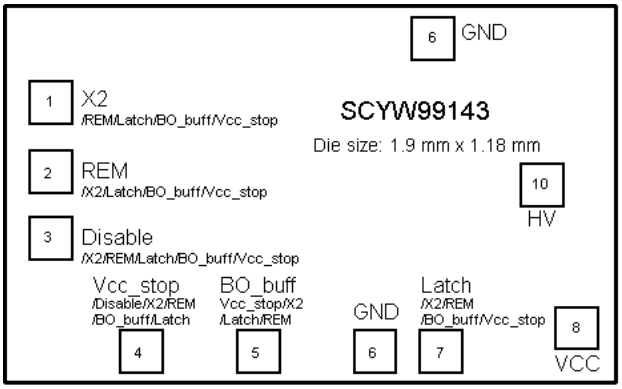
SCYW99143

Universal High Voltage Control Block for SMPS Controllers with Extremely Low Stand-by Power Consumption

Product Preview

The SCYW99143 is an HV control circuit specifically designed for flyback and other SMPS controllers for applications with extremely low no−load consumption. The internal startup current source supplies the SCYW99143 DIE and slaved SMPS controller during start−up. This function greatly simplifies the design of the auxiliary supply. The built−in Brown−out protection with X2 capacitor discharger allow for omitting inefficient resistor networks which usage would result in unacceptable standby power consumption increase. An Off−mode allows reaching extremely low no−load input power consumption by turning whole device off and thus minimizing the power consumption of the control circuitry.

PAD CONNECTIONS



Features

- High Voltage Start Up
- Internal Brown−Out Protection
- Buffered Brown−Out Divider Output Available
- Automatic and Lossless X2 Capacitor Discharge Function
- Remote Input for Standby Operation Control
- Active ON or OFF Off−mode Options
- Auto−Recovery Timer
- Open Collector Switch for Disabling Slave SMPS Controller
- Up to 28−V V_{cc} Operation
- Extremely Low No−load Standby Power
- Latched Short−Circuit Protection (only for co−package option)
- Internal Thermal Shutdown with Hysteresis
- This is a Pb−Free Device

Typical Applications

- Flyback and Other SMPS Converters with Extremely Low Stand−by Power Consumption

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

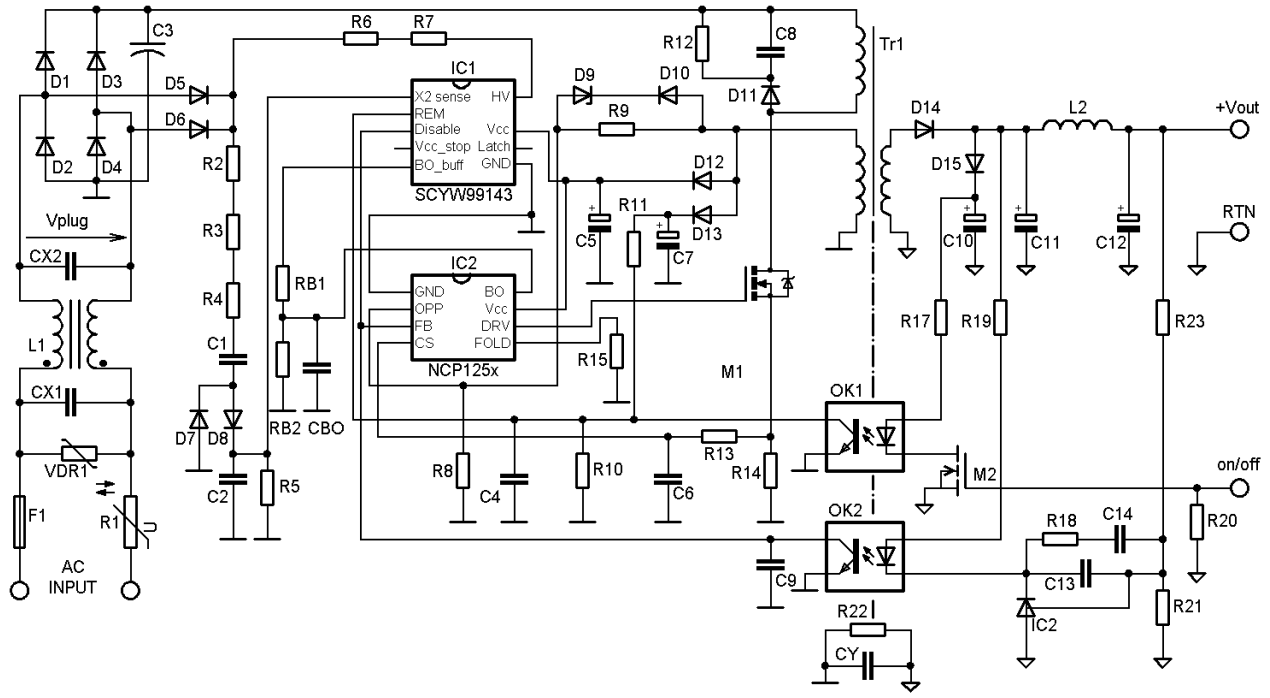


Figure 1. Typical Application Example (Active ON)

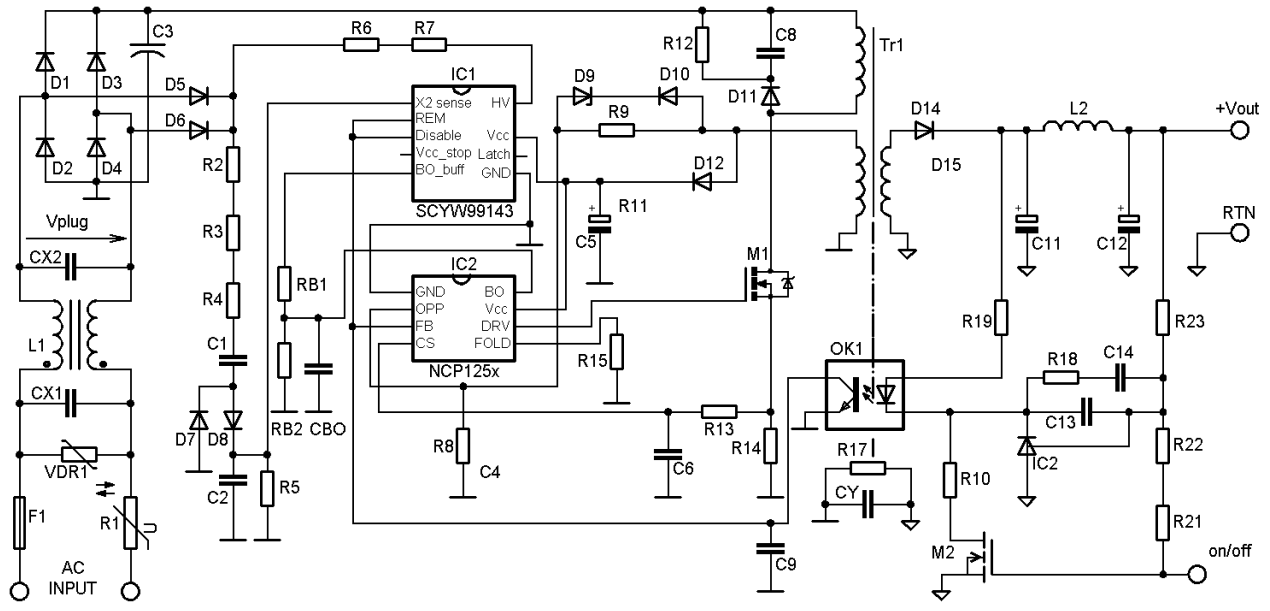


Figure 2. Typical Application Example (Active OFF)

Table 1. PAD CONNECTIONS

Pad No.	Pad Name	Function	Pad Description
1	X2	X2 discharge sense input	Detects AC line presence and activates X2 discharge circuitry with certain delay when the application is unplugged from the mains.
2	REM	Remote input	Initiates ultra low consumption mode (off−mode) when cross V_REM_off.
3	Disable	Open collector	Open collector to grounding FB pin to disable the second controller
4	VCC_stop	VCC start input for communication between two ICs	Voltage input to detect that second controller reaches $VCC_{(on)}$ threshold
5	BO_buff	Brown out divider output	Output signal of integrated Brown out sensing network
6	GND	−	The HV controller ground.
7	Latch	Latch input for communication between two ICs or outside latch condition	The SCYW99143 can be latched−off via this input when used as a standalone IC or for Latch signal from second controller (inter−bonding connection) to detect transition to latch−off mode..
8	V_{cc}	Supplies the controller	This pin is connected to an external auxiliary voltage and supplies the controller.
10	HV	HV startup input	Connects internal HV startup current source to rectified AC input line. Allows for lossless Brown Out detection. Discharges X2 capacitor(s) when application is unplugged from the mains.

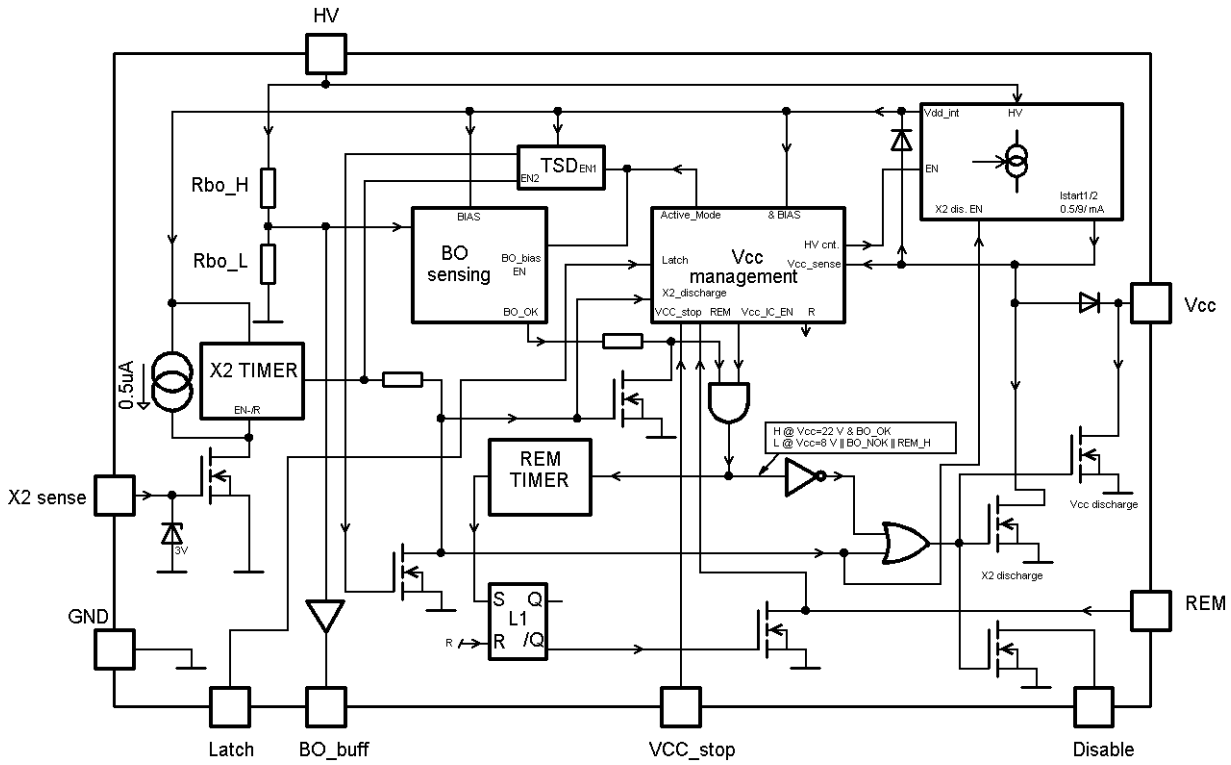


Figure 3. Internal Circuit Architecture (Active ON)

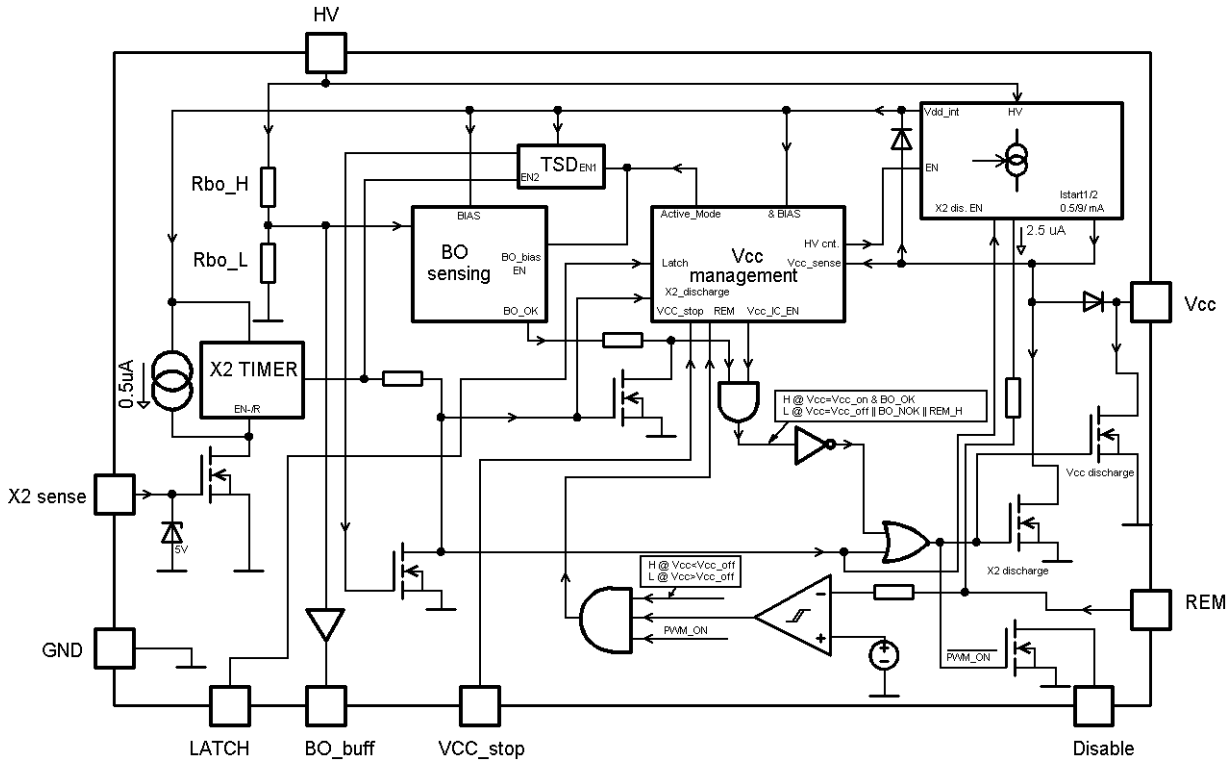


Figure 4. Internal Circuit Architecture (Active OFF)

Table 2. MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{cc}	Power Supply voltage, V_{cc} pad, continuous voltage	−0.3 to 28	V
V_{pad_x}	Voltage on all pads (except pads 8 and 10)	−0.3 to 10	V
V_REM_Active OFF	Voltage on all pins / pads 2 for Active Off version	−0.3 to 5	V
V_HV	High Voltage Pad (pad 10)	−0.3 to 500	V
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air (50 mm^2 x 35 μm Cu)	211	°C/W
$T_{J,max}$	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, HBM model, all pins	2	kV
	ESD Capability, Machine Model	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC standard JESD22, Method A114E
   Machine Model Method 200 V per JEDEC standard JESD22, Method A115A
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

Table 3. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{cc} = 12 V unless otherwise noted)

Symbol	Rating	Pad	Option	Min	Typ	Max	Unit
HV STARTUP CURRENT SOURCE							
VHV_min	Minimum voltage for current source operation (Vcc = 4 V)	10	–	–	30	60	V
Istart1	Current flowing out of Vcc pin (Vcc = 0 V)	10, 8	–	0.2	0.5	0.8	mA
Istart2	Current flowing out of Vcc pin (Vcc = Vcc_on − 0.5 V)	10, 8	–	6	10	15	mA
Istart_off	Off−state leakage current (VHV = 500 V, Vcc < Vcc_on, V_REM = 0 V)	10	–	–	15	–	μA
IHV_off_mode_1	HV pin current when off−mode is active (VHV = 141 V, Vcc = 0 V)	10	–	–	–	15	μA
IHV_off_mode_2	HV pin current when off−mode is active (VHV = 325 V, Vcc = 0 V)	10	–	–	–	19	μA
VHV_min_off−mode	Minimum voltage on HV pin during off−mode (VREM = 10 V, Vcc = 0 V)	10	–	–	–	10	V
SUPPLY SECTION							
VCC_ON	Vcc increasing level at which disable switch is deactivated (Note 3)	8	VO1	19.5	22	24.5	V
			VO2	16.4	18	19.7	
			VO3	12.8	14	15.3	
VCC_OFF	V_{CC} decreasing level at which the disable switch is activated (Note 3)	8	VF1	10.4	11	12.1	V
			VF2	9.9	10.5	11.6	
			VF3	9.5	10	11	
			VF4	9	9.5	10.5	
			VF5	8.5	9	10	
			VF6	8	8.5	9.4	
			VF7	7.6	8	8.8	
			VF8	7.1	7.5	8.3	
			VF9	6.6	7	7.7	
VCC_HYST	Hysteresis Vcc_{ON}−Vcc_{OFF}	8	–	0.1	–	–	V
VCC_Bias	Vcc level during latch and auto−recover modes	8	–	4.7	5.5	6.3	V
VCC_INHIBIT	Vcc level for Istart1 to Istart2 transition	8	–	0.5	1	1.25	V
ICC	Internal IC consumption during on−mode	8	–	–	0.2	0.4	mA
BROWN−OUT							
V_BO_on	Brown−Out turn−on threshold (VHV going up) (VCC = VCC_Bias) (Note 3)	10	BO1	92	101	110	V
			BO2	102	111	120	
			BO3	104	112	120	
V_BO_off	Brown−Out turn−off threshold (VHV going down) (Note 3)	10	BF1	84	93	102	V
			BF2	94	103	112	
			BF3	97	105	113	
BO_timer	Timer duration for line cycle drop−out (Note 3)	10	–	43	–	86	ms

3. Possible modification by metal option.
4. If this signal is not connected, the function is not activated.
5. Minimum load impedance connected to BO_buff pin is 1 MΩ parallel with 1 nF.
6. Guaranteed by design.

Table 3. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{cc} = 12 V unless otherwise noted)

Symbol	Rating	Pad	Option	Min	Typ	Max	Unit
X2 DISCHARGE CIRCUITRY							
Vth_X2	X2 timer disable switch threshold voltage	1	–	1	1.5	2	V
Vth_X2_hyst	Hysteresis on the X2 pin (Note 6)	1		–	100	–	mV
V_X2_clamp	X2 input clamp voltage (I_X2_leak = 1 μA)	1	–	–	4	–	V
X2_timer	X2 timer duration (Note 3)	1	X1	70	–	140	ms
			X2	35	–	65	
			X3	17	–	33	
I_X2_leak	X2 input leakage current (V_X2 = 2.5 V)	1	–	–	–	0.3	μA
I_X2_dis	Maximum discharge switch current (VCC = 10 V)	10	–	6	10	13	mA
I_VCC_dis	VCC cap discharge switch resistance (VCC = 10 V)	1	–	6	10	13	mA
REMOTE INPUT ACTIVE ON							
V_REM_on	Remote pin voltage below which is the off−mode deactivated (V_REM going down) (Vcc = 0 V)	2	–	1	1.5	2	V
V_REM_off	Remote pin voltage above which is the off−mode activated (V_REM going up) (Note 3)	2	VR1	7.2	8	8.8	V
			VR2	5.4	6	6.6	
REM_timer	Remote timer duration (Note 3)	2	RT1	140	–	260	ms
			RT2	70	–	140	
			RT3	35	–	65	
			RT4	17	–	33	
R_SW_REM	Internal remote pull down switch resistance (V_REM = 8 V)	2	–	1000	–	3000	Ω
I_REM_leak	Remote input leakage current (V_REM = 9 V, Note 6)	2	–	–	0.02	1	μA
REMOTE INPUT ACTIVE OFF							
V_REM_on	Remote pin voltage above which is the off−mode deactivated (V_REM going up) (Vcc = 0 V)	2	–	1.5	2	2.5	V
V_REM_off	Remote pin voltage below which is the off−mode activated (V_REM going down) (Note 3)	2	VR3	0.18	0.2	0.22	V
			VR4	0.27	0.3	0.33	
			VR5	0.36	0.4	0.44	
I_REM_leak	Remote input leakage current (V_REM = 5 V, Note 6)	2	–	–	0.02	1	μA
I_REM_bias	Pull−up bias current which biased REM pin during off−mode	2	–	–	2.4	5	μA
INTERNAL COMMUNICATION FOR CO−PACKAGE OPTION							
Latch_input_on	Voltage level to start Latch−off mode (Note 4)	7	–	1.53	1.8	2.07	V
VCC_stop_on	Voltage level for detect that VCC is higher than secondary controller's $VCC_{(on)}$ (Note 4)	4	–	1.53	1.8	2.07	V
Pull_up_current	Pull−up current when VCC_stop_on or Latch_input_on signals are connected to open drain switch	4, 7	–	3	4	6	μA
Pull_down_current	Pull−down current when VCC_stop_on or Latch_input_on signals are connected to logic signal	4, 7	–	2	4	6	μA
R_BO_buff	Internal series resistance on BO_buff (Note 6)	5	–	–	10	–	kΩ

3. Possible modification by metal option.
4. If this signal is not connected, the function is not activated.
5. Minimum load impedance connected to BO_buff pin is 1 MΩ parallel with 1 nF.
6. Guaranteed by design.

Table 3. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{cc} = 12 V unless otherwise noted)

Symbol	Rating	Pad	Option	Min	Typ	Max	Unit
INTERNAL COMMUNICATION FOR CO−PACKAGE OPTION							
VBO_buff_ratio1	Ratio between voltage on HV and voltage on BO_buff (V_BO_on (typ) = 101 V) (Note 5)	10, 5	–	–	112:1	–	–
VBO_buff_ratio2	Ratio between voltage on HV and voltage on BO_buff (V_BO_on (typ) = 111 V) (Note 5)	10, 5	–	–	123:1	–	–
VBO_buff_ratio3	Ratio between voltage on HV and voltage on BO_buff (V_BO_on (typ) = 112 V) (Note 5)	10, 5	–	–	124:1	–	–
DISABLE SWITCH OUTPUT							
R_SW_Disable	Internal disable pull down switch resistance (Idisable = 500 μA)	3	–	–	250	500	Ω
LATCH INPUT (when pinned out)							
Vlatch	Voltage threshold above which the SCYW99143 enters latch−off mode	7	–	1.53	1.8	2.07	V
PROTECTIONS							
T_{A-rec_timer}	Auto−recovery timer duration (Note 3)	–	AT1	0.7	–	–	s
		–	AT2	1.4	–	–	
$T_{A-rec\_timer\_max}$	Maximum timer duration (Note 6)	–	–	–	–	3.8	s
TEMPERATURE SHUTDOWN							
T_{TSD}	Temperature shutdown (Note 3)	–	T1	–	150	–	°C
		–	T2	–	140	–	
		–	T3	–	130	–	
$T_{TSD(HYS)}$	Temperature shutdown hysteresis	–	–	–	30	–	°C

3. Possible modification by metal option.
4. If this signal is not connected, the function is not activated.
5. Minimum load impedance connected to BO_buff pin is 1 MΩ parallel with 1 nF.
6. Guaranteed by design.

Table 4. FUNCTION OPTIONS

Option	Internal BO	Active ON	Active OFF	Input signal for VCC start on	Input signal for Latch input on	Assembly
A	Yes	Yes	NO	Logic	Logic	Co−package
B	Yes	Yes	NO	Logic	Open drain	Co−package
C	Yes	Yes	NO	Open drain	Open drain	Co−package
D	Yes	Yes	NO	Open drain	Logic	Co−package
E	Yes	NO	Yes	Logic	Logic	Co−package
F	Yes	NO	Yes	Logic	Open drain	Co−package
G	Yes	NO	Yes	Open drain	Open drain	Co−package
H	Yes	NO	Yes	Open drain	Logic	Co−package
I	NO	Yes	NO	Logic	Logic	Co−package
J	NO	Yes	NO	Logic	Open drain	Co−package
K	NO	Yes	NO	Open drain	Open drain	Co−package
L	NO	Yes	NO	Open drain	Logic	Co−package
M	NO	NO	Yes	Logic	Logic	Co−package
N	NO	NO	Yes	Logic	Open drain	Co−package
O	NO	NO	Yes	Open drain	Open drain	Co−package
P	NO	NO	Yes	Open drain	Logic	Co−package
Q	Yes	Yes	NO	−	−	Standalone
R	Yes	NO	Yes	−	−	Standalone

DEVICE CODE: SCYW99143 FVOxVFxBOxBFxXxVRxRTxATxTx

Where:

F − Function option (A−R)

VOx − VCC_ON (VO1−VO3)

VFx − VCC_OFF (VF1−VF9)

BOx − VBO_ON (BO1−BO3)

BFx − VBO_OFF (BF1−BF3)

Xx − X2_timer (X1−X3)

VRx − V_REM_off − Active ON version (VR1, VR2), Active OFF version (VR3−VR5)

RTx − REM_timer (RT1−RT5)

ATx − Tautorec (AT1−AT2)

Tx − TSD (T1−T3)

TYPICAL CHARACTERISTICS

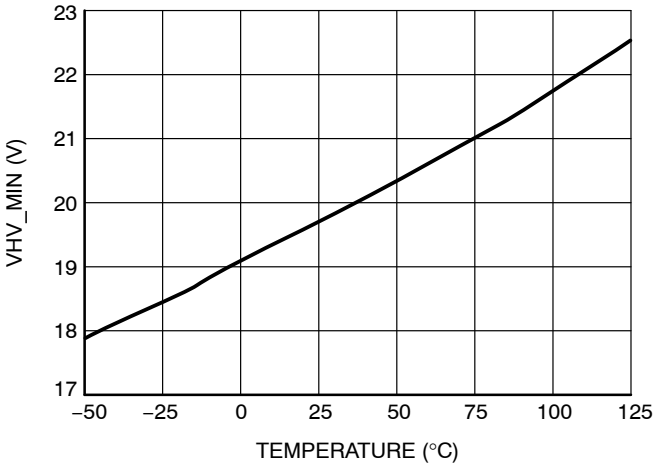


Figure 5. Minimum Current Source Operation, VHV_min

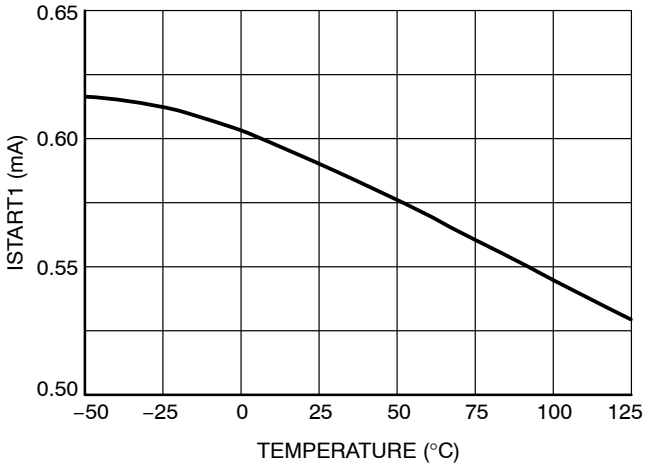


Figure 6. High Voltage Startup Current Flowing Out of VCC Pin, Istart1

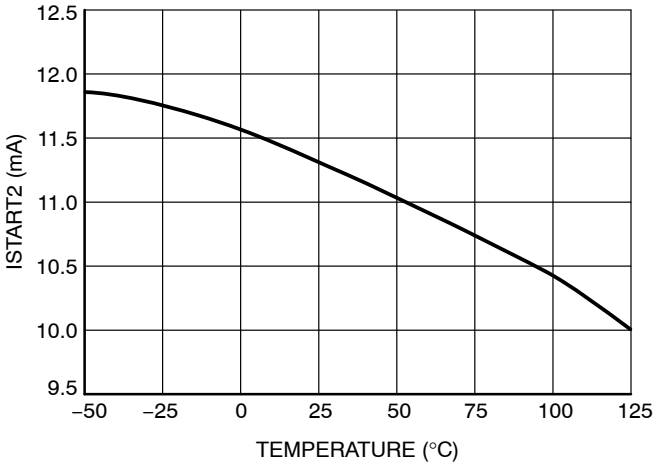


Figure 7. High Voltage Startup Current Flowing Out of VCC Pin, Istart2

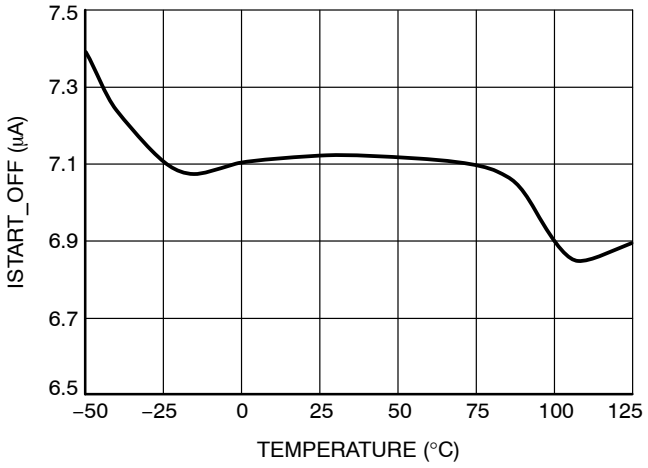


Figure 8. Off−state Leakage Current, Istart_off

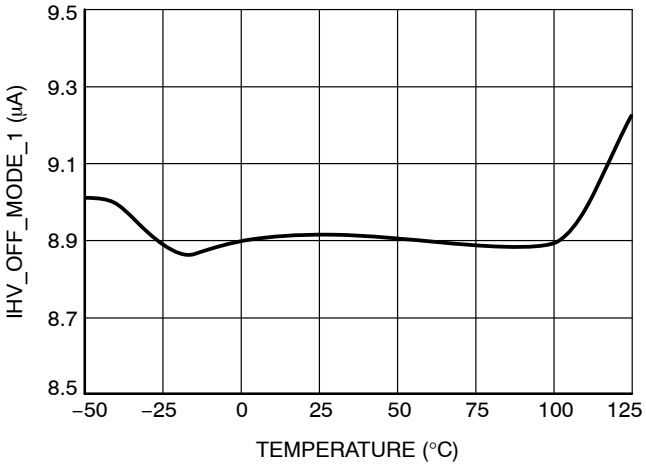


Figure 9. HV Pin Current during Off−mode, IHV_off_mode_1

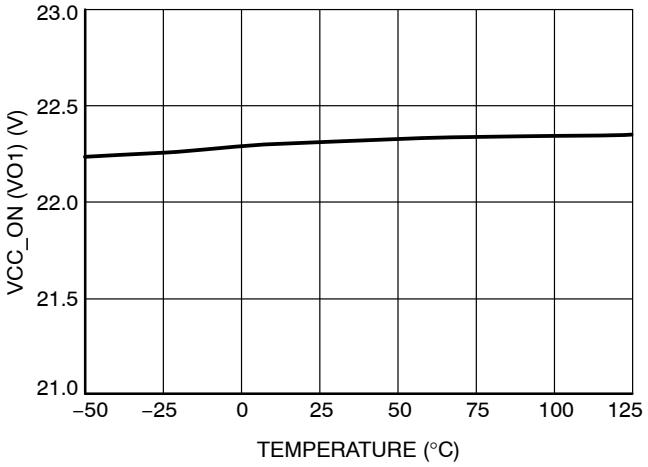


Figure 10. Vcc Increasing Level at which Disable Switch is Deactivated, VCC_ON (option VO1)

TYPICAL CHARACTERISTICS

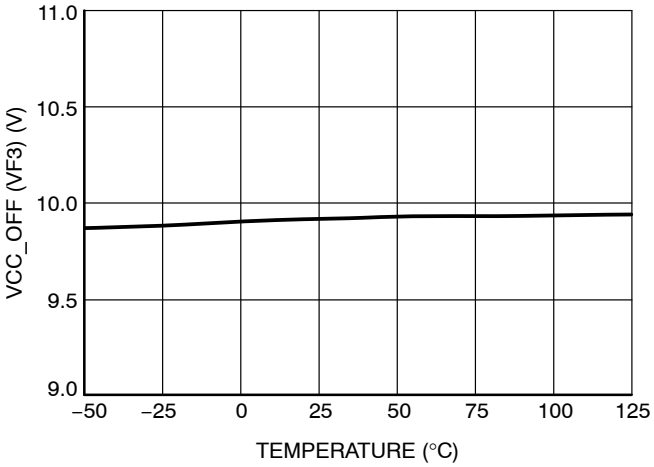


Figure 11. VCC Decreasing Level at which the Disable Switch is Activated, VCC_OFF (option VF3)

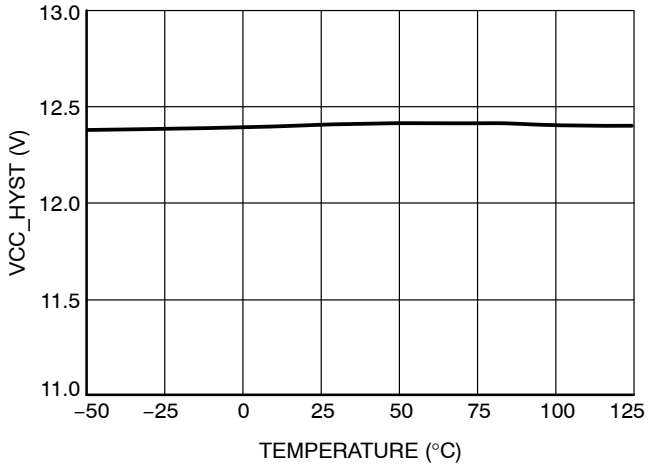


Figure 12. VCC Hysteresis, VCC_HYST

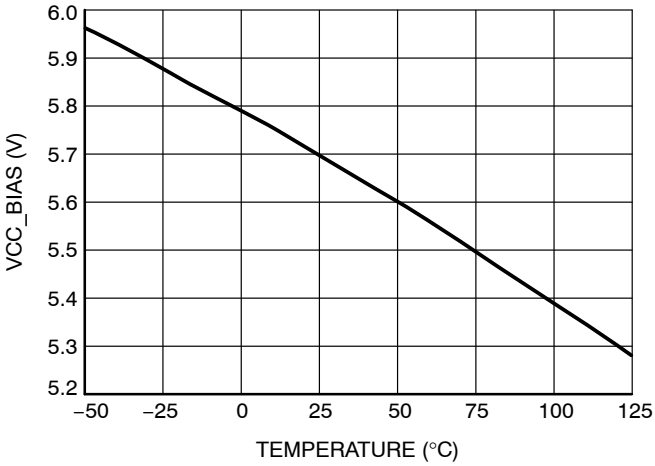


Figure 13. Vcc Level at Fault Modes, VCC_Bias

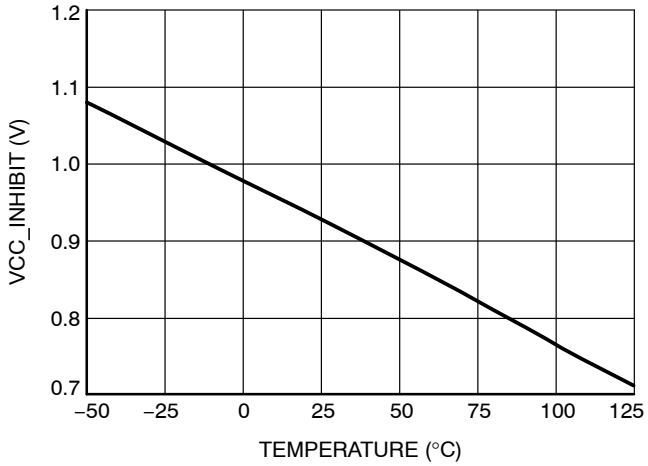


Figure 14. Vcc Level for Istart1 to Istart2 Transition, VCC_INHIBIT

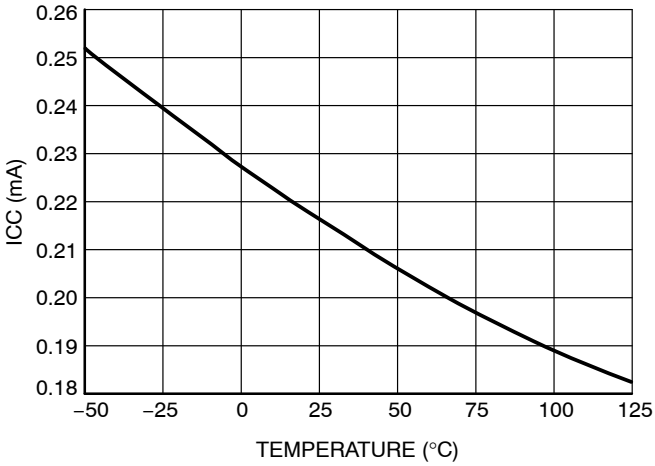


Figure 15. Internal IC Consumption during On−mode, ICC

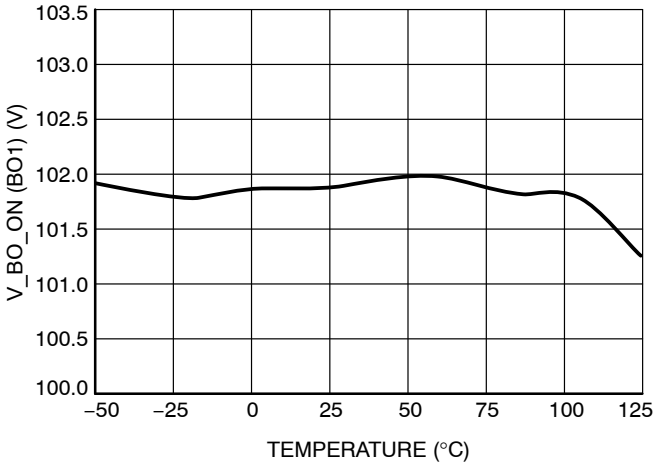


Figure 16. Brown−Out Turn−on Threshold, V_BO_on (option BO1)

TYPICAL CHARACTERISTICS

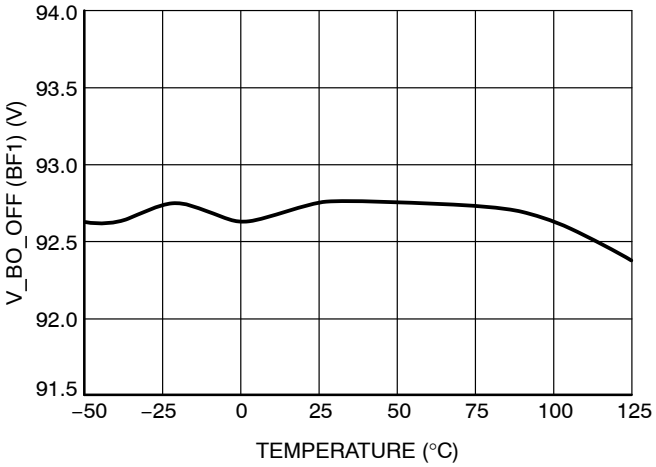


Figure 17. Brown−Out Turn−off Threshold, V_BO_off (option BF1)

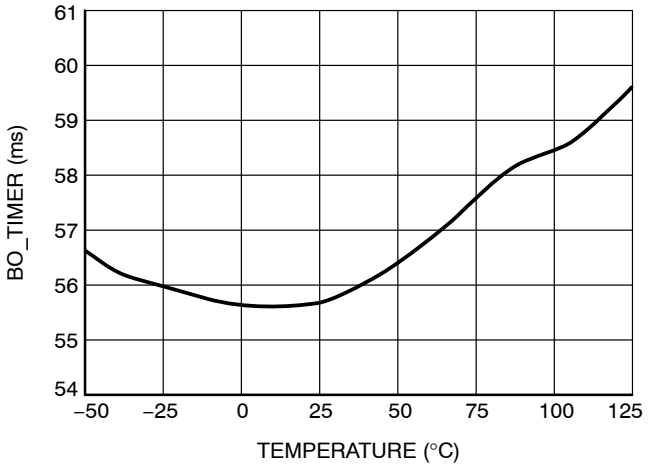


Figure 18. Timer Duration for Line Cycle Drop−out, BO_timer

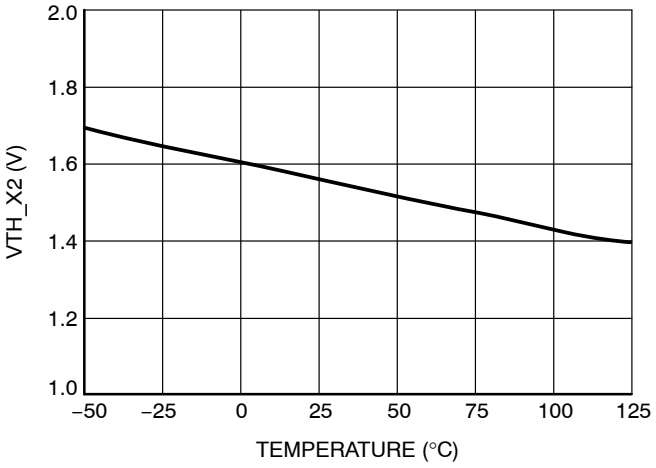


Figure 19. X2 Timer Disable Switch Threshold, VTH_X2

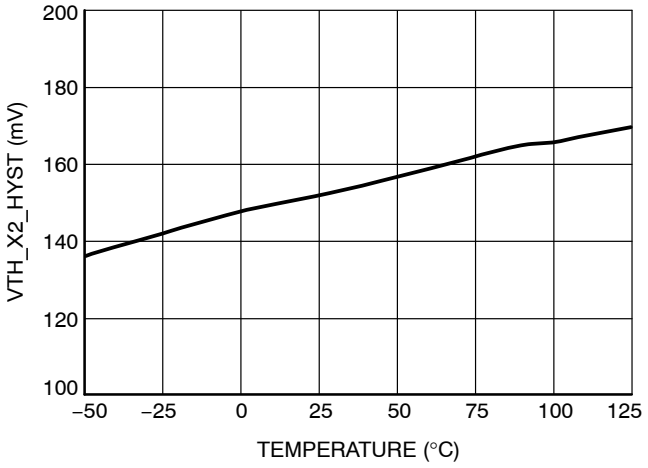


Figure 20. Hysteresis on the X2 Pin, VTH_X2_hyst

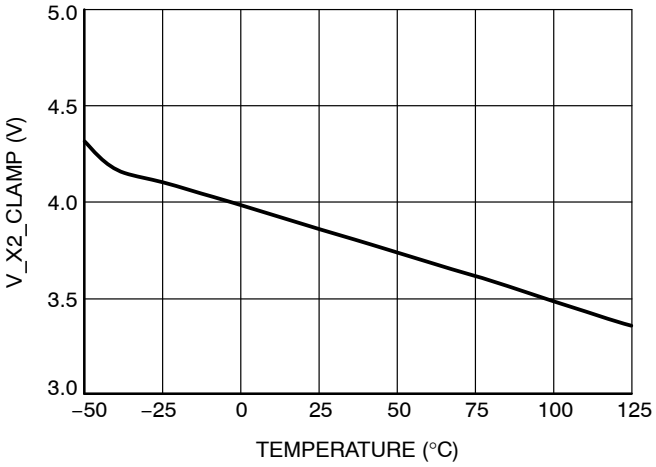


Figure 21. X2 Input Clamp Voltage, V_X2_clamp

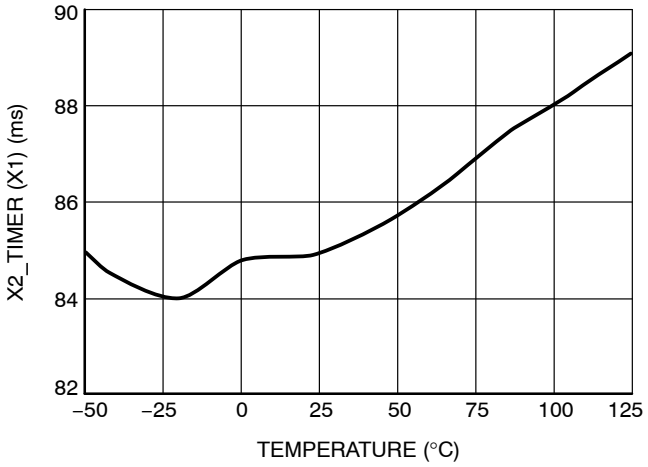


Figure 22. X2 Timer Duration, X2_timer

TYPICAL CHARACTERISTICS

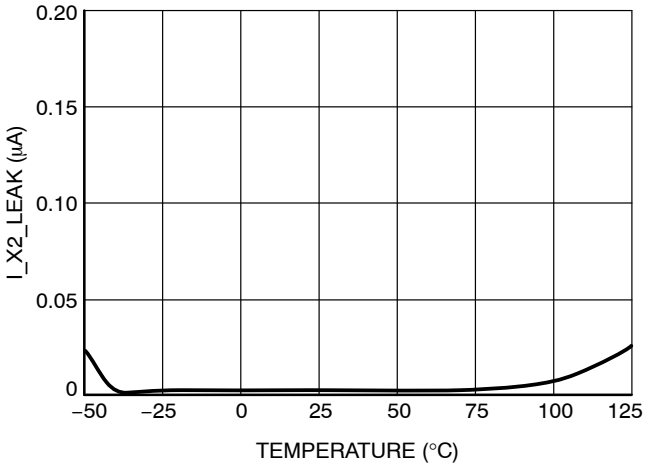


Figure 23. X2 Input Leakage Current, I_X2_leak

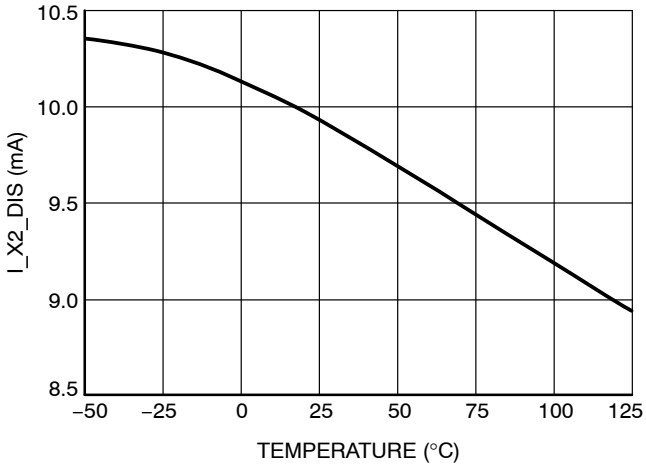


Figure 24. Maximum X2 Cap Discharge Current, I_X2_dis

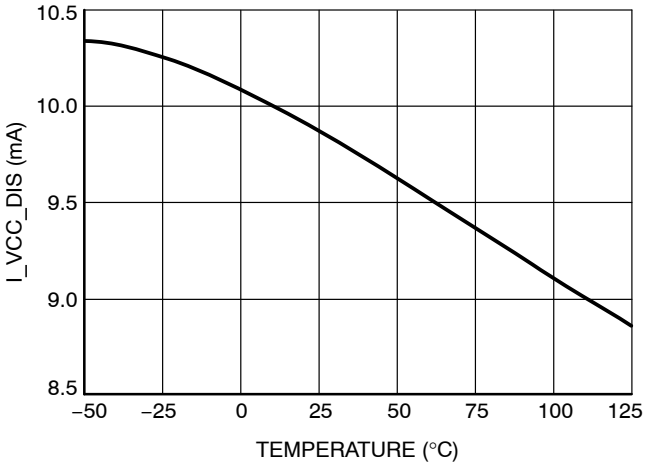


Figure 25. Maximum VCC Cap Discharge Current, I_VCC_dis

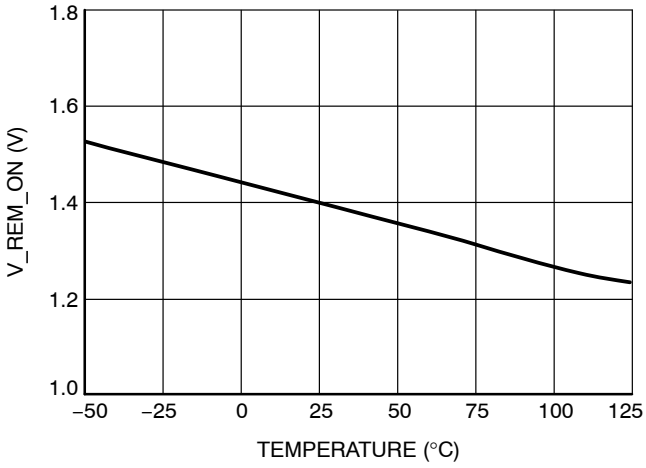


Figure 26. Off−mode Turn−off Threshold, V_REM_on

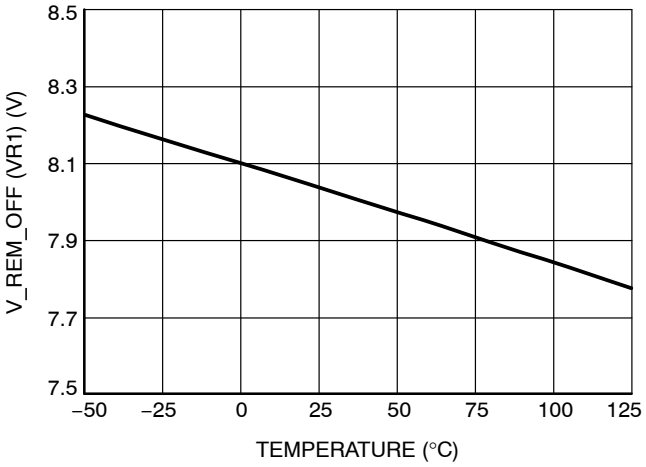


Figure 27. Off−mode Turn−on Threshold, V_REM_off (option VR1)

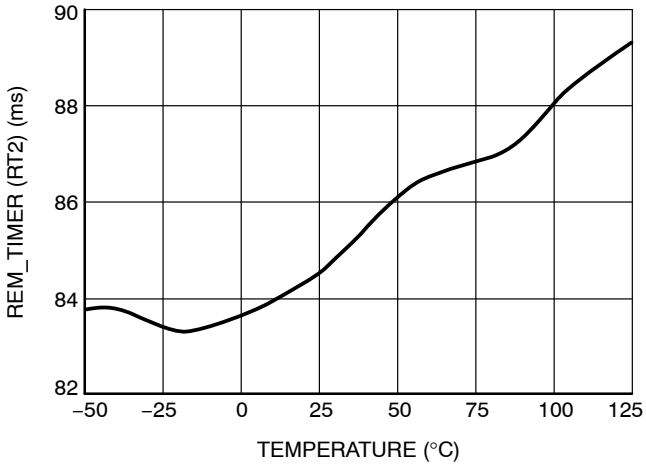


Figure 28. Remote Timer Duration, REM_timer (option RT2)

TYPICAL CHARACTERISTICS

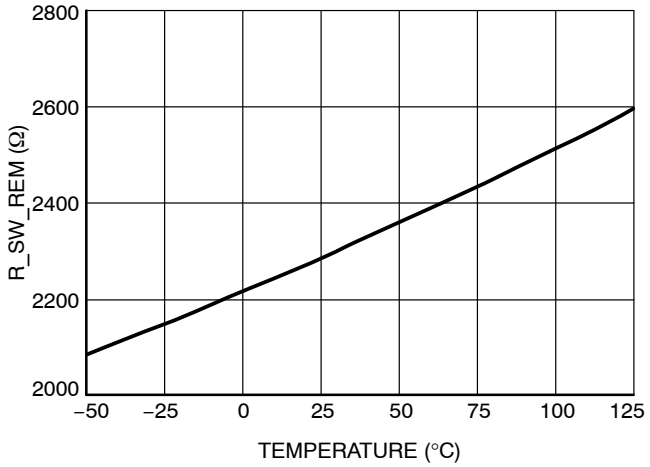


Figure 29. Internal Remote Pull Down Switch Resistance, R_SW_REM

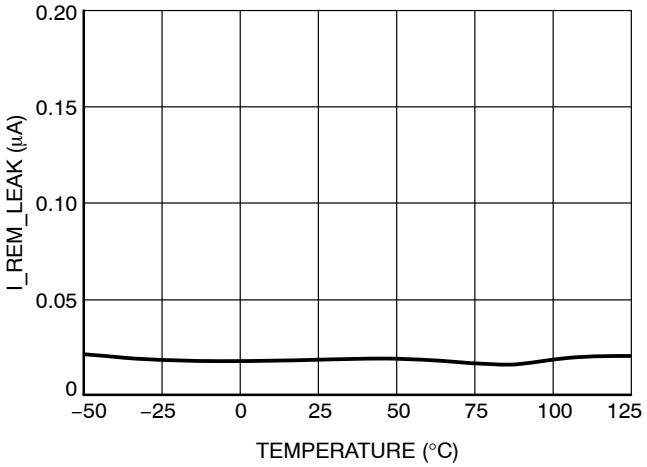


Figure 30. Remote Input Leakage Current, I_REM_leak

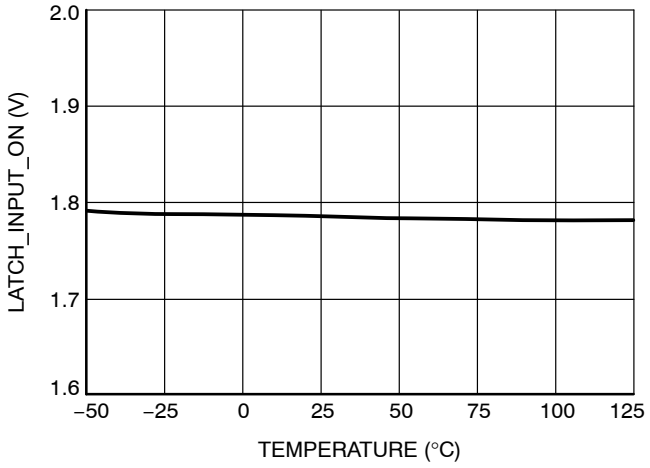


Figure 31. Voltage Level to Start Latch−off Mode, Latch_input_on

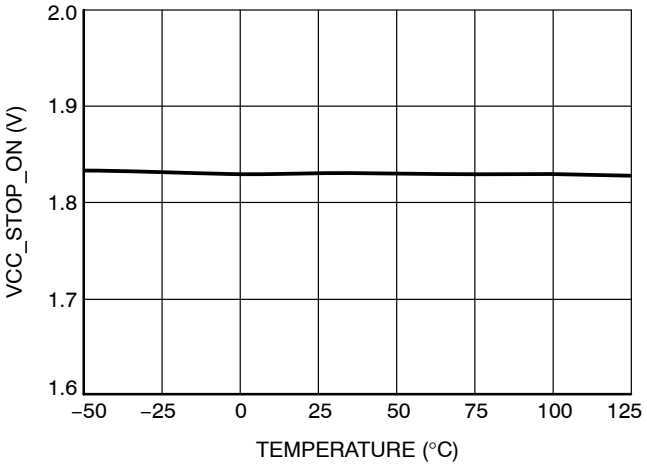


Figure 32. Voltage Level to Stop HV Current Source, VCC_stop_on

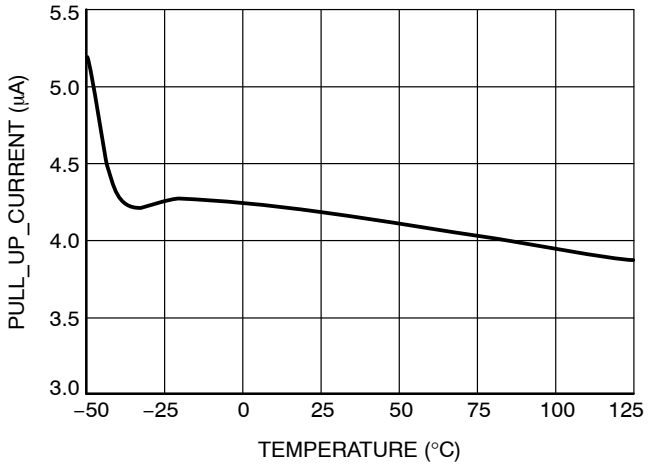


Figure 33. Pull−up Current for Open−drain Inter−bonding Signals, Pull_up_current

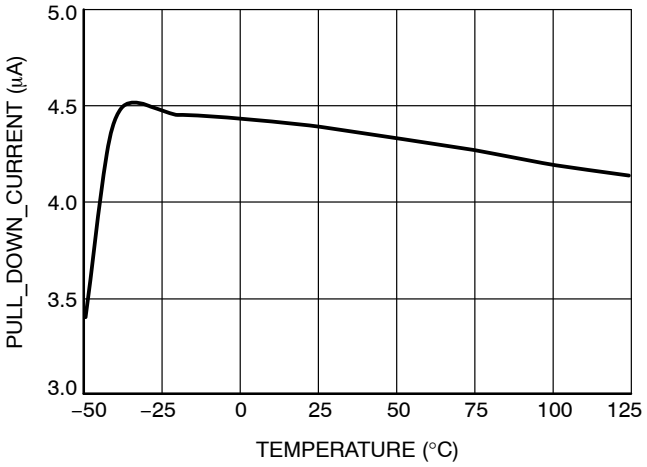


Figure 34. Pull−down Current for Logic Inter−bonding Signals, Pull_down_current

TYPICAL CHARACTERISTICS

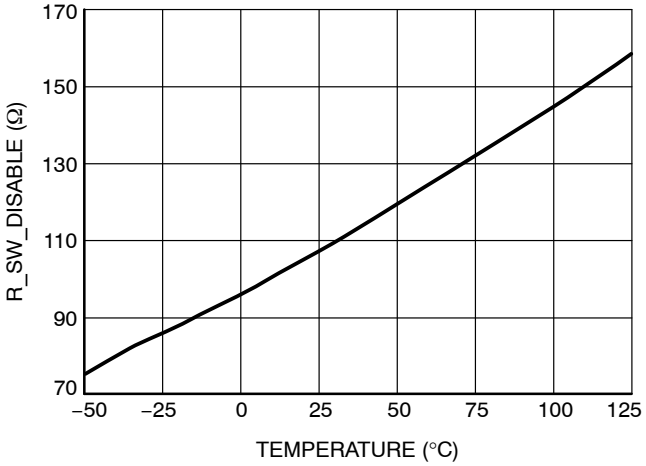


Figure 35. Internal Disable Pull Down Switch Resistance, R_SW_DISABLE

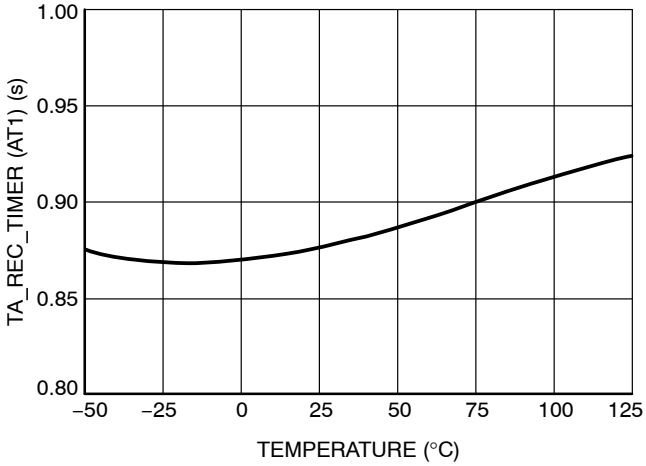


Figure 36. Auto−recovery Timer Duration, T_{A-rec_timer}

Introduction

This device is specifically designed for SMPS applications targeting ultra−low no−load power consumption. SCYW99143 DIE implements an HV startup current source with X2 discharge circuitry and Brown−out protection.

- **HV startup current source:** Reaching a low no−load standby power always represents a difficult exercise when standard resistor startup network is used. Thanks to its proprietary technology, the SCYW99143 implements HV startup current source that provides fast and reliable startup sequence while cuts−off power consumption when application operates under light load and especially no−load conditions.
- **X2 capacitor discharge circuitry:** The X2 capacitor(s) charge could result in electric shock to SMPS user if not discharged after application is unplugged from the mains. Thus, according to international standards, it is mandatory to discharge X2 capacitor(s) in given time to pass safety qualification. Built−in X2 discharger in DAP029 controller together with external X2 sensing network provides reliable and loss−less discharge function when application is unplugged under any operating conditions.
- **Internal Brown−out protection:** Brow−out (BO) protection is required in adapter applications to guarantee that the application won't be operated under too low input voltage. Internal high impedance Brow−out sensing network consumes minimum power from HV input and provides excellent noise and PCB leakage currents immunity compare to standard external BO networks composed from high resistance SMT chip resistors.
- **Auto recovery UVP on VCC:** It is sometimes interesting to implement a circuit protection by sensing the VCC level. This is what SCYW99143 provides by monitoring its VCC pin. When the voltage on this pin drops under $VCC_{(off)}$ threshold, the disable pin is immediately activated and the part enters hiccup mode. When the auto−recovery timer elapses SCYW99143 repeats start−up sequence.
- **Off−mode:** Off−mode helps to achieve low power consumption of an SMPS during no load conditions. The SCYW99143 goes into Off−mode when the REM pin is brought higher than the internal reference voltage $V_{-REM-off}$ (Active_ON version). Similarly, for active_OFF version, the SCYW99143 enters off mode operation when the REM pin is brought below reference voltage $V_{-REM-off}$. The disable input is pulled low, Vcc capacitor is discharged and consumption of all internal blocks is reduced once the off−mode is activated. Off mode is terminated when remote pin voltage crosses $V_{-REM-on}$ threshold or application is unplugged from the mains.

Brown−out Circuitry

The SCYW99143 features, on its HV pin, a true AC line monitoring circuitry – refer to Figure 37. This system includes a minimum start−up threshold and auto−recovery brown−out protection; both of them independent of the input voltage ripple. The thresholds are fixed, but they are designed to fit most of the standard AC−DC converter applications. When the HV pin voltage drops below *VBO_off* threshold for longer time than *Bo_timer*, the brown−out condition is detected and confirmed. Thus the controller stops operation – refer to Figure 38. The HV current source maintains V_{CC} at V_{CC}*_bias* level until the input voltage is back above *VBO_on*. The controller then discharges Vcc capacitor first to restart internal logic. Standard startup attempt is then placed by the controller. Refer to controller operation sequencing sections – case 2 for better understanding on how the SCYW99143 BO protection operates.

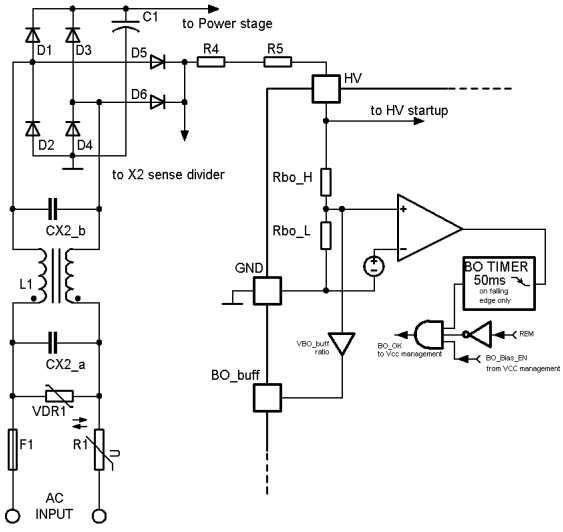


Figure 37. Simplified Block Diagram of Brown−out Detection Circuitry

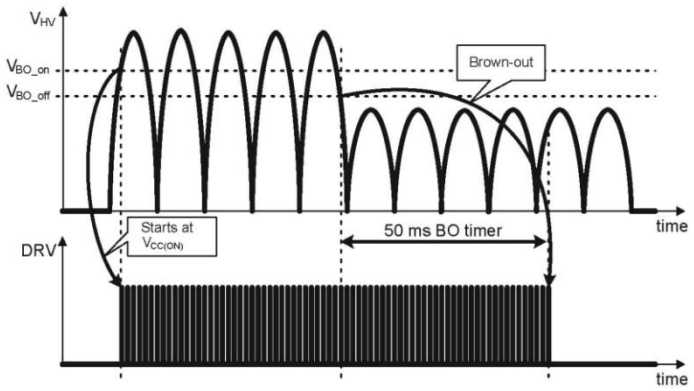


Figure 38. Brown−out Event Detection

The Internal HV BO sensing network is formed by high impedance resistor divider with minimum resistance of 20 MΩ. This solution reducing power losses during off−mode and thus helps to pass maximum standby power consumption limit. The internal BO network solution provides excellent noise and PCB leakage currents immunity that is hard to achieve when using external resistor divider built from SMT chip resistors.

The internal HV BO sensing network output is connected to the BO_buff bonding pad. This is buffered and trimmed output of the HV divider. The purpose of this pad is to be used in co−package solution with low voltage SMPS controller to provide voltage from HV pad into slave (low voltage) controller. The ratio between voltage on HV pad and voltage on BO_buff pad is defined by *VBO_buff_ratio* parameter.

X2 Discharge Circuitry

The SCYW99143 X2 discharge circuitry uses dedicated pin (X2) together with external charge pump sensing network to detect whether is application plugged into the mains or not. Advantage of this solution is that the internal IC consumption can be reduced to extremely low level by keeping all internal blocks unbiased except simple and low consuming X2 timer disable circuitry. The internal X2 timer with duration of *X2_timer* is used to overcome unwanted activation of the X2 and Vcc discharge switches in case of AC line dropout. The internal X2 and Vcc discharge switches are activated once the X2 timer elapses. The HV startup current source is enabled in the same time thus the discharge path for X2 capacitor exists – refer to Figure 39.

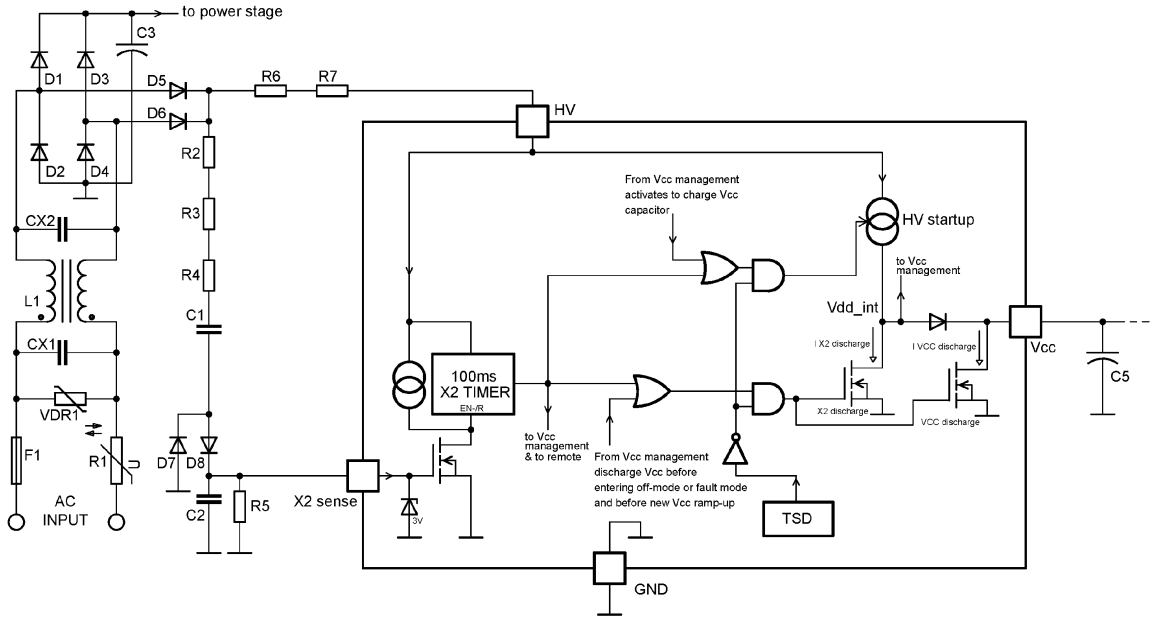


Figure 39. Simplified Block Diagram of X2 Capacitor Discharge Circuitry

The time duration of X2 capacitors discharging could be calculated by:

$$t = \frac{U_{C_{X1.2}}}{I_{\_X2\_dis}} \cdot C_{X1,2} \qquad \text{(eq. 1)}$$

The X2 capacitor discharging process can be interrupted by increasing voltage on X2 pin back above *Vth_X2*.

The over temperature protection block is active during discharging process to protect controller chip against unwanted overheat that could occur in case the X2 pin is opened and the high voltage is present on the HV pin (like during open – short pins testing for instance).

The X2 discharge switch is also activated to discharge Vcc capacitor when entering into fault mode (latch mode, auto−recovery mode or the HV pin voltage drops below *VBO_off* threshold for more than 50 ms), off−mode and also before controller Vcc restart.

Refer to controller operation sequencing section – cases 1 − 5 for better understanding on how the SCYW99143 X2 discharge circuitry works.

Remote Input

The SCYW99143 features dedicated input (Remote pin) that allows user to activate ultra low consumption mode during which the IC consumption is reduced to only very low HV pin leakage current (refer to IHV_off−mode_1 and *IHV_off_ mode_2* parameters). The off−mode is activated when remote pin voltage exceeds *V_REM_off* threshold (8 V typically for *Active_ON* version) or drops under *V_REM_off* threshold (0.4 V Typically for Active _OFF version). Normal operating mode (i.e. on−mode) is then initiated again when remote input voltage crosses back *V_REM_on* threshold (1.5 V typically *Active_ON* version and 2 V typically *Active_OFF* version) – refer to Figure 40 or Figure 41 for better understanding.

Active ON Off−mode

The off−mode with active ON logic works in such a way that the off−mode is activated when the remote input is pulled up by auxiliary remote supply (refer to Figure 40.). The normal operation mode is then activated when dedicated opto−coupler pulls the remote input down. There could occur situation, in the application, that the auxiliary remote supply stays charged while the secondary bias has been lost. The application then cannot restart until the auxiliary remote supply capacitor fully discharges. Thus the remote input hosts internal pull down switch and remote timer with duration *REM_timer*. The controller pulls down remote pin using this circuitry in order to allow correct application restart in case the auxiliary bias capacitor (C7) stays charged while the secondary side is fully discharged already. The remote timer is activated each time the application starts after these events:

- Start after application was plugged into the mains (X2 discharger signal resets remote timer latch in this case)
- Restart from fault conditions in auto−recovery versions
- Restart after Vcc has been lost while remote pin was at low state
- Restart after BO event
- Restart after OTP event

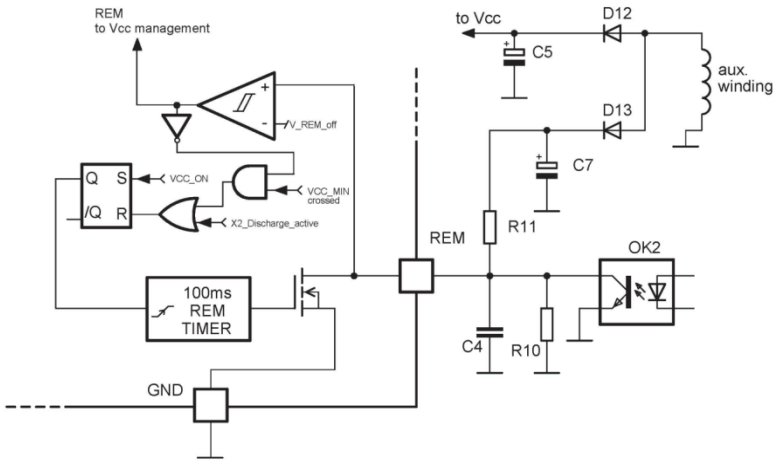


Figure 40. Simplified Block Diagram of Remote Control Input for Active ON Off−mode

The remote timer helps to assure correct application start or re−start from fault conditions by forcing controller operation for *REM_timer* duration. However, the secondary controller drives remote pin via opto−coupler during normal operating conditions in order to switch between on−mode and off−mode states. The on−mode is activated for very short time during no−load conditions – just to re−fill primary and secondary capacitors to keep application biased. The remote timer thus cannot be used in this case because it would increase no−load power consumption by forcing application on−mode operation for longer time than it is naturally needed. The remote timer with internal pull down switch is thus not activated in this case (i.e. when application restarts from off−mode operation).

Refer to controller operation sequencing section – cases 1 − 5 for better understanding on how the SCYW99143 remote circuitry works.

Active OFF Off−mode

The remote input is designed for direct connection to FB pin of a flyback controller. The voltage on remote pin follows FB pin voltage except during off−mode.

The FB pin is not biased in off−mode because Vcc is disabled by SCYW99143. The internal current source of (2.5 μA typically) then pulls−up the remote when FB optocoupler instructs the primary side to restart normal operation. The feedback pin of the flyback controller thus has to feature protection against reverse current from FB to Vcc pins. The easiest way how to overcome this reverse current is to use a diode in FB pin. Connection between remote and FB pins with simplified block diagram of remote control input are shown in Figure 41.

The off mode is activated when the remote pin is low and Vcc _off threshold is crossed i.e. when the skip mode takes so long time that Vcc is lost. Vcc capacitor is then discharged by internal consumption of the SCYW99143 and consumption of slave SMPS controller in skip mode. Maximum skip mode duration before the SCYW99143 enters off−mode is thus given by value of Vcc capacitor, total consumption during skip mode and voltage level on Vcc capacitor in the time when flyback controller enters skip mode.

The remote pin information is ignored in the case the FB pin is pulled down by SCYW99143 itself (i.e. like during BO event or Vcc fault cases) – refer to next paragraph “Disable input”.

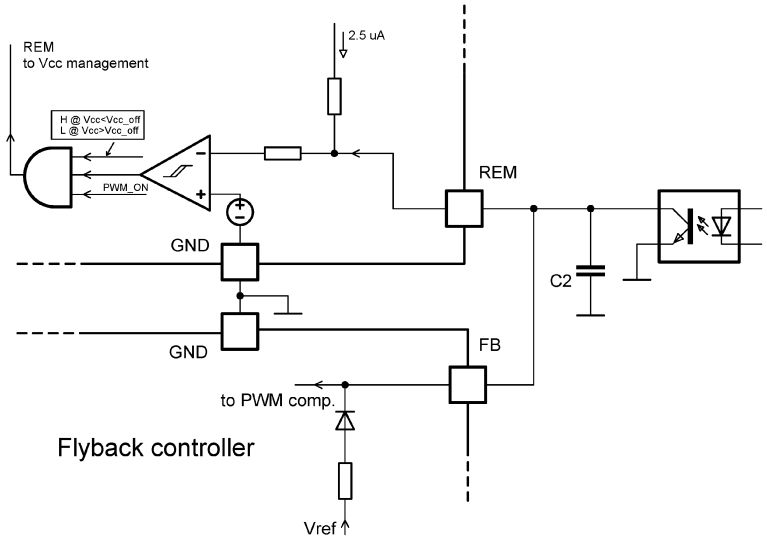


Figure 41. Simplified Block Diagram of Remote Control Input for Active OFF Off−mode

Refer to controller operation sequencing section – cases 1 – 5 for better understanding on how the SCYW99143 remote circuitry works.

Disable Switch Output

The SCYW99143 features internal open drain MOSFET switch that is connected to the disable pin/pad. This pad can be used to pull down FB pin of the slave SMPS controller in order to stop its operation immediately by activating skip mode. More specifically – this function is used for fast disabling of SMPS controller driver in these cases: remote mode (only Active ON option), auto−recovery mode, latch−off mode, after X2 discharge condition is confirmed, BO event and during every new start−up sequence. All these cases can be represent by one “/PWM_ON” signal (refer to Figure 42).

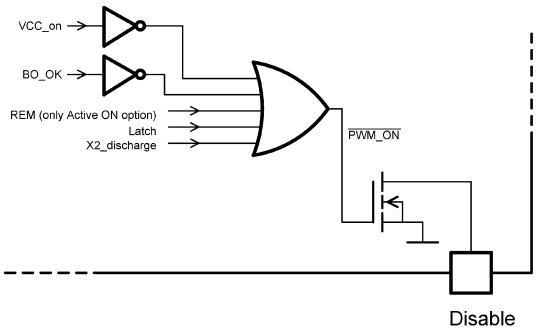


Figure 42. Simplified Block Diagram of Disable Switch Output

Auto−recovery UVP on VCC

The controller activates auto−recovery timer with duration T_{A-rec_timer} in case the Vcc drops below *Vcc_off* level. The Vcc capacitor is discharged down to *Vcc_bias* level when auto−recovery timer starts counting. The Vcc is maintained at *Vcc_bias* level (5 V) during this operation to keep the timer and other internal circuitry running.

The Vcc capacitor is fully discharged by X2 discharge switch before controller tries for restart from fault condition.

The restart from fault condition occurs when auto−recovery timer elapses or if Vcc is forced below 4 V externally.

Internal Communication between Two Controllers at Co−package Option

Co−package option can bring some benefits. SCYW99143 can obtain information about *VCC_on* of slave controller, and information about slave controller transition to Latch−off mode.

VCC_ON Detection

The SCYW99143 features *VCC_stop* bonding pad/input that can be used to terminate startup current source operation prior the regular Vcc_on threshold (22 V typically) is reached. This feature reduces startup time in case the slave SMPS controller provides *VCC_stop* signal based on its own Vcc_on threshold (like 18 V in NCP1250 case). Difference between start up sequences with and without *VCC_stop* bonding interconnection can be seen in Figure 43. Vcc_stop comparator is enabled only during start−up sequence − i.e. Vcc capacitor is charged from Vcc_off level to Vcc_on level.

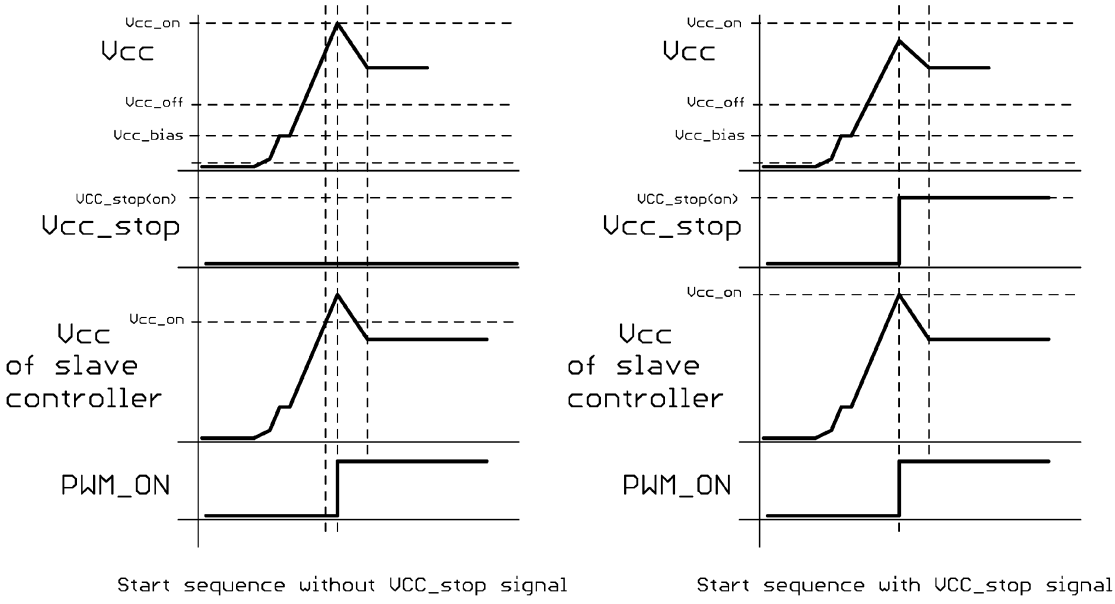


Figure 43. Start−up Sequence Without and With VCC_start Signal Interconnection

LATCH Detection

The SCYW99143 latch pad can be used to latch the HV startup block off in case of serious fail in SMPS. The internal latch signal from slave SMPS controller has to be provided to SCYW99143 in case of co−packaged solution. When the slave controller Latches−off without inter−bonding Latch information, the SCYW99143 detects only that Vcc was lost because of missing driver pulses i.e. no power from auxiliary winding. The SCYW99143 goes then into auto−recovery mode and restarts operation after T_{A-rec_timer} by a new start−up sequence refer to Figure 49. If the slave controller latches−off and inter−bonding Latch information is provided, the SCYW99143 goes into latch−off mode refer to Figure 50. Latch−off mode continues until the mains is unplugged − the X2 discharge is confirmed and activated or Vcc is forced below 4 V externally. The inter−bonding Latch signal does not have to be present for the time the controller is latched − the SCYW99143 internal logic triggers on rise edge of this signal only. More details are showed on Figure 44. Latch comparator is enabled only during regular operation − i.e. when Vcc level is between Vcc_on and Vcc_off levels.

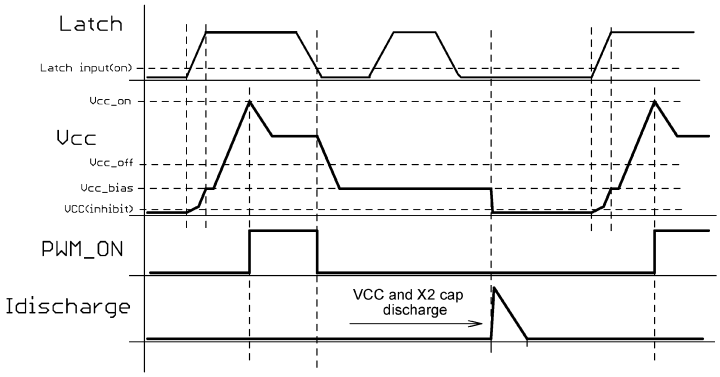


Figure 44. Internal Latch Signal Communication

Bonding Diagram

The bonding diagram of SCYW99143 can be seen in Figure 45. Pads 1, 2, 3, 5 and 7 can be swapped each other (using different metal masks options) to allow co−package with many SMSP controllers with different pinout. Disable switch output could be connected only on pads 3 and 4. Pads 6, 8, and 10, are fixed and cannot be swapped!

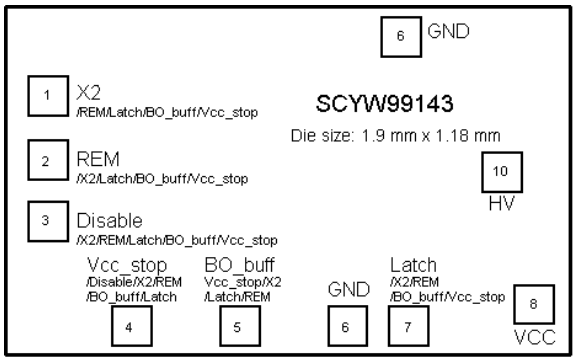


Figure 45. Bonding Diagram for Co−package Option

TSD Protection

The SCYW99143 includes a temperature shutdown protection. When the temperature rises above the high threshold during stable operation − i.e. start−up sequence is ended and Vcc is between *Vcc_on* and *Vcc_off* levels, the controller immediately actives disable switch to stop slave controller. After the temperature falls back below the lower threshold, the Vcc capacitor is fully discharged by Vcc discharge switch to restart both − SCYW99143 and slave controllers.

The TSD protection can be activated at some other cases (charging Vcc capacitor − start−up sequence and discharging X2 or Vcc capacitors). The TSD protection only interrupts current operating sequence − i.e. the operation sequence continue after the temperature falls back below the low threshold. The SCYW99143 is not reset by TSD activation in these cases.

Controller Operation Sequencing

Below paragraphs describe controller operation sequencing under several typical cases for Active ON and Active Off version that can occur in the application as well as transitions between them. Refer also to the detail status diagrams for the off−mode versions (Figure 56 and Figure 57).

Active ON Version

1. *Application start, remote off/on then AC line off − Figure 46:*

Application has been plugged into the mains at point **A**. The HV pin receives rectified AC line voltage and the X2 sense pin charges up via external charge pump sensing circuitry. As the high voltage is present on the HV pin the startup current source is activated to charge Vcc capacitor to *VCC_bias*. The BO block bias is enabled at this point (point **B**). The *Vcc_bias* is maintained until the controller receives BO−OK information from the BO block. When line voltage is high enough to enable application operation the startup current source continues to ramp up the Vcc voltage (point **C**) up to *Vcc_on* threshold (point **D**) where PWM block operation is enabled (PWM_ON signal). The remote timer and internal remote pin pull down switch are activated in the same time (point **E**) to mask the external remote pin information and thus assure the application start even if the remote pin bias remains from previous operation. The remote opto−coupler is then activated by secondary side controller to keep converter standard operation under any load conditions (e.g. standard PWM operation, frequency foldback or skip mode).

The remote opto−coupler has been turned−off by the secondary controller at point **F** to activate the off−mode operation. The voltage on remote pin thus grows above *V_REM_off* threshold. Controller stops PWM operation immediately by pulling down the FB pin via internal switch. The Vcc capacitor is then internally discharged to 5 V and all blocks are disabled to reduce IC consumption to minimum needed level. The Vcc pin remains unbiased during whole off−mode operation. The X2 discharge and remote internal blocks remain biased by the HV leakage current *Istart_off* (HV current source is OFF) − consuming minimum power but still keeping them operated.

The remote opto−coupler has been turned−on by the secondary controller at point **G** to activate normal operation

mode. The voltage on remote pin thus drops fast below *V_REM_on* threshold. Vcc is fully discharged and the controller enables the HV startup current source to built Vcc bias up again. The BO block bias is enabled at point **H**. This *Vcc_bias* level (5 V) is maintained until the controller receives BO_OK information from the BO block. If the line voltage is high enough to enable operation the startup current source continues to ramp up Vcc voltage (point **I**) up to *Vcc_on* threshold (point **J**) where controller PWM is enabled (PWM_ON signal). The remote timer is now not activated like during first start because there was line voltage present all the time during off−mode operation (the remote timer latch is reset by X2 discharge signal). Application then operates normally under any load conditions (e.g. standard PWM operation, frequency foldback or skip mode).

Application has been unplugged from the mains at point **K**. Let us consider the light load operation mode during this event as a worst case for X2 capacitor discharging process. The X2 capacitor stays charged on its actual voltage level (line peak voltage in worst case). The X2 capacitor provides DC bias to HV pin. The X2 sense input voltage starts to drop in the same time because there is no AC voltage and charge pump cannot transfer any charge to X2 pin. The 100 ms X2 timer is activated when the X2 input voltage drops below internal X2 timer disable switch threshold voltage (*Vth_X2*) point **L**. After the X2 timer elapses (point **M**), the PWM block operation is disabled by pulling down the FB pin via internal FB switch and the discharge switches (X2 and VCC) are activated and X2 capacitor discharges via HV startup current source until the X2 capacitor voltage drops to safe level and internal bias is lost. The over temperature protection is active during discharging process to overcome HV startup damage that would occur otherwise under fault cases – like when X2 pin is not connected.

2. *Application start, AC line dropout, low line off, BO restart, AC line off – Figure 47:*

Application operation from point **A** to point **F** is the same like in 1st case described above. The line dropout occurs at point **F**. BO timer starts to count down and X2 pin voltage drops below threshold voltage of internal X2 disable switch – thus also X2 timer is initiated. The line however recovers before the BO and X2 timer periods elapsed and Vcc has been lost. Application operation is thus is not interrupted. The energy for power stage operation is provided by bulk capacitor during dropout period in this case. The line voltage drops below *V_BO_off* threshold at point **G**. The BO timer is initiated and elapses after 50 ms thus the PWM block operation is disabled by pulling down the FB pin via internal FB switch. The Vcc capacitor is discharged by Vcc discharge switch to *Vcc_bias* level. The Vcc is then maintained at *VCC_bias* level by HV startup current source to keep BO block operation (VHV > 60 V).

The line voltage increases above *V_BO_on* threshold at point **I**. The BO_OK signal is received (point **J**) and internal Vcc discharge switch is activated to fully discharge Vcc capacitor and thus restart whole circuit. The HV startup current source is activated after discharge and ramps−up the Vcc voltage to *Vcc_bias* (5 V) level. The BO block is activated at point **K** and correct line voltage is confirmed at point **L** thus the HV startup current source continues to ramp−up the Vcc voltage up to Vcc_on threshold where is the PWM block operation enabled (point **M**). The remote pin is pulled down by internal switch to assure correct application restart even if the external bias remains on the remote pin. Application then operates normally under any load conditions (e.g. standard PWM operation, frequency foldback or skip mode).

User unplugged power supply from the mains at point **N**. The X2 discharge process takes place after 100 ms similarly as in case 1.

3. *Off−mode operation – restart by primary remote discharge then AC line off – Figure 48:*

The secondary controller turns−off the remote opto−coupler and off−mode is initiated at point **A**. The auxiliary voltage on remote input discharges very slowly during off−mode. If the off−mode is active for too long time the remote pin bias voltage will disappear. Thus the remote pin voltage crosses *V_REM_on* threshold at point **B**. Vcc capacitor is fully discharged and the HV startup current source is activated to build Vcc bias for BO block (point **C**). Once the BO_OK information is received (point **D**) the HV startup current source ramps up to *Vcc_on* level (point **E**). PWM block operation is enabled and remote pin bias voltage thus grows. The PWM block is disabled via FB pin, Vcc capacitor is internally discharged to 5 V and application enters off−mode again when remote pin voltage crosses *V_REM_off* threshold (point **F**). This operation mode is called automatic primary restart during off−mode. Restart occurs because remote pin bias is lost.

User unplugged application from the mains at point **G**. The application was operating in off−mode at that time. The X2 pin voltage drops because charge pump does not operate and X2 timer disable switch is opened at point **H** (X2 timer start counting). The X2 and Vcc dischargers are activated after X2 timer elapses (point **I**).

4. *Application start into short circuit, auto−recovery restart, overloads then AC line off – Figure 49:*

Application operation from point **A** to point **E** is the same like in 1st case described in paragraph 1. However, the short circuit is present at the converter output during startup sequence thus the Vcc voltage is not maintained and *Vcc_off* threshold is reached in point **F**. The PWM block is disabled via FB pin and 1 s auto−recovery timer is activated. The Vcc capacitor is discharged by Vcc discharge switch to *Vcc_bias* level where it is maintained by the HV startup current source. This Vcc bias provides powers to all needed blocks including auto−recovery timer.

The auto−recovery timer elapses at point **G** and controller places new restart by fully discharging Vcc capacitor and then enabling HV startup current source to ramp up Vcc voltage again. The BO block is enabled at point **H** as Vcc bias is available. The BO_OK information is received at

point **I** and startup current source is enabled again to charge Vcc capacitor up − to *Vcc_on* level. The PWM block is enabled at point **J** together with remote pull down switch and timer (point **K**). Application then operates regularly in PWM mode.

An overload condition occurs on the output in point **L**. The slave controller fault timer counts down the 100 ms period (fault timer duration is parameter of slave controller) before it disables PWM block internally (point **M**). The Vcc collapses due to controller consumption and passes *Vcc_off* threshold where 1 s auto−recovery timer is activated and PWM_ON signal is deactivated (point **N**). The Vcc is again maintained at *Vcc_bias* level when auto−recovery timer counts down the off− time. Application is suddenly unplugged from the mains (point **O**) before the auto−recovery timer elapses. The X2 timer is activated after X2 pin voltage drops (point **P**). The controller does not allow new attempt for restart when X2 timer is counting even the auto−recovery timer elapses. The X2 capacitor is then discharged after X2 timer elapses (point **Q**).

Note that auto−recovery timer is starter after *Vcc_off* threshold is reached AND remote pin is at low level – i.e. application felt into fault during PWM block operation. The remote input is ignored and new restart is placed after auto−recovery timer elapses.

5. *Application start, latch−off after 120 ms, AC line restart – Figure 50:*

Application operation from point **A** to point **E** is the same like in 1st case described in paragraph 1. The controller however latches−off approximately 120 ms after startup in this case – point **F**. Controller can be latched by various mechanisms – refer below to descriptions. The PWM block is disabled internally after latch has been asserted. The Vcc capacitor is discharged by Vcc discharge switch to *Vcc_bias* level. The *Vcc_bias* (5 V) is then maintained by HV startup current source to keep controller in latched state.

The user recognized that SMPS is not working and tries to restart it by re−plugging into the mains. Thus the application is unplugged at point **G**. The X2 discharge timer is activated via X2 pin (point **H**). The X2 capacitor is discharged and all Vcc is lost after X2 timer elapses (point **I**). The internal logic is thus reset and prepared for next start attempt.

User plugs application into the mains again at point **J**. Standard startup sequence occurs (including remote pull down switch and timer activation). Application then operates in normal operating modes (e.g. standard PWM operation, frequency foldback or skip mode).

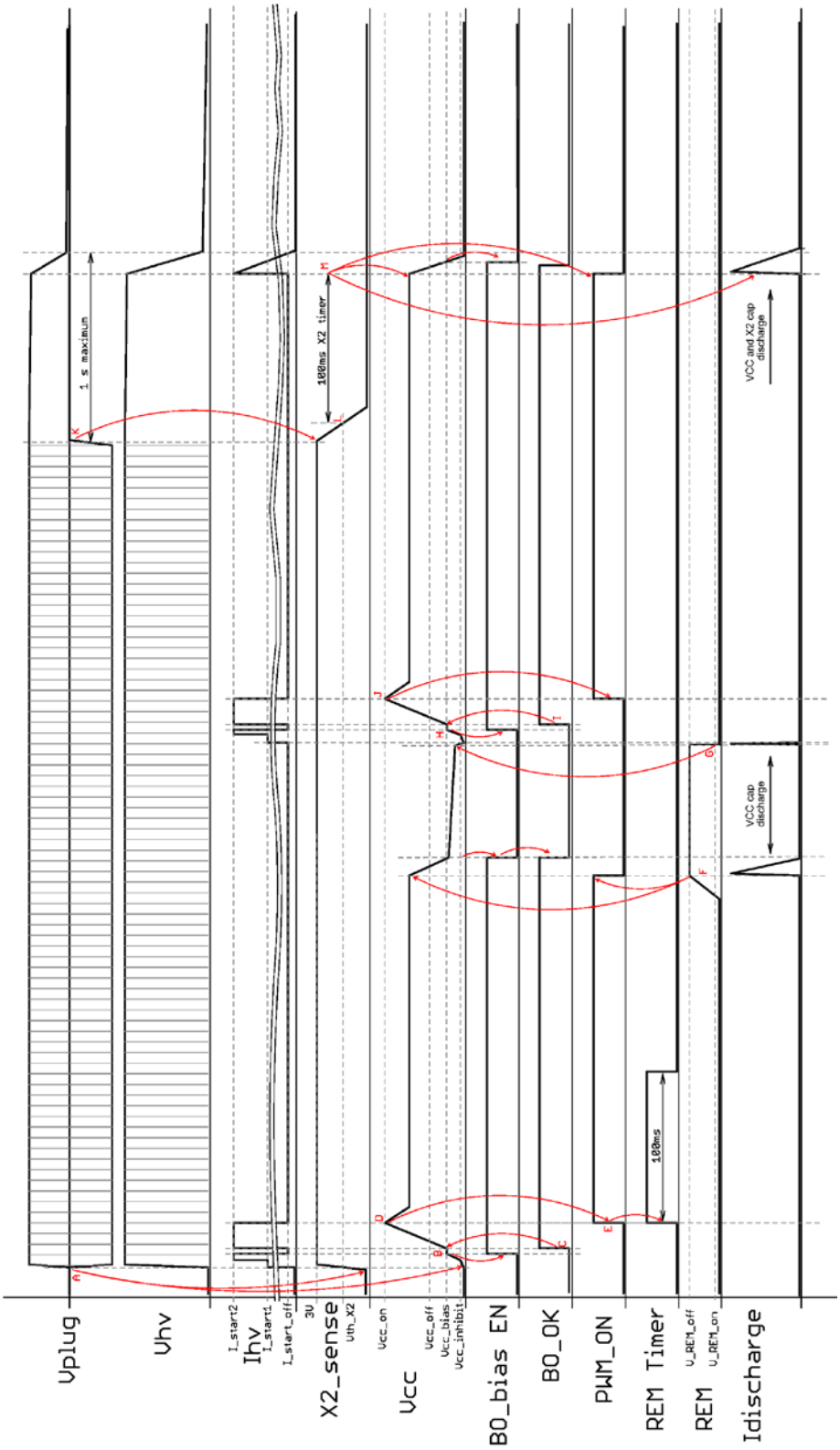


Figure 46. IC Operation Sequencing – Case 1 (Active ON)

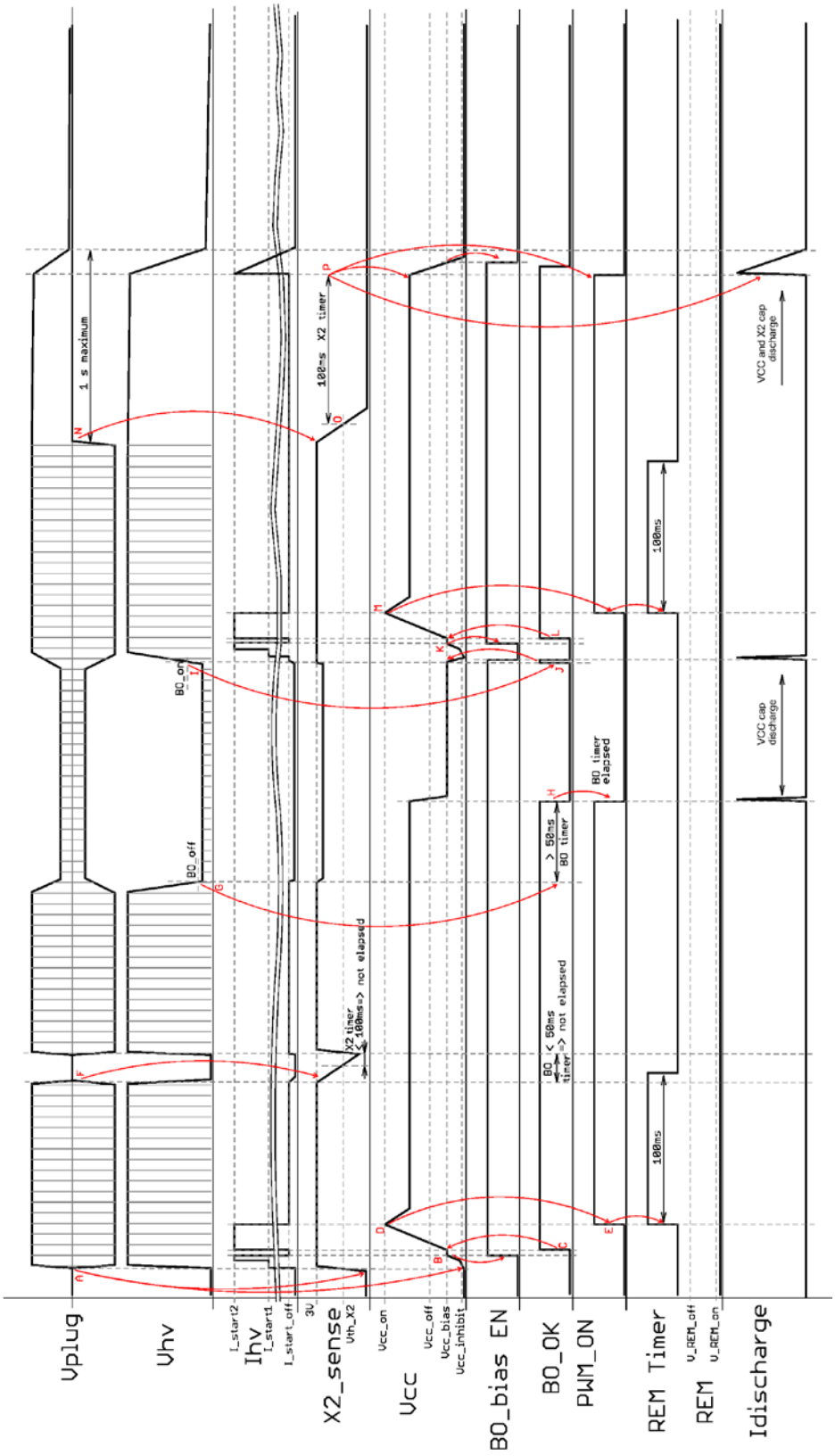


Figure 47. IC Operation Sequencing – Case 2 (Active ON)

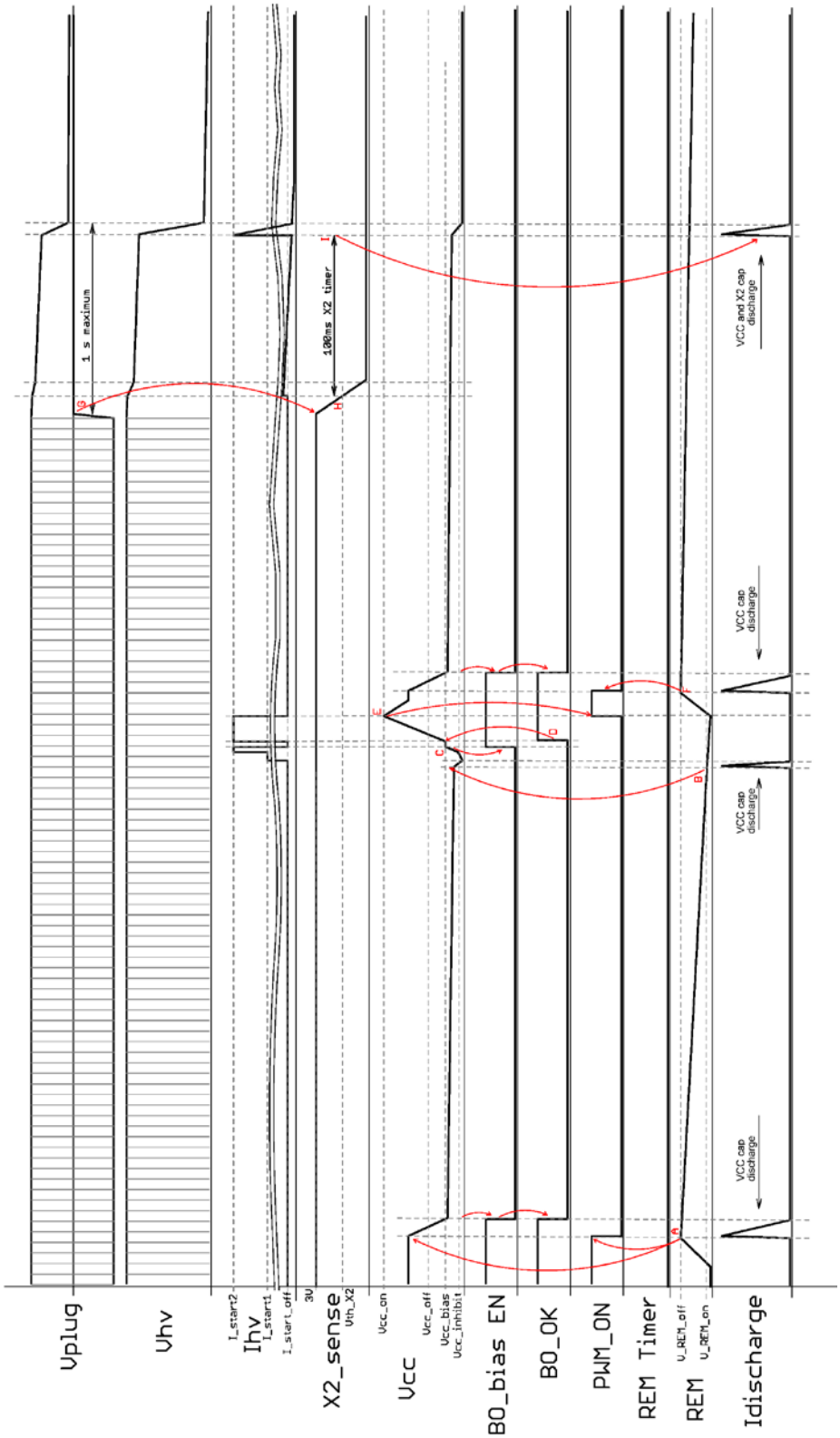


Figure 48. IC Operation Sequencing – Case 3 (Active ON)

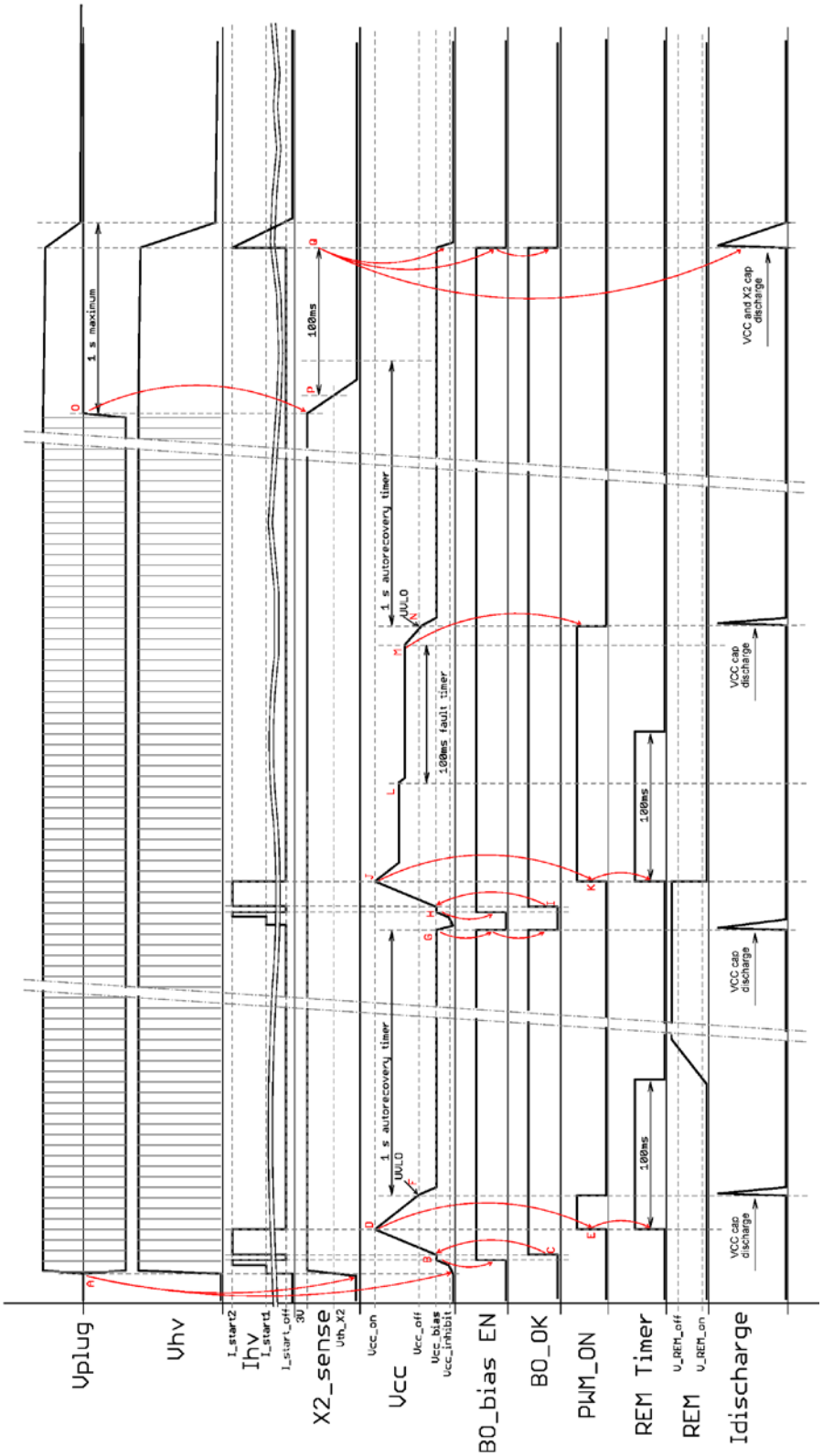


Figure 49. IC Operation Sequencing – Case 4 (Active ON)

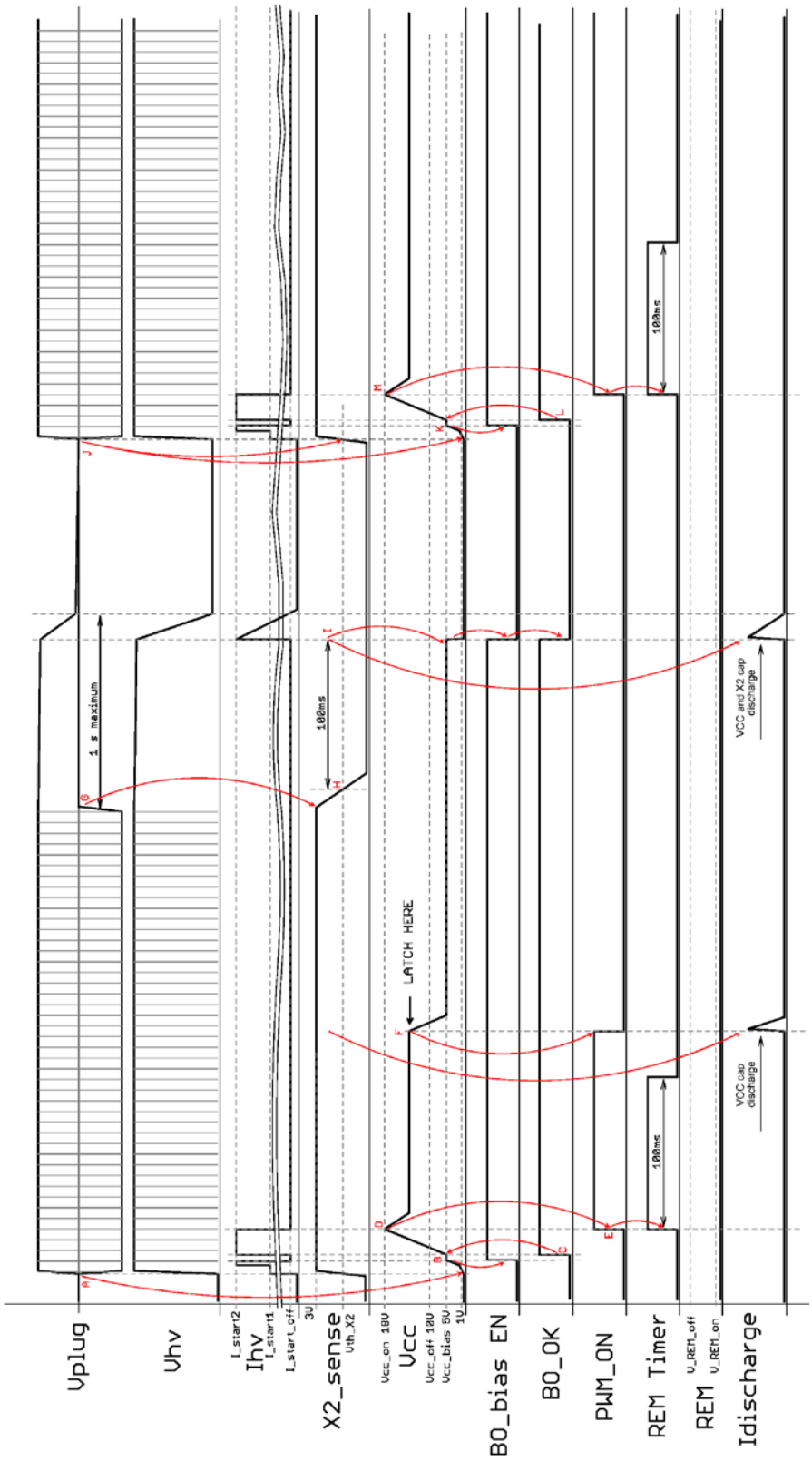


Figure 50. IC Operation Sequencing – Case 5 (Active ON)

Active OFF Version

1. *Application start, remote off/on then AC line off – Figure 51:*

Application has been plugged into the mains at point **A**. The HV pin receives rectified AC line voltage and the X2 sense pin charges up via external charge pump sensing circuitry. As the high voltage is present on the HV pin the startup current source is activated to charge Vcc capacitor to *VCC_bias*. The BO block bias is enabled at this point (point **B**). The *Vcc_bias* is maintained until the controller receives BO−OK information from the BO block. When line voltage is high enough to enable application operation the startup current source continues to ramp up the Vcc voltage (point **C**) up to *Vcc_on* threshold (point **D**) where PWM block operation is enabled (PWM_ON signal). The voltage on REM pin follows voltage on FB pin of slave controller (i.e. REM pin is connected directly to FB opto−coupler).

The voltage on REM falls under *VREM_off*. It is mean slave controller goes into skip mode. If the skip mode takes too long time, Vcc crosses *Vcc_off* level due to internal consumption (voltage on REM pin is still below *VREM_off*), then the off−mode is detected (point **E**). The Vcc capacitor is then internally discharged to 5V and all blocks are disabled to reduce IC consumption to minimum needed level. The Vcc pin remains unbiased during whole off−mode operation. The X2 discharge and remote internal blocks remain biased by the HV leakage current *Istart_off* (HV current source is OFF) − consuming minimum power but still keeping them operated.

FB opto−coupler is turned off and the voltage on REM pin is slowly increased by internal pull−up current source *I_REM_bias*. When the voltage on REM pin exceed *V_REM_on* threshold at point **F**, Vcc capacitor is fully discharged and the controller enables the HV startup current source to built Vcc bias up again. The BO block bias is enabled and PWM_ON signal is disabled at point **G**. This *Vcc_bias* level (5 V) is maintained until the controller receives BO_OK information from the BO block. If the line voltage is high enough to enable operation the startup current source continues to ramp up Vcc voltage (point **H**) up to *Vcc_on* threshold (point **I**) where controller PWM is enabled (PWM_ON signal). Application then operates normally under any load conditions (e.g. standard PWM operation, frequency foldback or skip mode).

Application has been unplugged from the mains at point **J**. Let us consider the light load operation mode during this event as a worst case for X2 capacitor discharging process. The X2 capacitor stays charged on its actual voltage level (line peak voltage in worst case). The X2 capacitor provides DC bias to HV pin. The X2 sense input voltage starts to drop in the same time because there is no AC voltage and charge pump cannot transfer any charge to X2 pin. The 100 ms X2 timer is activated when the X2 input voltage drops below internal X2 timer disable switch threshold voltage (*Vth_X2*) point **K**. After the X2 timer elapses (point **L**), the PWM block operation is disabled by pulling down the FB pin via internal FB switch, the discharge switches (X2 and VCC) are activated and X2 capacitor discharges via HV startup current source until the X2 capacitor voltage drops to safe level and internal bias is lost (point **M**). The over temperature protection is active during discharging process to overcome HV startup damage that would occur otherwise under fault cases – like when X2 pin is not connected.

2. *Application start, AC line dropout, low line off, BO restart, AC line off – Figure 52:*

This case is the same as for Active ON version except levels of voltage on REM pin. The voltage on REM pin follows voltage on FB pin of the slave controller

3. *Off−mode operation – restart by primary remote pull−up then AC line off – Figure 53:*

The voltage on REM falls under *VREM_off*. The slave controller goes to skip mode for long time. Vcc crosses *Vcc_off* level due to internal consumption (voltage on REM pin is still below *VREM_off*) and off−mode is initiated (point **A**). As soon as the FB opto−coupler is turned off, the voltage on REM pin is slowly increased by internal pull−up current source *I_REM_bias*. When the voltage on REM pin exceed *V_REM_on* threshold at point **B**, Vcc capacitor is fully discharged and the controller enables the HV startup current source to built Vcc bias for BO block and PWM_ON signal is disabled (point **C**). Once the BO_OK information is received (point **D**) the HV startup current source ramps up to *Vcc_on* level (point **E**). PWM block operation is enabled and the voltage on REM pin is decreasing by turning on of FB opto−coupler. The application enters into off−mode again when remote pin voltage crosses *V_REM_off* threshold and Vcc falls under *VCC_off* (point **F**). Restart occurs because REM pin is biased when FB opto−coupler is turned off.

User unplugged application from the mains at point **G**. The application was operating in off−mode at that time. The X2 pin voltage drops because charge pump does not operate and X2 timer disable switch is opened at point **H** (X2 timer start counting). The X2 discharger is activated after X2 timer elapses (point **I**).

4. *Application start into short circuit, auto−recovery restart, overloads then AC line off – Figure 54:*

This case is the same as for Active ON version except levels of voltage on REM pin. The voltage on REM pin follows voltage on FB pin of the slave controller.

5. *Application start, latch−off after 120 ms, AC line restart – Figure 55:*

This case is the same as for Active ON version except levels of voltage on REM pin. The voltage on REM pin follows voltage on FB pin of the slave controller.

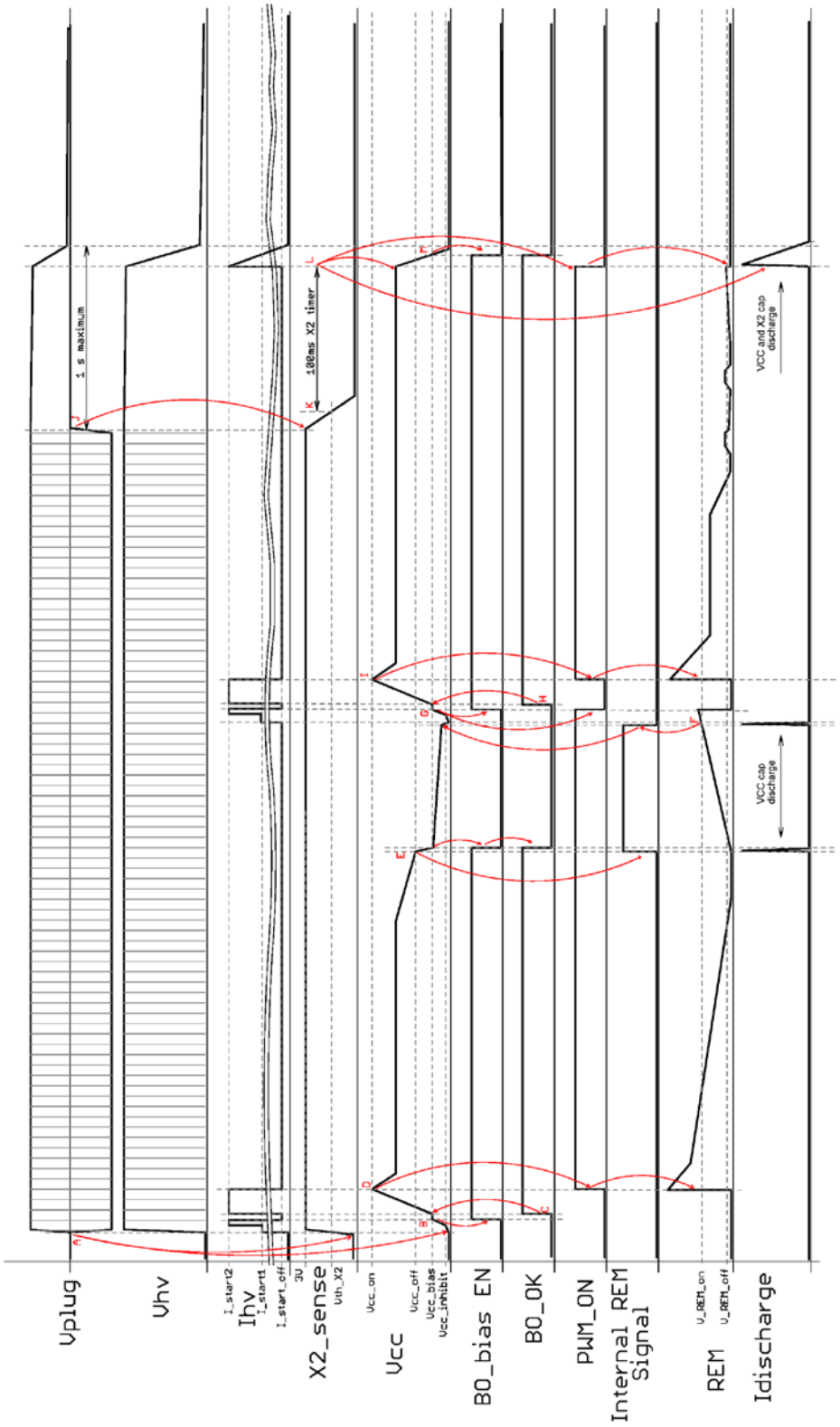


Figure 51. IC Operation Sequencing – Case 1 (Active OFF)

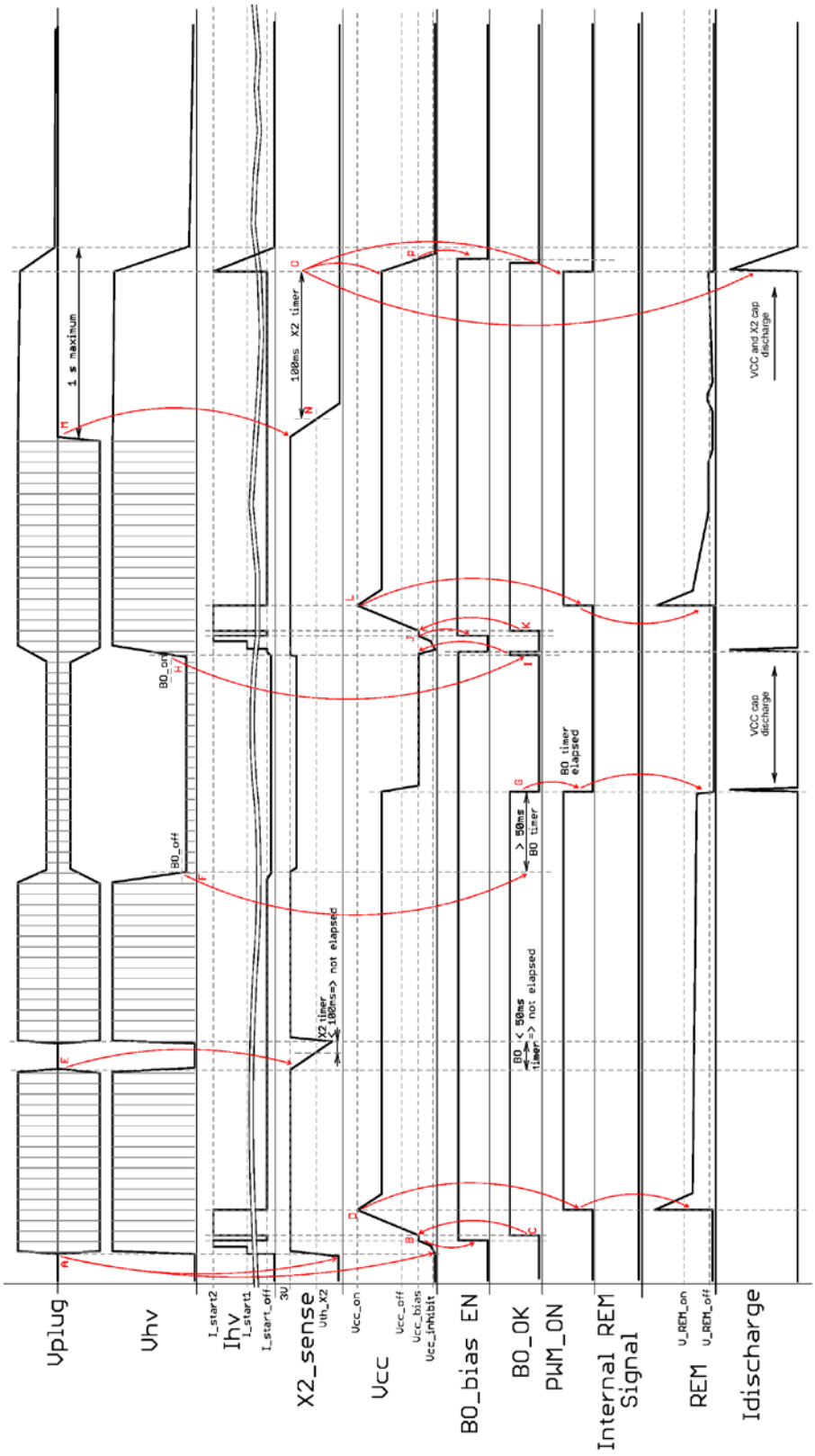


Figure 52. IC Operation Sequencing – Case 2 (Active OFF)

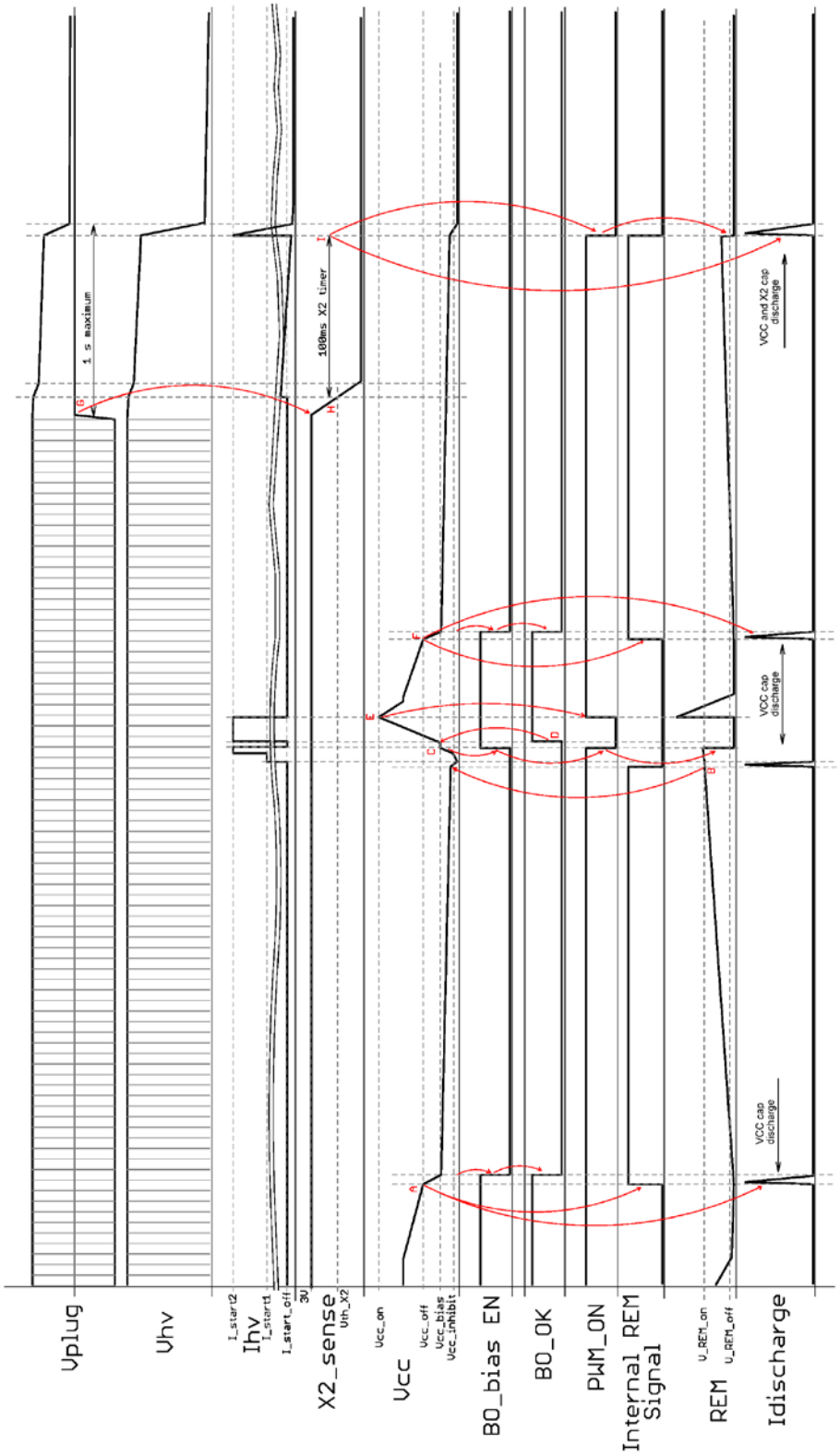


Figure 53. IC Operation Sequencing – Case 3 (Active OFF)

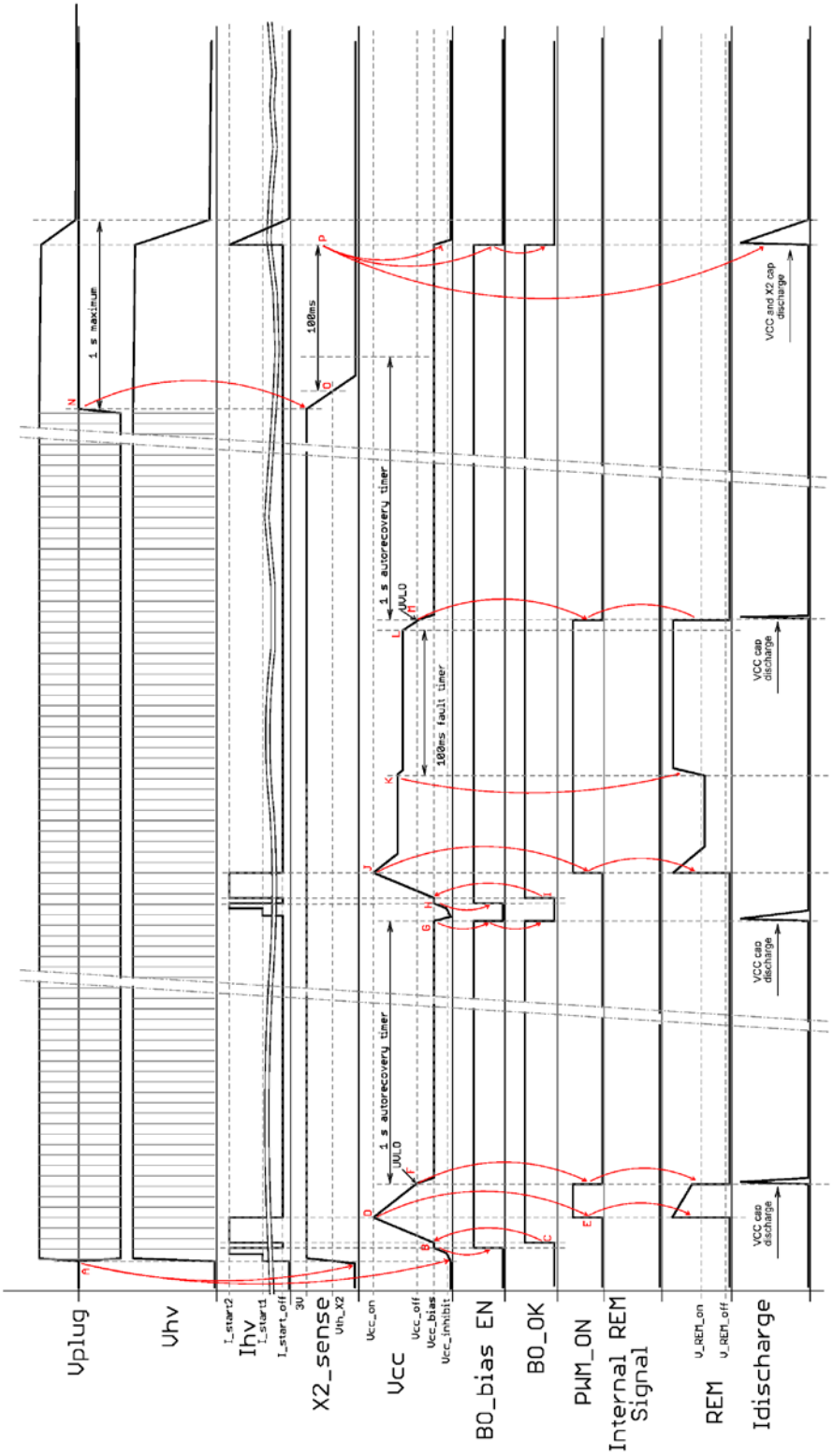


Figure 54. IC Operation Sequencing – Case 4 (Active OFF)

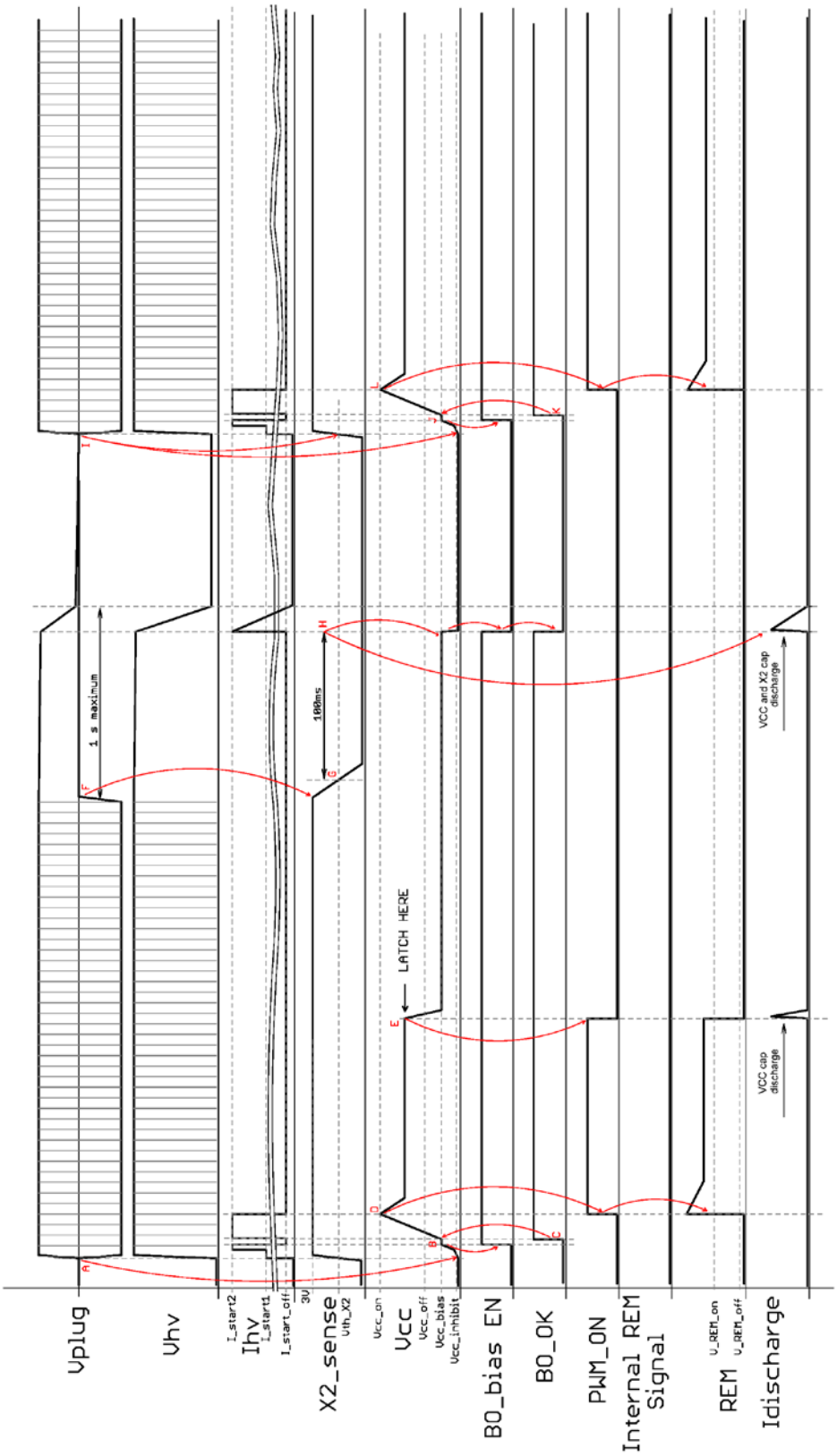


Figure 55. IC Operation Sequencing – Case 5 (Active OFF)

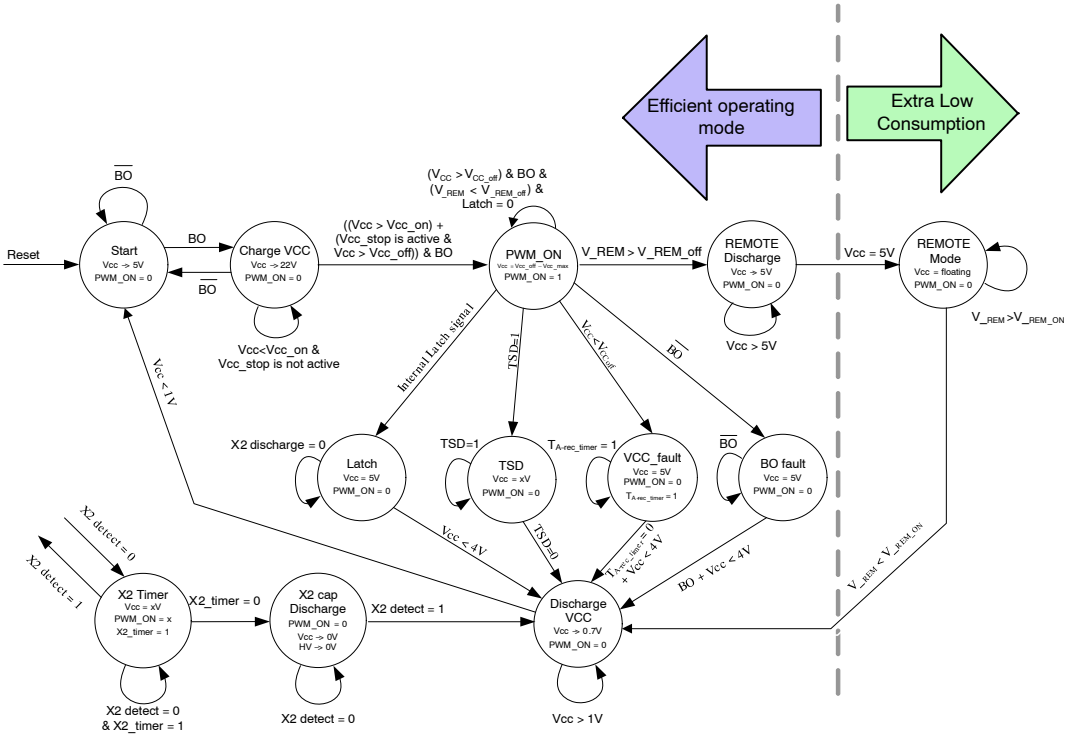


Figure 56. Operating Status Diagram for the Active ON Version

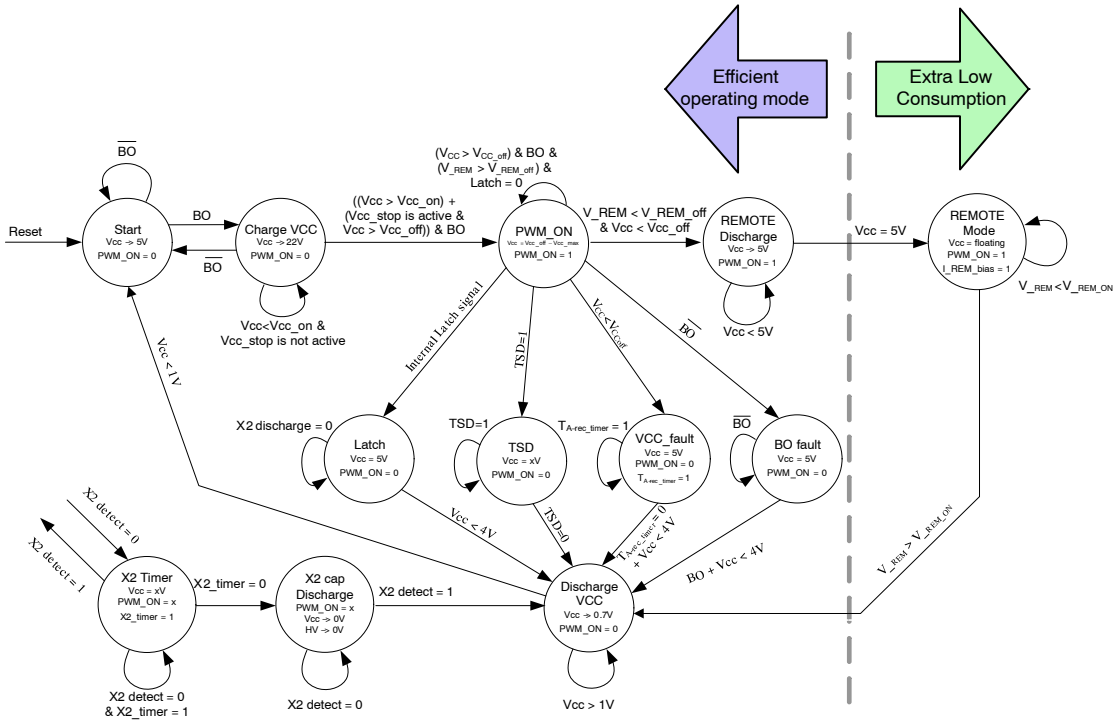


Figure 57. Operating Status Diagram for the Active OFF Version

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