Universal Semiconductor

SD210, SD211, SD212
SD213, SD214, SD215

N-Channel Enhancement-Mode Lateral D-MOS FETs

Ordering Information

Description	Gate Protective Diode			No Gate Protective Diode		
	30V, 45Ω	10V, 45Ω	20V, 45Ω	30V, 45Ω	10V, 45Ω	20V, 45Ω
TO-72 Pkg, w/o Shorting Rings	SD211DE	SD213DE	SD215DE	SD210DE	SD212DE	SD214DE
TO-72 Pkg, Shorting Rings	SD211DE/R	SD213DE/R	SD215DE/R	SD210DE/R	SD212DE/R	SD214DE/R
Gold-Backed Chips in Waffle Pack	SD211CHP	SD213CHP	SD215CHP	SD210CHP	SD212CHP	SD214CHP

Features:

- Self-Aligning Silicon Gate Structure
- Low Transfer Capacitance — 0.2 pF typ.
- Low Input Capacitance — 2.4 pF typ.
- Low Output Capacitance — 1.3 pF typ.
- Low Gate Threshold Voltage — 0.6V typ.

Applications:

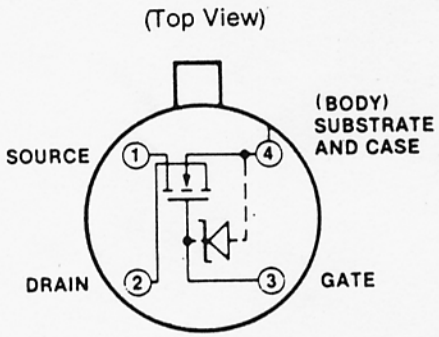
- ±15V Switch Drivers — SD210, SD211
- ±10V Analog Switches — SD214, SD215
- ±5V Analog Switches — SD212, SD213
- Sample and Hold
- Track and Hold
- Video Switches

Absolute Maximum Ratings (T_A = +25°C unless otherwise noted)

Parameter	SD210	SD211	SD212	SD213	SD214	SD215	Unit
V_{DS}	+30	+30	+10	+10	+20	+20	Vdc
V_{SD}	+10	+10	+10	+10	+20	+20	Vdc
V_{DB}	+30	+30	+15	+15	+25	+25	Vdc
V_{SB}	+15	+15	+15	+15	+25	+25	Vdc
V_{GS}	±40	−15	±40	−15	±40	−25	Vdc
		+25		+25		+30	Vdc
V_{GB}	±40	−0.3	±40	−0.3	±40	−0.3	Vdc
		+25		+25		+30	Vdc
V_{GD}	±40	−30	±40	−15	±40	−25	Vdc
		+25		+25		+30	Vdc

I_D	Continuous Drain Current	50mA
P_T	Power Dissipation (at or below T_C = +25°C)	1.2W
	Linear Derating Factor	8.0mW/°C
P_D	Power Dissipation (at or below T_A = +25°C)	300mW
	Linear Derating Factor	2.0mW/°C
T_j	Operating Junction Temperature Range	−55 to +125°C
T_S	Storage Temperature Range	−65 to +175°C

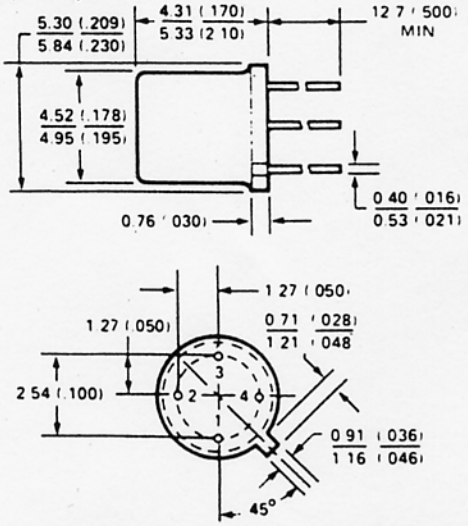
Pin Configuration



Gate Protective Diode on SD211, SD213 SD215 only

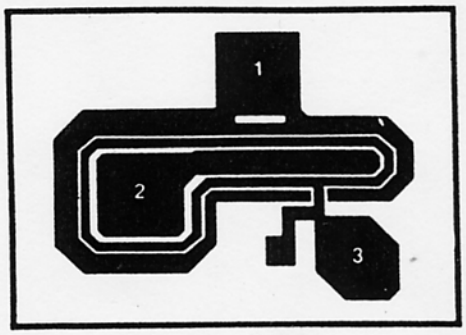
Package Dimensions

(TO-72)



All dimensions in inches and (millimeters)

Chip Configuration



Pad No.	Pad Function
1	SOURCE
2	DRAIN
3	GATE

Body (Substrate) is backside contact

Dimensions: .020 x .024 x .013 inches

Gate internally connected to Protective Diode on SD211, SD213 and SD215 only

N-Channel Enhancement-Mode Lateral D-MOS FETs

DC Electrical Characteristics (T_A = +25°C)

Parameter			SD210, SD211 Min	SD210, SD211 Typ	SD210, SD211 Max	SD212, SD213 Min	SD212, SD213 Typ	SD212, SD213 Max	SD214, SD215 Min	SD214, SD215 Typ	SD214, SD215 Max	Unit	Test Conditions	
BV_{DS}	Drain-Source Breakdown Voltage		30	35								V	$I_D = 10\mu A$ $V_{GS} = V_{BS} = 0$	
			10	25		10	25		20	25		V	$I_D = 10nA$ $V_{GS} = V_{BS} = -5V$	
BV_{SD}	Source-Drain Breakdown Voltage		10			10			20			V	$I_S = 10nA$ $V_{GD} = V_{BD} = -5V$	
BV_{DB}	Drain-Substrate Breakdown Voltage		15			15			25			V	$I_D = 10nA$, $V_{GB} = 0$ Source OPEN	
BV_{SB}	Source-Substrate Breakdown Voltage		15			15			25			V	$I_S = 10\mu A$, $V_{GB} = 0$ Drain OPEN	
$I_{D(off)}$	Drain-Source OFF Current				10			10				nA	$V_{DS} = 10V$	$V_{GS} = V_{BS} = -5V$
											10	nA	$V_{DS} = 20V$	
$I_{S(off)}$	Source-Drain OFF Current				10			10				nA	$V_{SD} = 10V$	$V_{GD} = V_{BD} = -5V$
											10	nA	$V_{SD} = 20V$	
I_{GBS}	Gate-Body Leakage Current	SD210			0.1							nA	$V_{GB} = \pm 40V$	$V_{DB} = V_{SB} = 0$
		SD212						0.1				nA		
		SD214									0.1	nA		
		SD211			10							μA	$V_{GB} = 25V$	
		SD213						10				μA		
		SD215									10	μA	$V_{GB} = 30V$	
$V_{GS(th)}$	Gate Threshold Voltage		0.5	0.6	2.0	0.1	0.6	2.0	0.1	0.6	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1\mu A$, $V_{SB} = 0$	
$r_{DS(on)}$	Drain-Source ON Resistance			50	70		50	70		50	70	ohms	$V_{GS} = 5V$	$I_D = 1mA$
				30	45		30	45		30	45	ohms	$V_{GS} = 10V$	$V_{SB} = 0$

AC Electrical Characteristics (T_A = +25°C)

Parameter		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
g_{fs}	Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	$V_{DS} = 10V$ $I_D = 20mA$ f = 1KHz, $V_{SB} = 0$
$C_{(gs + gd + gb)}$	Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	$V_{DS} = 10V$ $V_{GS} = V_{BS} = -5V$ f = 1MHz
$C_{(gd + db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5	pF	
$C_{(gs + gd)}$	Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0	pF	
$C_{(dg)}$	Reverse Transfer Capacitance		0.2	0.5		0.2	0.5		0.2	0.5	pF	