SD210DE SERIES

Siliconix incorporated

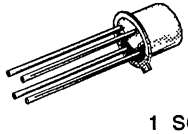
N-Channel Lateral DMOS FETs

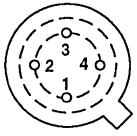
The SD210DE Series of single-pole, single-throw analog switches is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. For long term reliability, this series also features a poly-silicon gate.

For additional design information please see performance curves DMCB, which are located in Section 7.

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} MAX (ns)
SD210DE	20	45	0.5	2
SD212DE	10	45	0.5	2
SD214DE	15	45	0.5	2

TO-72 BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE, CASE

SIMILAR PRODUCTS

- Quad Array, See SD5000 Series
- SO-14 Array, See SD5400 Series
- Zener Protection, See SD211DE Series
- SOT-143, See SST211 Series
- Chips, Order SD21XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT			UNITS
		SD210DE	SD212DE	SD214DE	
Gate-Source, Gate-Drain Gate-Substrate Voltage	V_{GS},V_{GD},V_{GB}	±40	±40	±40	V
Drain-Source Voltage	V_{DS}	30	10	20	
Source-Drain Voltage	V_{SD}	10	10	20	
Drain-Substrate Voltage	V_{DB}	30	15	25	
Source-Substrate Voltage	V_{SB}	15	15	25	
Drain Current	I_D	50	50	50	mA
Power Dissipation (25°C Case)	P_D	1200	1200	1200	mW
Power Derating		9.6	9.6	9.6	mW/°C
Operating Junction Temperature	T_J	-55 to 150			°C
Storage Temperature	T_{stg}	-65 to 200			
Lead Temperature (1/16" from case for 10 seconds)	T_L	300			

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					SD210DE		SD212DE		SD214DE		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10\,\mu$A		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_D = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN		35	15		15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10\,\mu$A, Drain OPEN		35	15		15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10		10			nA
			$V_{DS} = 20$ V	0.9						10	
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10		10			
			$V_{SD} = 20$ V	1						10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = \pm 40$ V		0.001		0.1		0.1		0.1	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1\,\mu$A, $V_{SB} = 0$ V		0.7	0.5	2	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 1$ mA, $V_{SB} = 0$ V	$V_{GS} = 5$ V	58		70		70		70	Ω
			$V_{GS} = 10$ V	38		45		45		45	
			$V_{GS} = 15$ V	30							
			$V_{GS} = 20$ V	26							
			$V_{GS} = 25$ V	24							
DYNAMIC											
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, $f = 1$ kHz		11	10		10		10		mS
Output Conductance	g_{os}			0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, $f = 1$ MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5		0.5	
SWITCHING											
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\ \Omega$, $V_{IN} = 0$ to 5 V		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-OFF Time	$t_{d(OFF)}$			2							
	t_f			6							

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

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