n-channel dual enhancement mode lateral D-MOS FETs

Siliconix

designed for . . .

- **Wideband Differential Amplifiers**
- **Cascode High Slew Rate Amplifiers**
- **Single Ended High-Speed Amps**
- **High-Speed Analog Comparators**
- **Sample & Hold Ckts**
- **High-Speed Matched Analog Switches**

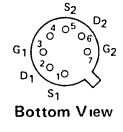
FEATURES
- High Figure-of-Merit gfs/C
- Ultra Low Feedback Capacitance 0.3 pF
- Low Output Capacitance
- Low Input (Gate) Leakage
- Non-Critical Operating Current/Voltage
- Matched Characteristics

BENEFITS
- High Frequency Performance
- High Slew Rate
- High Speed Switching
- Tight Temperature Tracking

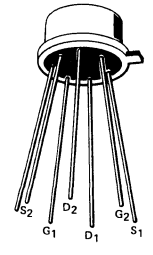
ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Drain Voltage	±25V
Drain-Source Voltage	+25V
Drain Current	50 mA
Device Dissipation (Each Side), (Derate 3 mW/°C)	367 mW
Total Device Dissipation (Derate 4 mW/°C)	500 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-78
See Section 6



Bottom View



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Typ	Max	Unit	Test Conditions
I_{GSS}	Gate Reverse Current		0.05	1	nA	V_{GS} = +15V, V_{DS} = 0
BV_{DS}	Drain-Source Breakdown Voltage	25			V	I_D = 1 μA, V_{GS} = 0
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.1	0.8	2.0	V	V_{DS} = V_{GS} = 10V, I_D = 1 μA
V_{GS}	Gate-Source Voltage		1.9	3.0	V	V_{DG} = 10V, I_D = 5 mA
I_G	Gate Operating Current		0.05	1	nA	V_{DG} = 10V, I_D = 5 mA
gfs	Common-Source Forward Transconductance	7,000	9,000	15,000	μmhos	V_{DS} = 10V, V_{GS} = 0, f = 1 KHz
gos	Common-Source Output Conductance		20	100	μmhos	
$R_{DS(ON)}$	Drain-Source Resistance			60	Ω	I_D = 1 mA, V_{GS} = 10V
C_{iss}	Common-Source Input Capacitance		3.2	5	pF	V_{DS} = 10V, V_{GS} = 0, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		0 5	1.2	pF	

Characteristic			SD2110		SD2120		Unit	Test Condition	
			Min	Max	Min	Max			
MATCHING	$\lvert V_{GS1} = V_{GS2} \rvert$	Differential Gate-Source Voltage		10		20	mV	V_{DG} = 10V, I_D = 5 mA	T_A = 25°C T_B = 125°C
	$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Differential Drift[3]		25 25		50 50	μV/°C μV/°C		T_A = −55°C T_B = 25°C
	$\frac{gfs_1}{gfs_2}$	Transconductance Ratio[2]	0.95	1	0.95	1			f = 1 KHz

NOTES:
1. Pulsewidth ≤ 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.