

N-CHANNEL ENHANCEMENT-MODE D-MOS FET SWITCHES

ORDERING INFORMATION

TO-206AF (TO-72) Package	SD210DE	SD211DE	SD212DE	SD213DE	SD214DE	SD215DE
Shorting Rings	SD210DE/R	SD211DE/R	SD212DE/R	SD213DE/R	SD214DE/R	SD215DE/R
Sorted Chips in Carriers	SD210CHP	SD211CHP	SD212CHP	SD213CHP	SD214CHP	SD215CHP

FEATURES

- High Input to Output Isolation—120dB typical
- Low feedthrough and feedback transients
- Low Inter-electrode Capacitances

APPLICATIONS

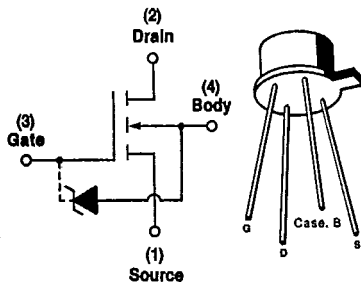
- +30V Switch Drivers—SD210, SD211
- ±10V Analog Switches—SD214, SD215
- ±5V Analog Switches—SD212, SD213

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	SD210	SD211	SD212	SD213	SD214	SD215	UNIT
Breakdown Voltages							
V _{DS}	+30	+30	+10	+10	+20	+20	Vdc
V _{SD}	+10	+10	+10	+10	+20	+20	Vdc
V _{DB}	+30	+30	+15	+15	+25	+25	Vdc
V _{SB}	+15	+15	+15	+15	+25	+25	Vdc
V _{GS}	±40	-15	±40	-15	±40	-25	Vdc
		+25		+25		+30	Vdc
V _{GB}	±40	-0.3	±40	-0.3	±40	-0.3	Vdc
		+25		+25		+30	Vdc
V _{GD}	±40	-30	±40	-15	±40	-25	Vdc
		+25		+25		+30	Vdc

I _D	Continuous Drain Current	50mA
P _T	Power Dissipation (at or below T _C = +25°C)	1.2W
	Linear Derating Factor	12mW/°C
P _D	Power Dissipation (at or below T _A = +25°C)	300mW
	Linear Derating Factor	3.0mW/°C
T _J	Operating Junction Temperature Range	-55 to +125°C
T _S	Storage Temperature Range	-65 to +175°C

SCHEMATIC DIAGRAM

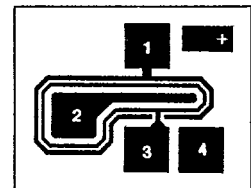


Body internally connected to Case.

Diode protection on SD211/SD213/SD215 only.

PACKAGE DIMENSIONS (TO-72) TO-206AF (See Package 3)

CHIP CONFIGURATION



PAD
1—Source
2—Drain
3—Gate
4—Diode

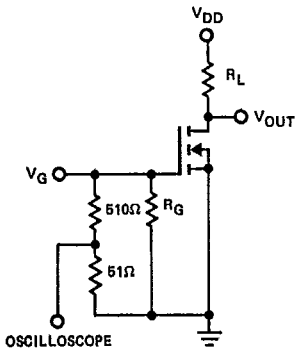
For SD211/213/215CHP bond Gate and Diode
www.DataSheet44.com

Dimensions: .022 × .025 × .013 Inches

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

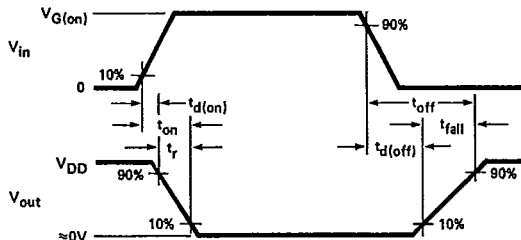
#	PARAMETER		SD210, SD211			SD212, SD213			SD214, SD215			UNIT	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	B _{VDS}	Drain-Source Breakdown Voltage	30	35							V	I _D = 10μA V _{GS} = V _{BS} = 0	
2			10	25		10	25		20	25	V	I _D = 10nA V _{GS} = V _{BS} = -5V	
3		Source-Drain Breakdown Voltage	10			10			20		V	I _S = 10nA V _{GD} = V _{BD} = -5V	
4		Drain-Substrate Breakdown Voltage	15			15			25		V	I _D = 10nA, V _{GB} = 0 Source OPEN	
5		Source-Substrate Breakdown Voltage	15			15			25		V	I _S = 10μA, V _{GB} = 0 Drain OPEN	
6	I _D (off)	Drain-Source OFF Current			10			10			nA	V _{DS} = 10V V _{GS} = V _{BS} = -5V	
7										10	nA	V _{DS} = 20V	
8					10			10				nA	V _{SD} = 10V V _{GD} = V _{BD} = -5V
9		Source-Drain OFF Current								10	nA	V _{SD} = 20V	
10		I _{GBS}	Gate-Body Leakage Current	SD210		0.1						nA	V _{GB} = ±40V V _{DB} = V _{SB} = 0
11	SD212						0.1				nA		
12	SD214									0.1	nA		
13	SD211					10					μA		
14	SD213							10			μA		
15	SD215									10	μA		
16	V _{GS} (th)	Gate Threshold Voltage	0.5	1.0	2.0	0.1		2.0	0.1	1.0	2.0	V	V _{DS} = V _{GS} I _D = 1μA, V _{SB} = 0
17	r _{DS} (on)	Drain-Source ON Resistance		50	70		50	70		50	70	ohms	I _D = 1mA V _{SB} = 0
18				30	45		30	45		30	45	ohms	
19	g _{fs}	Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	V _{DS} = 10V, I _D = 20mA f = 1KHz, V _{SB} = 0
20	C _(gs + gd + gb)	Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	V _{DS} = 10V V _{GS} = V _{BS} = -15V f = 1MHz
21	C _(gd + db)	Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5	pF	
22	C _(gs + sb)	Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0	pF	
23	C _(dg)	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5	pF	
24	t _{d(on)}	Turn ON Delay Time		0.7	1.0		0.7	1.0		0.7	1.0	nSec	
25	t _r	Rise Time		0.8	1.0		0.8	1.0		0.8	1.0	nSec	
26	t _{off}	Turn OFF Time		10			10			10		nSec	

SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
 $t_r < 0.5 \text{ nSEC}$
 PULSE WIDTH - 100 nSEC
 SAMPLING OSCILLOSCOPE
 $t_s < 0.36 \text{ nSEC}$
 $R_{in} > 1M\Omega$
 $C_{in} < 2.0 \text{ pF}$

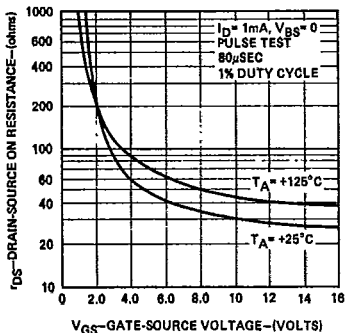
TEST WAVEFORMS



TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

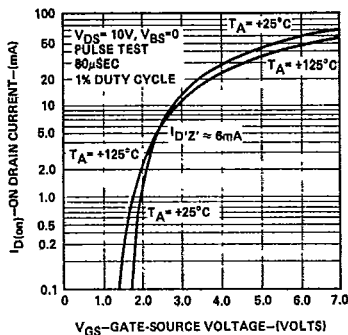
DRAIN-SOURCE ON RESISTANCE

—vs—
GATE-SOURCE VOLTAGE



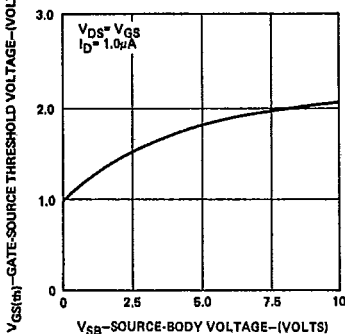
ON DRAIN CURRENT

—vs—
GATE-SOURCE VOLTAGE



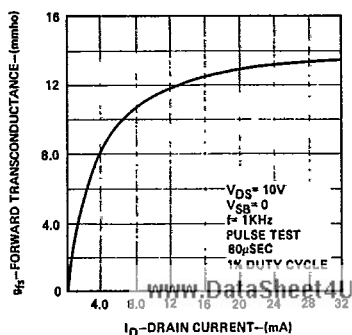
GATE-SOURCE THRESHOLD VOLTAGE

—vs—
SOURCE-BODY VOLTAGE

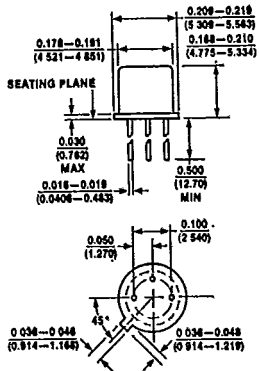


FORWARD TRANSCONDUCTANCE

—vs—
ON DRAIN CURRENT

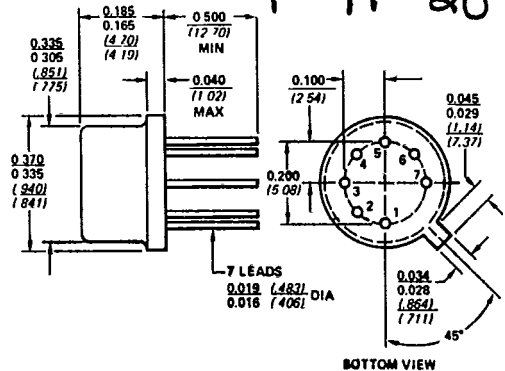


Package 1 (TO-18) TO-206AA



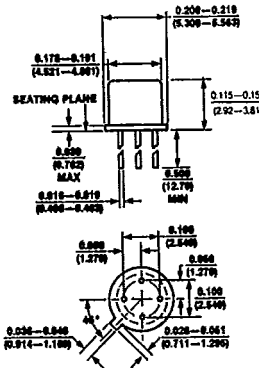
All Dimensions in Inches and (millimeters)

Package 4 (TO-78)



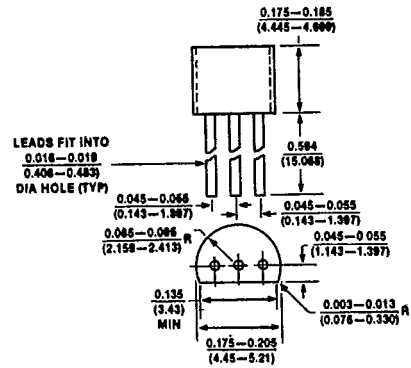
All Dimensions in Inches and (millimeters)

Package 2 (TO-52) 4-Lead



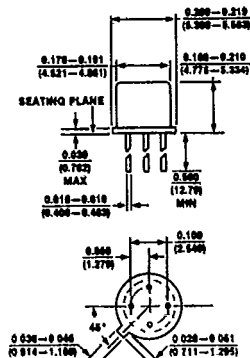
All Dimensions in Inches and (millimeters)

Package 5 (TO-92) TO-226AA



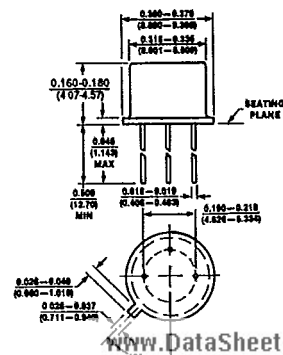
All Dimensions in Inches and (millimeters)

Package 3 (TO-72) TO-206AF



All Dimensions in Inches and (millimeters)

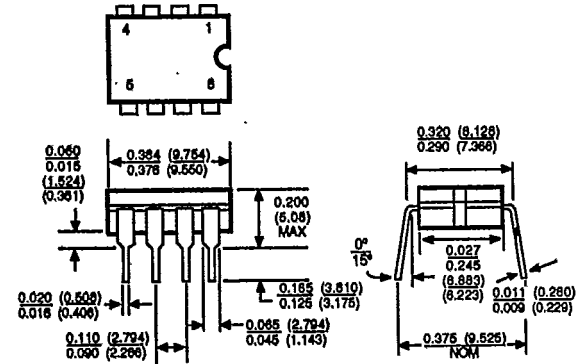
Package 6 (TO-39) TO-205AF



All Dimensions in Inches and (millimeters)

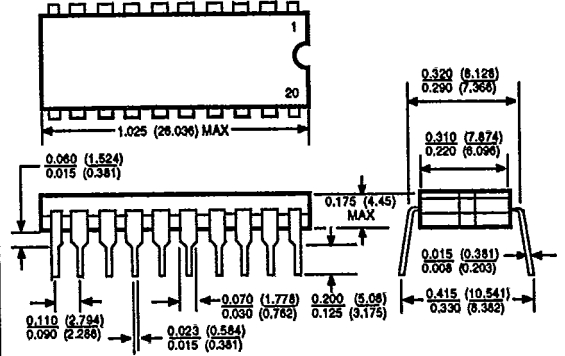
T-91-20

Package 13 8-Pin Ceramic Dip



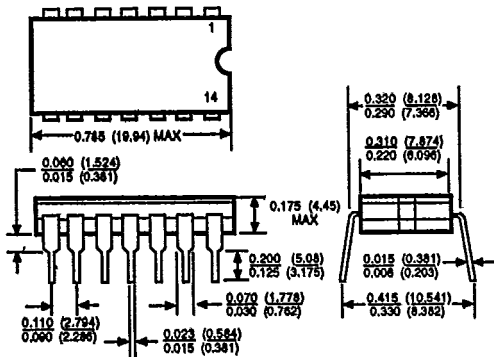
All Dimensions in Inches and (millimeters)

Package 16 20-Pin Ceramic Dip



All Dimensions in Inches and (millimeters)

Package 14 (TO-116) 14-Pin Ceramic Dip



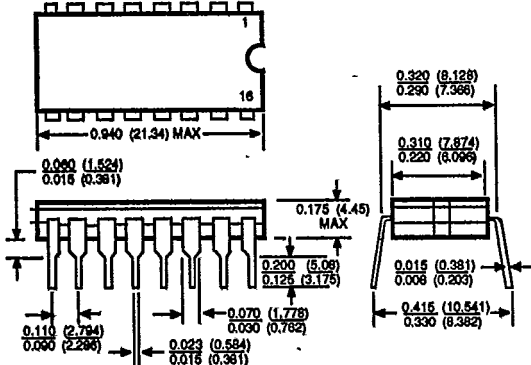
All Dimensions in Inches and (millimeters)

Package 17

NONE

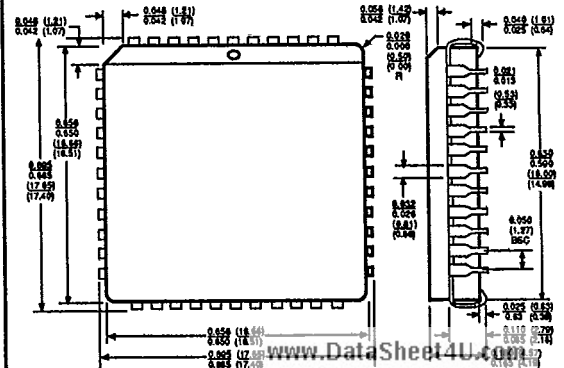
All Dimensions in Inches and (millimeters)

Package 15 16-Pin Ceramic Dip



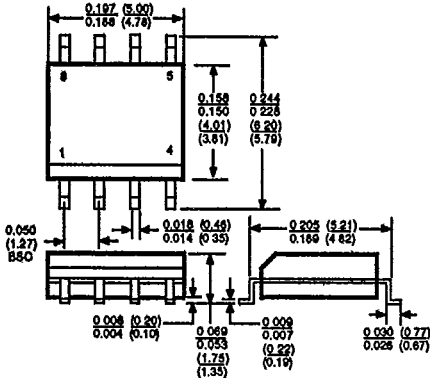
All Dimensions in Inches and (millimeters)

Package 18 PLCC-44



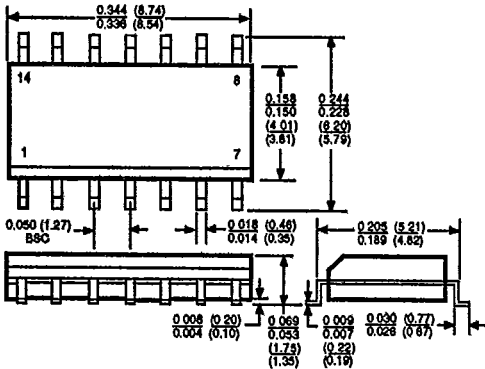
All Dimensions in Inches and (millimeters)

Package 19 (SO-8)



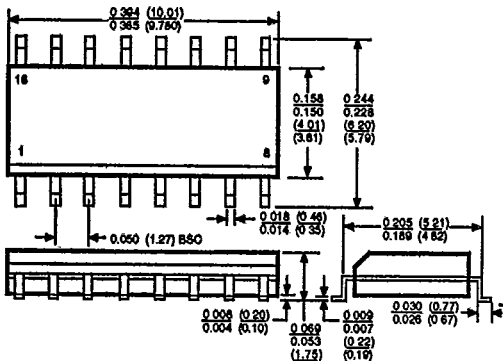
All Dimensions in Inches and (millimeters)

Package 20 (SO-14)



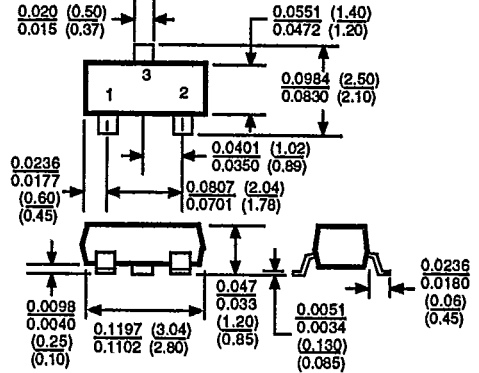
All Dimensions in Inches and (millimeters)

Package 21 (SO-16)



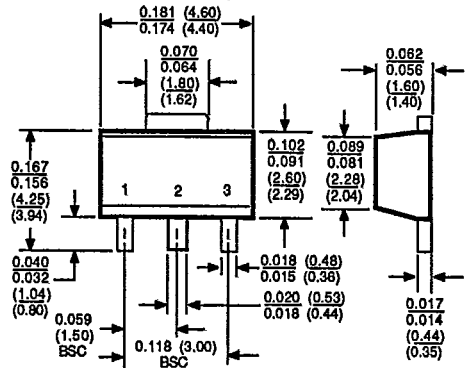
All Dimensions in Inches and (millimeters)

Package 22 (SOT-23) TO-236AA



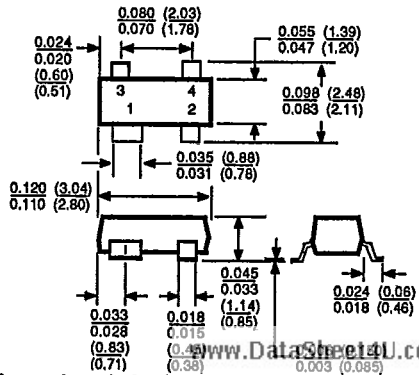
All Dimensions in Inches and (millimeters)

Package 23 (SOT-89) TO-243AA



All Dimensions in Inches and (millimeters)

Package 24 (SOT-143)



All Dimensions in Inches and (millimeters)