D-MOS FET quad analog switch arrays and driver

Siliconix

designed for Military and Industrial Applications . . .

SD5200 APPLICATIONS

- **Switch Drivers**

DESCRIPTION

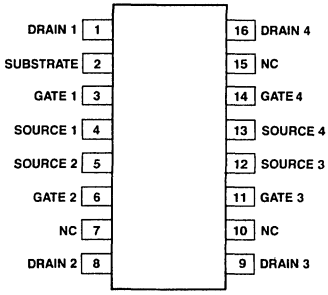
The SILICONIX D-MOS SD5200 monolithic arrays of silicon, insulated-gate, field-effect transistors using the N-channel enchancement mode technology.

This device is designed to handle a wide variety of driver applications. The SD5200 is intended for use as a 30V driver to complement the other switch products.

FEATURES

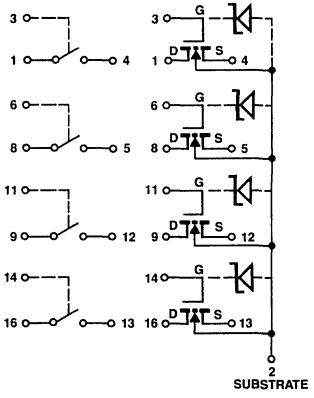
- **Low Input Capacitance—2.4 pF**
- **Low Feedback Capacitance—0.3 pF**
- **Low Output Capacitance—1.3 pF**
- **±10V Analog Signal Range**
- **Low Propagation Delay Time—600 ps**
- **Low on Resistance—30Ω**
- **Low Feedthrough and Feedback Transients**
- **Ion Implanted for Greater Reliability**
- **High Channel-to-Channel Isolation—107 dB**
- **Transient Protection for Gates**

I, N PACKAGE
(TOP VIEW)



ORDER PART NO.
SD5200N (PLASTIC)
SD52001 (SIDE BRAZE)

SD5200



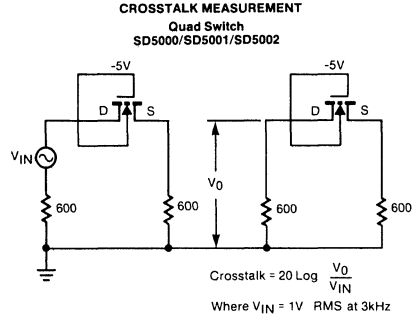
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified.)

Parameters		SD5200	Unit
V_{DS} Drain-to-Source		+30	V_{dc}
V_{SD} Source-to-Drain[1]		+0.5	
V_{DB} Drain-to-Substrate		+30	
V_{SB} Source-to-Substrate		+0.5	
V_{GS} Gate-to-Source		+20	
V_{GB} Gate-to-Substrate		+20	
		−0.3	
V_{GD} Gate-to-Drain		+20	
I_D Drain Current		50	mA
Ambient Temperature Range	Storage	−55 to +150	°C
	Operating	−55 to +125	
Power Dissipation	Total Package Dissipation[2]	640	mW
	Individual Transistor Dissipation	300	

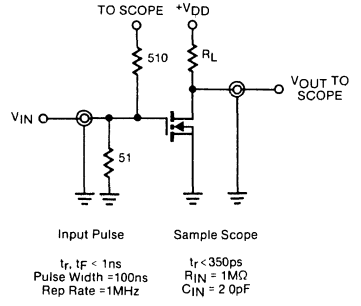
NOTES

1. Refer to test conditions specified in Electrical Characteristics Table.
2. Derated 5 mW per degree centigrade.

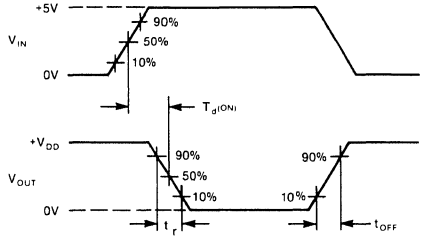
TEST CIRCUIT



SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS

		$t_{d(ON)}$(ns)		t_{r}(ns)		* t_{OFF}(ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0 7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and does not depend on the device characteristics.

DC ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

Parameter		Test Conditions	SD5200			Unit
			Min	Typ	Max	
BREAKDOWN VOLTAGE BV_{DS}	Drain-to-Source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\ \mu A$	30	35		V
		$V_{GS} = V_{BS} = -5V$, $I_S = 10$ nA				
BV_{SD}	Source-to-Drain	$V_{GD} = V_{BD} = -5V$, $I_D = 10$ nA				V
BV_{DB}	Drain-to-Substrate	$V_{GB} = 0V$, Source Open $I_D = 10$ nA				V
BV_{SB}	Source-to-Substrate	$V_{GB} = 0V$, Drain Open $I_S = 10\ \mu A$				V
LEAKAGE CURRENT $I_{DS(OFF)}$	Drain-to-Source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +15V$ $V_{DS} = +10V$				nA
$I_{SD(OFF)}$	Source-to-Drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +15V$ $V_{SD} = +10V$				nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = 30V$				μA
V_T	Threshold Voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\ \mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	V
$r_{DS(ON)}$	Drain-to-Source Resistance	$I_D = 1.0$ mA, $V_{SB} = 0$, $V_{GS} = +5V$		50	80	Ω
		$I_D = 1.0$ mA, $V_{SB} = 0$, $V_{GS} = +10V$		30		
		$I_D = 1.0$ mA, $V_{SB} = 0$, $V_{GS} = +15V$		23		
		$I_D = 1.0$ mA, $V_{SB} = 0$, $V_{GS} = +20V$		19		
$r_{DS(ON)}$	Resistance Match[1]	$I_D = 1.0$ mA, $V_{SB} = 0$ $V_{GS} = +5V$				Ω

NOTE:
1. This untested parameter is guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	SD5200			Unit
			Min	Typ	Max	
gfs	Forward Transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20$ mA, f = 1 kHz	10	15		mmho
$C_{(GS+GD+GB)}$	Gate Node Capacitances	$V_{DS} = 10V$, f = 1 MHz $V_{GS} = V_{BS} = -15V$ See Capacitance Model in Figure 1		2.4	3.5	pF
$C_{(GD+DB)}$	Drain Node Capacitances			1.3	1.5	
$C_{(GS+SB)}$	Source Node Capacitances					
C_{DG}	Reverse Transfer Capacitances			0.3	0.5	
C_T	Cross Talk	See Test Circuits No. 1 and 2, f = 3 kHz		−107		dB