SD5400 SERIES

Siliconix incorporated

N-Channel Lateral DMOS Quad FETs

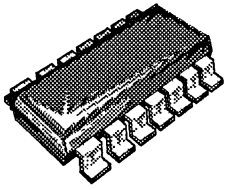
The Siliconix SD5400 series is a monolithic array of single-pole, single-throw analog switches designed for high-speed switching in audio, video and high frequency applications in communications, instrumentation, and process control. Designed with the Siliconix DMOS process, the SD5400 is rated for analog signals of ±10 V, while the SD5401 and SD5402 are rated for ±5 V and ±7.5 V respectively.

These bidirectional switches feature very low interelectrode capacitance and on-resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

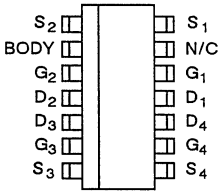
For additional design information please see performance curves DMCA, which are located in Section 7.

PART NUMBER	$V_{(BR)DS}$ MIN (V)	$V_{GS(TH)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	t_{ON} MAX (ns)
SD5400CY	20	2.0	70	2
SD5401CY	10	2.0	70	2
SD5402CY	15	2.0	70	2

SO-14



TOP VIEW



SIMILAR PRODUCTS

- TO-18, See SD211DE Series
- 16-Pin DIP, See SD5000 Series
- SOT-143, See SST211 Series
- Chips, Order SD540XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT			UNITS
			SD5400	SD5401	SD5402	
Gate-Source, Gate-Drain Voltage		V_{GS}, V_{GD}	30/–25	25/–15	30/–22.5	V
Drain-Substrate, Source-Substrate Voltage		V_{DB}, V_{SB}	25	15	22.5	
Drain-Source, Source-Drain Voltage		V_{DS}, V_{SD}	20	10	15	
Gate-Substrate Voltage [1]		V_{GB}	30/–0.3	25/–0.3	30/–0.3	
Drain Current		I_D	50			mA
Power Dissipation	Package	P_D	500			mW
	Each Device		300			
Power Derating (Package)			5			mW/°C
Operating Junction Temperature		T_J	–55 to 125			°C
Storage Temperature		T_{stg}	–55 to 125			
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			

[1] These devices feature an internal Zener protected gate.

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				SD5400CY		SD5401CY		SD5402CY		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA	30	20		10		15		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA	22	20		10		15		V
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN	35	25		15		22.5		V
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain OPEN	35	25		15		22.5		V
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V, $V_{DS} = 20$ V	0.9		10					nA
		$V_{DS} = 10$ V	0.4				10			nA
		$V_{DS} = 15$ V	0.7						10	nA
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V, $V_{SD} = 20$ V	1		10					nA
		$V_{SD} = 10$ V	0.5				10			nA
		$V_{SD} = 15$ V	0.8						10	nA
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$ V	10^{-5}		1		1		1	µA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$µA, $V_{SB} = 0$ V	0.7	0.1	2	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 1$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V	58		70		70		70	Ω
		$V_{GS} = 10$ V	38							Ω
		$V_{GS} = 15$ V	30							Ω
		$V_{GS} = 20$ V	26							Ω
Resistance Match		$I_D = 1$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V	1		5		5		5	Ω
DYNAMIC										
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, $f = 1$ kHz	11	10		10		10		mS
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, $f = 1$ MHz, $V_{GS} = V_{BS} = -15$ V	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$		1.1		2		2		2	pF
Source Node Capacitance	$C_{(GS+SB)}$		3.7		6		6		6	pF
Reverse Transfer Capacitance	C_{rss}		0.2		0.5		0.5		0.5	pF
Crosstalk		f = 3 kHz, See Test Circuits in DMCA Performance Curves	-107							dB
SWITCHING										
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω, $V_{IN} = 5$ V	0.5		1		1		1	ns
	t_r		0.6		1		1		1	ns
Turn-OFF Time	$t_{d(OFF)}$		2							ns
	t_f		6							ns

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

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