SD60C32/P, SD60C52/P

CMOS SINGLE-COMPONENT 8-BIT MICROCOMPUTER

Description

The AUK 60C32/P 60C52/P is a high-performance micro controller fabricated with AUK high-density CMOS technology. The AUK CMOS technology combines the high speed and density characteristics of MOS with the low power attributes of CMOS.

The 60C52 contains a 8K×8 ROM, a 256×8 RAM, 32 I/O lines, three 16bit counter/timers, a six sourc two-priority level nested interrupt structure, a serial I/O port for either multi-processor communication, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device has two software selectable modes of power reduction idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning.

The power-down mode saves the RAM contents but freezes the oscillator , causing all other chip function to be inoperative.

Features

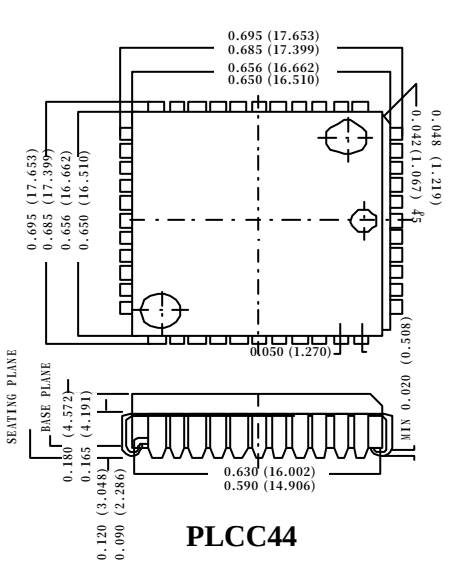
- 8-bit CPU optimized for control applications.
- Pin-to-pin compatible with intel's 80C52/80C32.
- 256 Bytes of on-chip data RAM.
- 60C52 low power CPU only.
- 32 programmable I/O lines.
- Three 16bit timer/counters.
- TTL and CMOS compatible logic levels
- 64K external program memory space and data memory space.
- MCS-51 fully compatible instruction set
- ONCE™ (ON-circuit emulation) mode
- Power control modes
  - Idle mode
  - Power down mode
- 6 interrupt source

Ordering Information

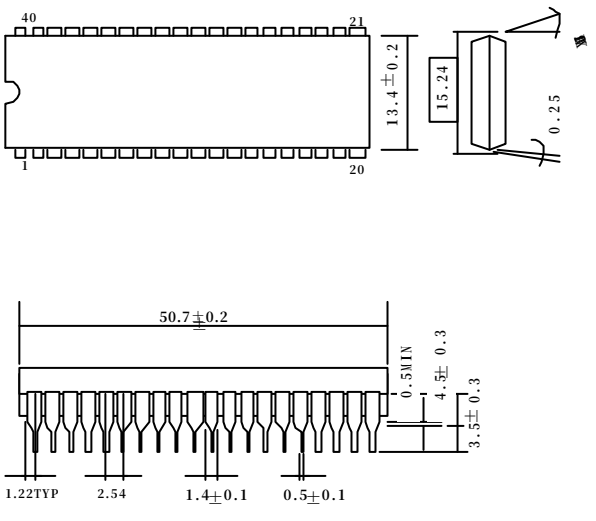
Type NO.	Marking	Package Code	Type NO.	Marking	Package Code
SD60C32	SD60C32	PLCC44	SD60C32P	SD60C32	DIP40
SD60C52	SD60C52	PLCC44	SD60C52P	SD60C52	DIP40

Outline Dimensions

unit : mm



PLCC44

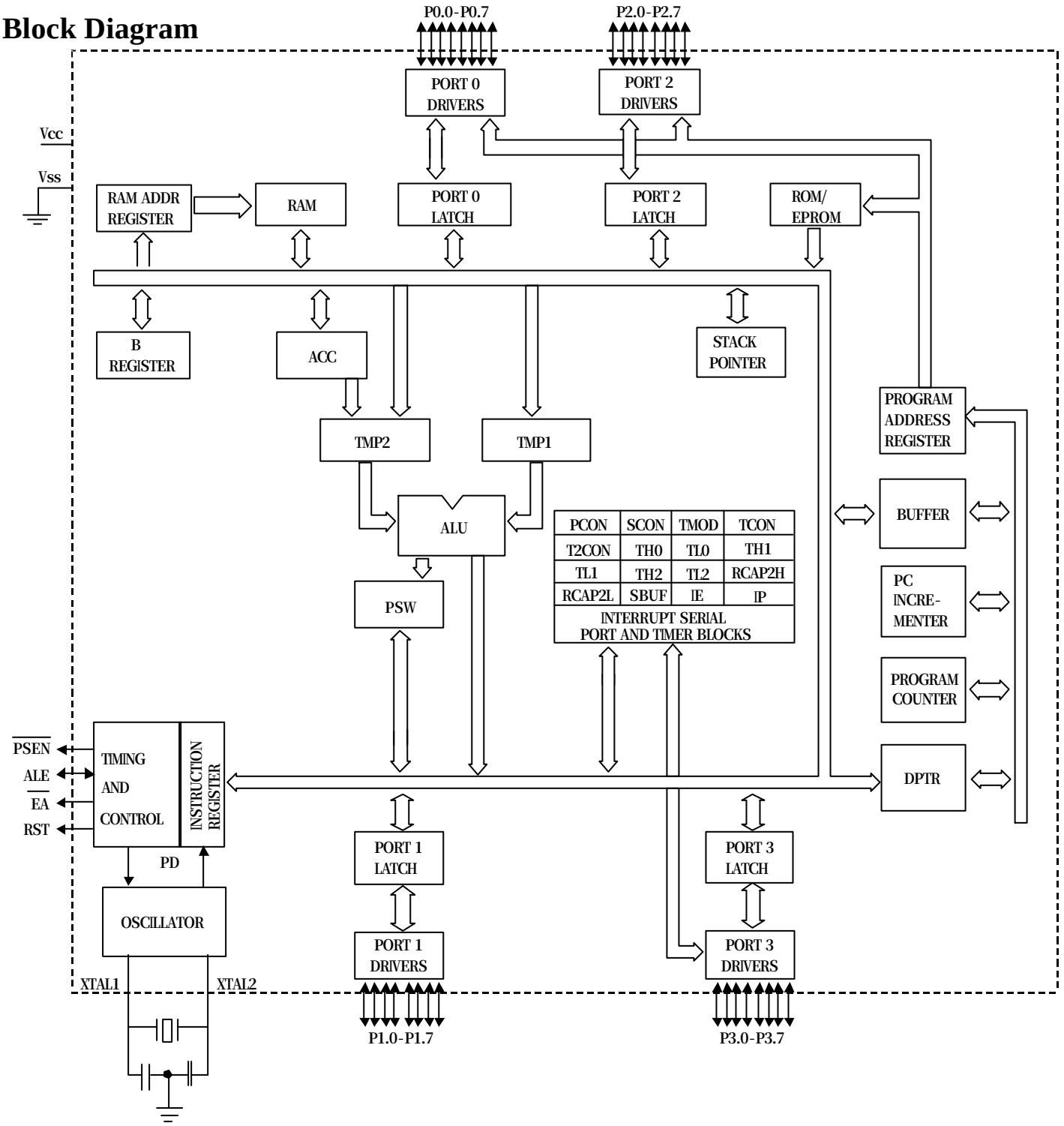


DIP40

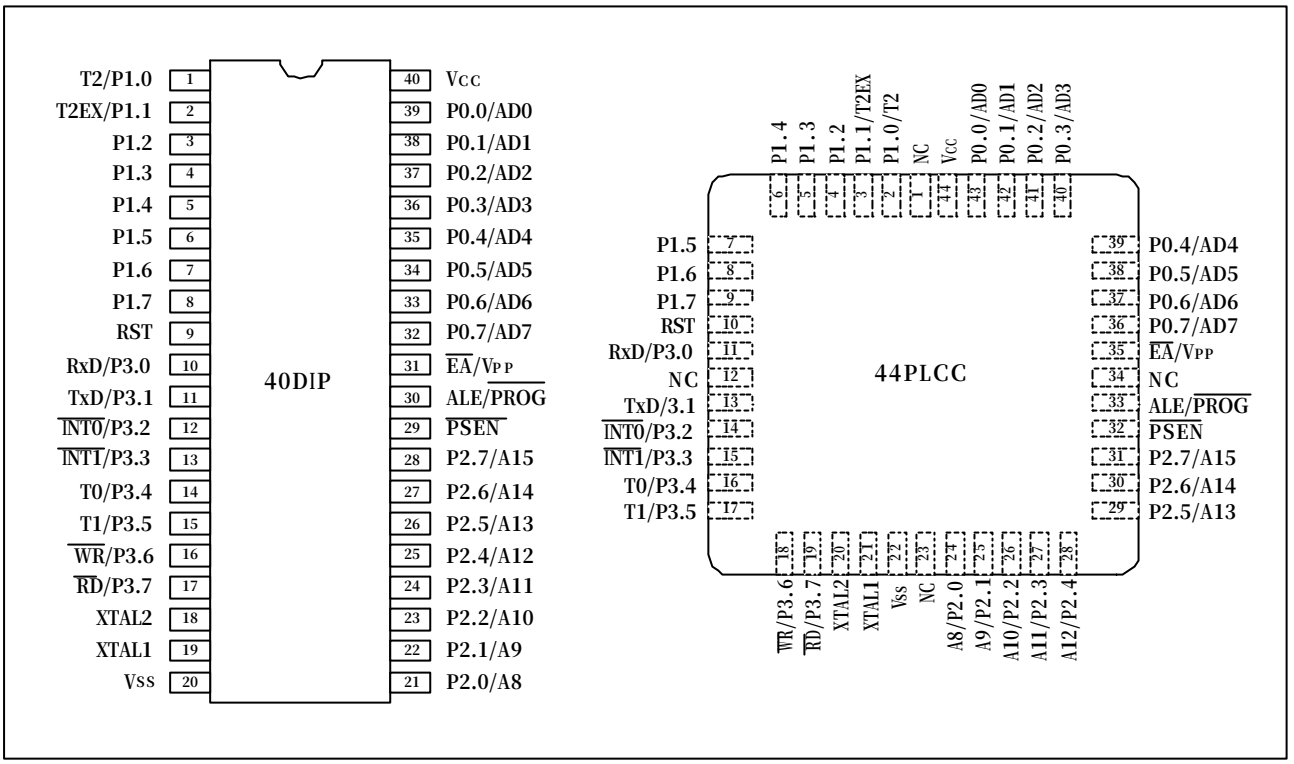
Absolute Maximum Ratings

Characteristic	Rating	Unit
Ambient temperature under bias	0 ~ +70	°C
Storage temperature	- 65 ~ + 150	°C
Voltage on any pin to V_{SS}	- 0.5 ~ V_{CC} + 0.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation	1.5	W

Block Diagram



Pin Configuration



Pin Description

V_{CC} : PIN 40 (DIP40), PIN 44 (PLCC44)

Supply voltage during normal, Idle and power down operations.

V_{SS} : PIN 20 (DIP40), PIN 22 (PLCC44)

Circuit ground.

Port 0 : PIN 32~39 (DIP40), PIN 36~43 (PLCC44)

Port 0 is an 8bit open drain bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory.

In this application it uses strong internal pullups when emitting 1's and source and sink several LS TTL inputs. Port 0 outputs the code bytes during program verification on the 60C52 external pullups resistors are required during program verification.

Port 1 : PIN 1~8 (DIP40), PIN 2~9 (PLCC44)

Port 1 output buffers can drive LSI TTL inputs.

Port 1 is an 8bit bi-directional I/O port with internal pullups.

Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current because of the internal pullups

Pin Description (Continued)

In addition, Port 1 serves the functions of the following special features of the 60C52.

Port Pin	Alternate Function
P1.0	T2(External Count Input to Timer / Counter 2)
P1.1	T2EX(Timer / Counter 2 Capture/Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during ROM verification.

Port 2 : PIN 21~28 (40DIP), PIN 24~31 (44PLCC)

Port 2 is an 8-bit bi-directional I/O port with internal pullups. The port 2 output buffers can drive LS TTL inputs.

Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as input.

As inputs, port 2 pins that are externally being pulled low will source current because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8 bit addresses (MOVX @ Ri), port 2 emits the contents of the P2 special function register

Port 3 : PIN 10~17 (DIP40), PIN 13~19 (PLCC44)

Port 3 is an 8bit bi-directional I/O port with internal pullups. The port 3 output buffers can drive LS TTL input. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the pullups.

Port 3 also serves the function of various special feature of the MCS-51 Family, as listed below :

Port PIN	PIN NO.	Alternate Function
P3.0	10	RxD (Serial input port)
P3.1	11	TxD (Serial output port)
P3.2	12	$\overline{\text{INT0}}$ (External interrupt 0)
P3.3	13	$\overline{\text{INT1}}$ (External interrupt 1)
P3.4	14	T0 (Timer 0 external input)
P3.5	15	T1 (Timer 1 external input)
P3.6	16	$\overline{\text{WR}}$ (External data memory write strobe)
P3.7	17	$\overline{\text{RD}}$ (External data memory read strobe)

RST: PIN 9 (DIP40), PIN 10 (PLCC44)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: PIN 30 (DIP40), PIN 33 (PLCC44)

Address latch enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes.

Note : However, that one ALE pulse is skipped during each access to external data memory.

This pin is also the program pulse input PROG during EPROM programming.

$\overline{PSEN}$: PIN 29 (DIP40), PIN 32 (PLCC44)

Program store enable is the read strobe to external program memory. When the 60C52 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.

$\overline{EA}$: PIN 31 (DIP40), PIN 35 (PLCC44)

External access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH.

If $\overline{EA}$ is strapped to V_{CC} the device executes from internal program memory unless the program counter contains an address greater than 0FFFH.

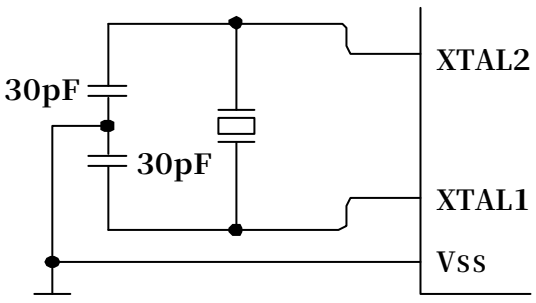
XTAL1: PIN 19 (DIP40), PIN 21 (PLCC44)

Input to the Inverting oscillator amplifier and input to the internal clock generator circuits.

XTAL2: PIN 18 (DIP40), PIN 20 (PLCC44)

Output from the inverting oscillator amplifier

0 Crystal Oscillator



NC: PIN1, 12, 23, 34 (PLCC44)

Non connection pins.

Idle Mode

In the Idle mode, the CPU puts itself to sleep while all the on chip peripherals stay active. The instruction that invokes the Idle mode is the last instruction executed in the normal operating mode before Idle mode is activated.

The content of the on-chip RAM and all the special function registers remain intact during this mode. The Idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor the same as a power on reset.

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and special function register retain their values until the power down mode is terminated.

The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

The control bits for the reduced power modes are in the special function register PCON.

Table. Status of the external pins during Idle and power down modes.

Mode	Program Memory	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Electrical Characteristics (DC)

(T_a = 0℃ ~ 70℃ or -40℃ ~ 85℃, V_{CC} = 5V ± 20%, V_{SS}=0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP.	MAX	
V_{IL}	Input low voltage, except $\overline{EA}$		-0.5		$0.2V_{CC}$-0.1	V
V_{IL1}	Input low voltage to $\overline{EA}$		0		$0.2V_{CC}$-0.3	V
V_{IH}	Input high voltage, except XTAL1,RST		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage to XTAL1, RST		0.7 V_{CC}		V_{CC}+0.5	V
V_{OL}	Output low voltage to ports 1,2,3	I_{OL}=1.6mA			0.45	V
V_{OL1}	Output low voltage to ports 0, ALE, $\overline{PSEN}$	I_{OL}=3.2mA			0.45	V
V_{OH}	Output high voltage to ports 1,2,3,ALE,PSEN	I_{OH}=-60μA I_{OH}=-30μA I_{OH}=-10μA	V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5			V
V_{OH1}	Output high voltage (port 0 in external bus mode)	I_{OH}=-200μA I_{OH}=-3.2mA I_{OH}=-7.0mA	V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5			V
I_{IL}	Logical 0 input current to ports 1,2,3	V_{IN}=0.45V		-10	-50	μA
I_{TL}	Logical 1 to 0 transition current to ports 1,2,3	VI_N=2V		- 265	-650	μA
I_{LI}	Input leakage current to port 0, $\overline{EA}$	0 < V_{IN} < V_{CC}		0.02	±10	μA
I_{CC}	Power supply current Active mode @ 12MHz Idle mode @ 12MHz Power-down mode			15 5 5	30 7.5 75	mA mA μA
R_{RST}	Internal reset pull-down resistor		40	100	225	kohm
C_{IO}	Pin capacitance			10		pF

Electrical Characteristics (AC)

(T_a = 0℃ ~ 70℃ or -40℃ ~ 85℃, V_{CC} = 5V ± 20%, V_{SS}=0V)

SYSBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$		Oscillator frequency : Speed Versions 60C32/60C52			3.5	16	MHz
t_{LHLL}	1	ALE pulse width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	1	Address valid to ALE low	43		t_{CLCL}-40		ns
t_{LLAX}	1	Address hold after ALE low	53		t_{CLCL}-30		ns
t_{LLIV}	1	ALE low to valid instruction in		234		$4t_{CLCL}$-100	ns
t_{LLPL}	1	ALE low to PSEN low	53		t_{CLCL}-30		ns
t_{PLPH}	1	PSEN pulse with	205		$3t_{CLCL}$-45		ns
t_{PLIV}	1	PSEN low to valid instruction in		145		3_{CLCL}-105	ns
t_{PXIX}	1	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	1	Input instruction float after PSEN		59		t_{CLCL}-25	ns
t_{AVIV}	1	Address to valid instruction in		312		$5t_{CLCL}$-105	ns
t_{PLAZ}	1	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	2, 3	RD pulse width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	2, 3	WR pulse width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	2, 3	RD low to valid data in		252		$5t_{CLCL}$-165	ns
t_{RHDX}	2, 3	Data hold after RD	0		0		ns
t_{RHDZ}	2, 3	Data float after RD		107		$2t_{CLCL}$-70	ns
t_{LLDV}	2, 3	ALE low to valid data in		517		$8t_{CLCL}$-150	ns
t_{AVDV}	2, 3	Address to valid data in		585		$9t_{CLCL}$-165	ns
t_{LLWL}	2, 3	ALE low to RD or WR low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	2, 3	Address valid to WR low or RD low	203		$4t_{CLCL}$-130		ns
t_{QVWX}	2, 3	Data valid to WR transition	33		t_{CLCL}-50		ns
t_{WHQX}	2, 3	Data hold after WR	33		t_{CLCL}-50		ns
t_{QVWH}	2, 3	Data valid to WR High	433		$7t_{CLCL}$-150		ns
t_{RLAZ}	2, 3	RD low to address float		0		0	ns
t_{WHLH}	2, 3	RD or WR high to ALE high	43	123	t_{CLCL}-40	t_{CLCL}-40	ns
External Clock							
t_{CHCX}	4	High time	20		20		ns
t_{CLCX}	4	Low time	20		20		ns
t_{CLCH}	4	Rise time		20		20	ns
t_{CHCL}	4	Fall time		20		20	ns

Electrical Characteristics (Continued)

(T_a = 0℃ ~ 70℃ or -40℃ ~ 85℃, V_{CC} = 5V ± 20%, V_{SS}=0V)

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$		Oscillator frequency : Speed Versions 60C52/60C32			3.5	16	MHz
t_{LHLL}	1	ALE pulse width	85		$2t_{CLCL}$-40		ns
t_{AVLL}	1	Address valid to ALE low	23		t_{CLCL}-40		ns
t_{LLAX}	1	Address hold after ALE low	33		t_{CLCL}-30		ns
t_{LLIV}	1	ALE low to valid instruction in		150		$4t_{CLCL}$-100	ns
t_{LLPL}	1	ALE low to PSEN low	23		t_{CLCL}-40		ns
t_{PLPH}	1	PSEN pulse with	143		$3t_{CLCL}$-45		ns
t_{PLIV}	1	PSEN low to valid instruction in		83		3_{CLCL}-105	ns
t_{PXIX}	1	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	1	Input instruction float after PSEN		38		t_{CLCL}-25	ns
t_{AVTV}	1	Address to valid instruction in		208		$5t_{CLCL}$-105	ns
t_{PLAZ}	1	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	2, 3	RD pulse width	275		$6t_{CLCL}$-100		ns
t_{WLWH}	2, 3	WR pulse width	275		$6t_{CLCL}$-100		ns
t_{RLDV}	2, 3	RD low to valid data in		148		$5t_{CLCL}$-165	ns
t_{RHDX}	2, 3	Data hold after RD	0		0		ns
t_{RHDZ}	2, 3	Data float after RD		55		$2t_{CLCL}$-70	ns
t_{LLDV}	2, 3	ALE low to valid data in		350		$8t_{CLCL}$-150	ns
t_{AVDV}	2, 3	Address to valid data in		398		$9t_{CLCL}$-165	ns
t_{LLWL}	2, 3	ALE low to RD or WR low	138	238	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	2, 3	Address valid to WR low or RD low	120		$4t_{CLCL}$-130		ns
t_{ZVWX}	2, 3	Data valid to WR transition	13		t_{CLCL}-50		ns
t_{WHOX}	2, 3	Data hold after WR	13		t_{CLCL}-50		ns
t_{OVWH}	2, 3	Data valid to WR High	288		$7t_{CLCL}$-150		ns
t_{RLAZ}	2, 3	RD low to address float		0		0	ns
t_{WHLH}	2, 3	RD or WR high to ALE high	23	103	t_{CLCL}-40	t_{CLCL}+40	ns
External Clock							
t_{CHCX}	4	High time	20		20		ns
t_{CLCX}	4	Low time	20		20		ns
t_{CLCH}	4	Rise time		20		20	ns
t_{CHCL}	4	Fall time		20		20	ns

Timing Diagram

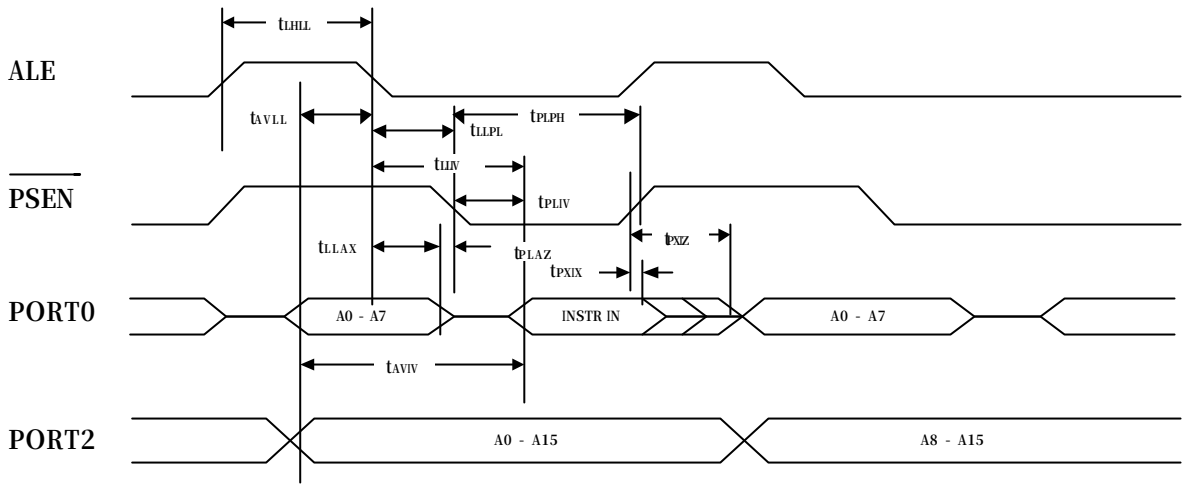


Figure 1. External Program Memory Read Cycle

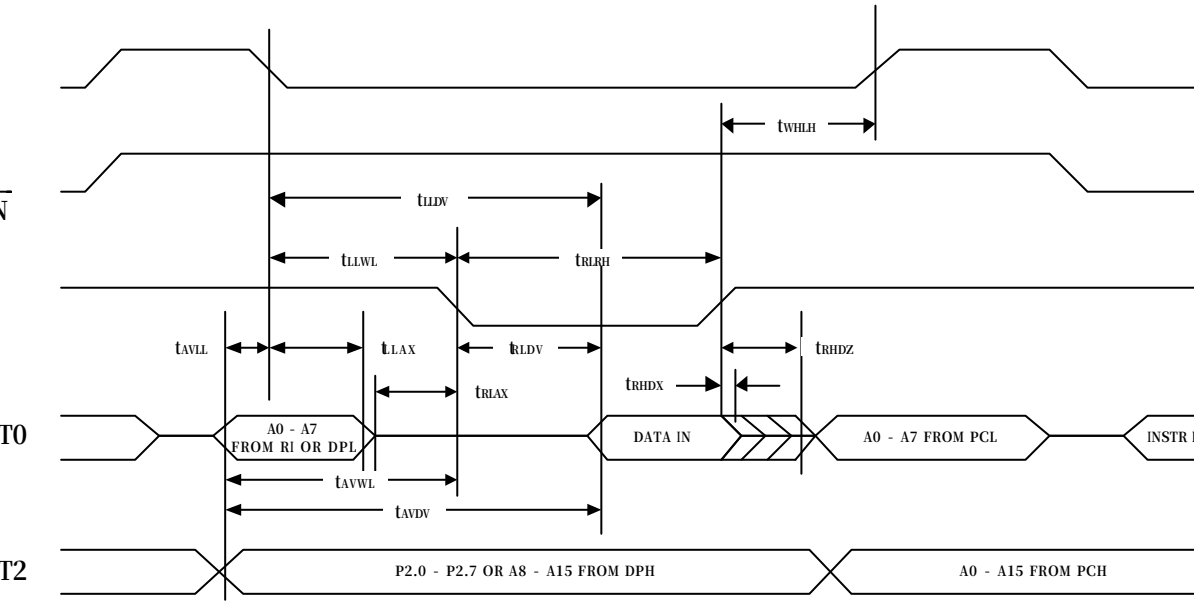


Figure 2. External Data Memory Read Cycle

Timing Diagram (Continued)

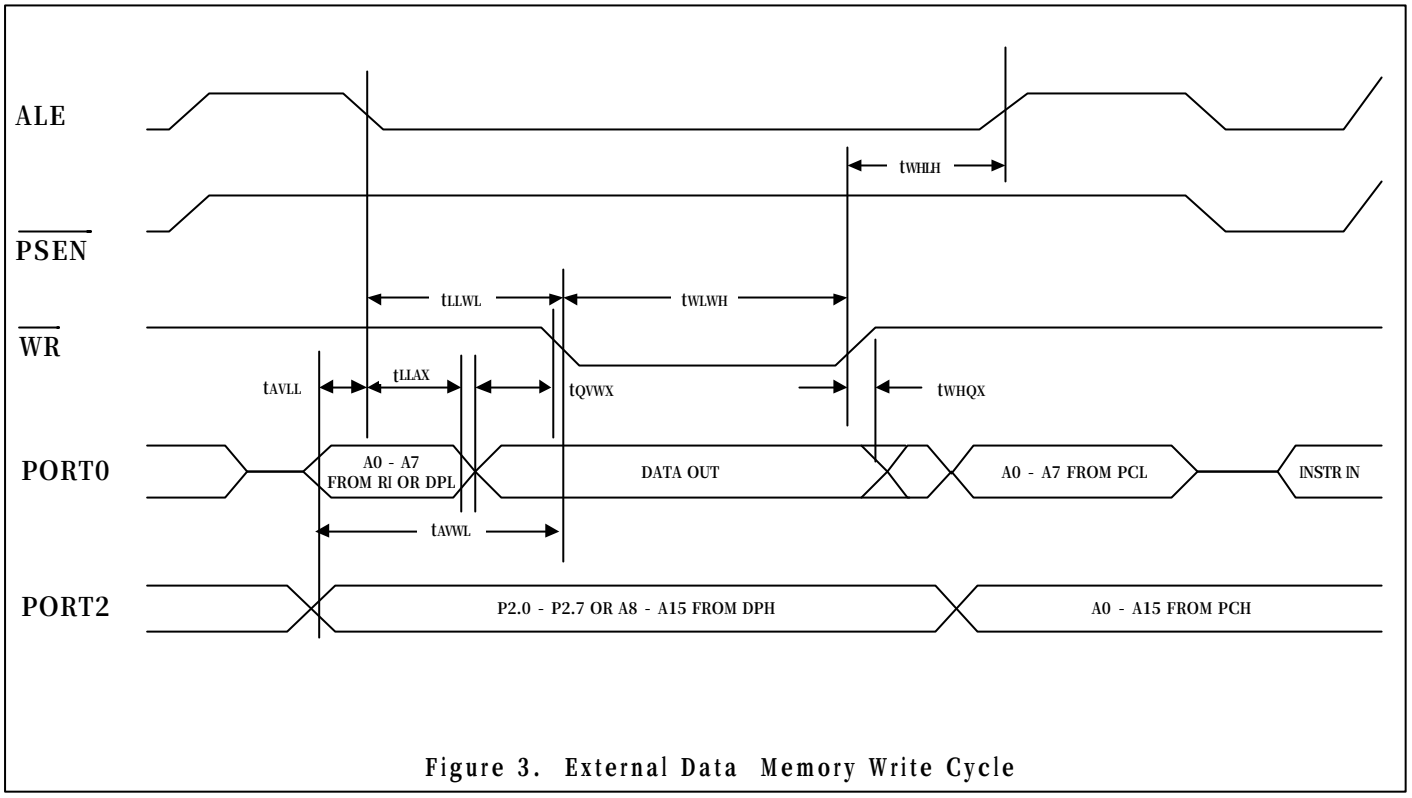


Figure 3. External Data Memory Write Cycle

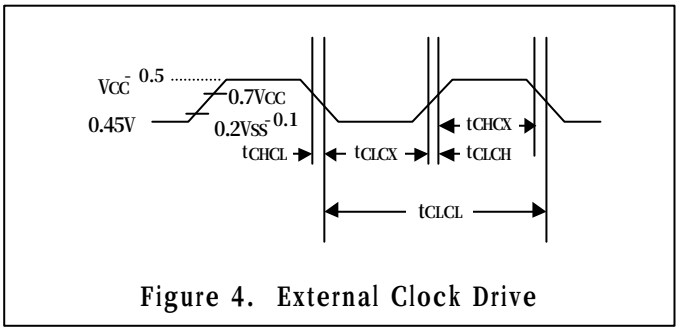
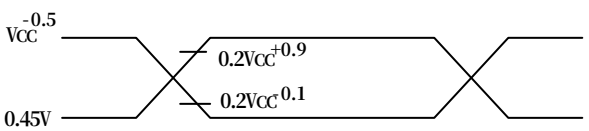
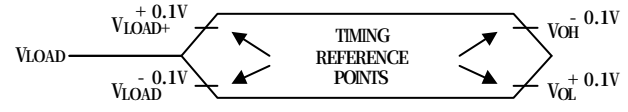


Figure 4. External Clock Drive



NOTE :
AC Inputs during testing are driven at VCC - 0.5 for a logic '1' and 0.45V for a logic '0'. Timing measurements are made at VIH min for a logic '1' and VIL for a logic '0'

Figure 5. AC Testing Input/Output



NOTE :
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begings to float when a 100mV change from the loaded VOH/VOL level occurs. IOH/IOL ≥ 20mA

Figure 6. Float Waveform

Timing Diagram (Continued)

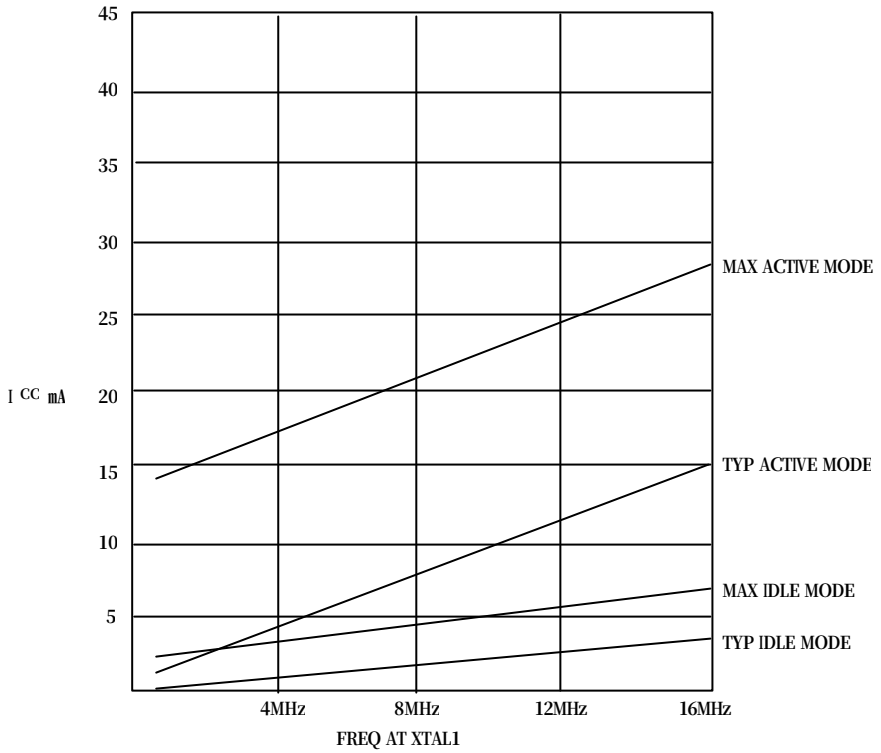


Figure 7. Icc vs. FREQ
Valid only within frequency specifications
of the device under test

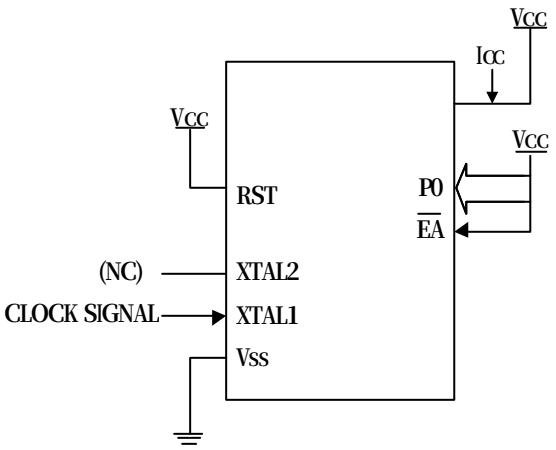


Figure 8. ICC Test Condition, Active Mode
All other pins are disconnected

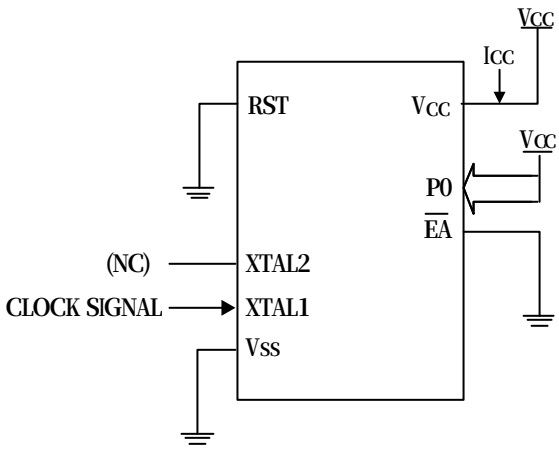


Figure 9. ICC Test Condition, Idle Mode
All other pins are disconnected

Timing Diagram (Continued)

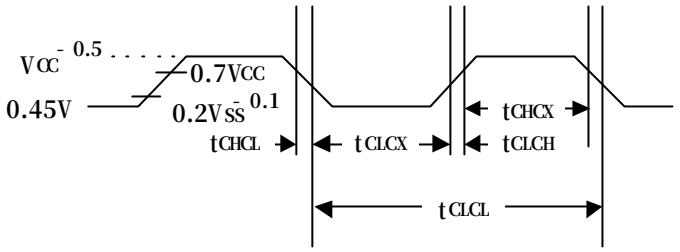


Figure 10. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

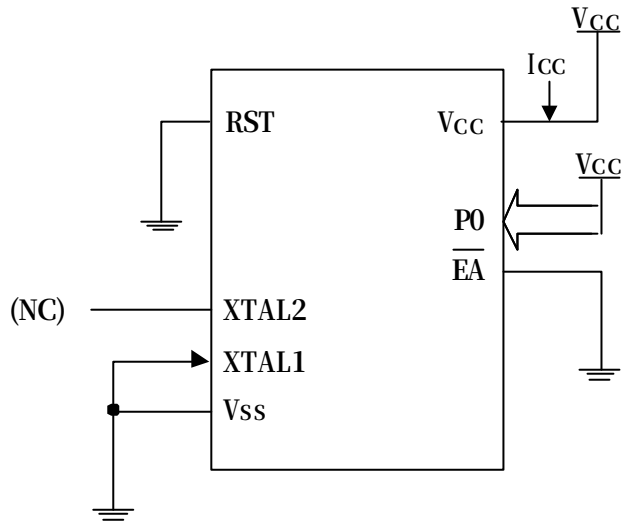


Figure 11. I_{CC} Test Condition, Power down Mode
All other pins are disconnected, V_{CC} = 2V to 5.5V