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INNOVATION

SD705/ SD706/ SD707/ SD708 – INERTIAL MODULE SINGLE AXIS IN PLANE OR OUT OF PLANE GYROSCOPE PRODUCT DATASHEET

Date:	01.10.2010
Revision:	1.9
TYP	Micro-machined Integrated Inertial Module with Single Axis In-Plane or Out-of-Plane Gyroscope
DEVICE NAME	SD705 / SD706/ SD707/ SD708
PACKAGE	QFN 40, 6x6mm

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APPLICATIONS

The high performance level, mechanical robustness and the wide operating temperature range make the SD70x Inertial Module best suitable for several applications like:

- Navigational systems
- Platform stabilization
- High end toys (e.g. helicopters)
- Image stabilization
- Motion control

FEATURES

- Tiny QFN40 package of only 6x6x2 mm³
- Temperature operating range -40°C to +85°C
- Fully calibrated over the whole operating temperature range
- Continuously working self diagnosis
- Sensitive gyroscope axis either in-plane or out-of-plane
- Simultaneously two measurement ranges of ±100°/s and ±300°/s
- Provide over range up to ±128°/s and ±512°/s, respectively
- Available as 3.3V or 5V version

GENERAL DESCRIPTION

The SD70x module integrates a high performance sensor element and a mixed signal ASIC within a 40 pins QFN plastic package. The SD705 and SD707 are sensitive to in plane angular velocities (parallel to the PCB, X-axis), while the SD706 and SD708 are sensitive to out of plane angular velocities (perpendicular to the PCB, Z-axis). The SD705 and SD706 are for 3.3V operation and the SD707 and SD708 for 5V operation.

PART NAME	GYROSCOPE AXIS	SUPPLY VOLTAGE
SD705	X	3.3V
SD706	Z	3.3V
SD707	X	5V
SD708	Z	5V

The sensor element is manufactured in a surface micromachining process and encapsulated in a first level packaging technique. The sensor module provides a digital rate output via an integrated serial peripheral interface (SPI).

The SD70x is designed to provide a high signal-to-noise ratio with excellent performance over temperature. Two measurement ranges are available simultaneously: ±128 °/sec with 10Hz bandwidth and ±512 °/sec with 75Hz bandwidth.

The micro-machined gyroscope element exploits the principle of the Coriolis Effect and a capacitive-based sensing system. Rotation of the sensor around the sensitive axis causes a secondary movement of an oscillating silicon structure resulting in a capacitance change. The ASIC detects and transforms these changes in capacitance into a digital output signal, which is proportional to the angular rate.

The inertial module comes fully calibrated with the calibration data stored in non-volatile memory.

CONTENTS

1. General

1.1. Absolute Maximum Ratings

Stress levels exceeding the values listed here may cause permanent damage to the device.

Environmental Specification

PARAMETER	MIN	MAX	UNIT	CONDITION
SD705, SD706 Supply Voltage	-0.5	4.6	V	
SD707, SD708 Supply Voltage	-0.5	6.0		
Storage temperature	-40	125	° C	
Package Drop Survival (AEC-Q100)		1.2	m	unpowered
SD705, SD707 Mechanical shock survival** half sine according JESD22-B104C		2000	g	unpowered
		1500	g	powered
SD706, SD708 Mechanical shock survival** half sine according JESD22-B104C		TBD	g	unpowered
		TBD	g	powered
ESD*	2		kV	HBM at any pin

* The SD70x Inertial module is rated to 2kV using the Human Body Model (HBM). Although this product features patented or proprietary protection circuitry against electrostatic discharge (ESD) damage may occur if devices are subjected to high-energy ESD pulses. Therefore, proper precaution has to be taken to avoid performance degradation or loss of functionality.

** Drops onto hard surfaces can cause shocks of greater than 2000g and exceed the absolute maximum rating of the device. Care should be exercised in handling to avoid damage.

WARNING!

1.2. Normal Operating Range

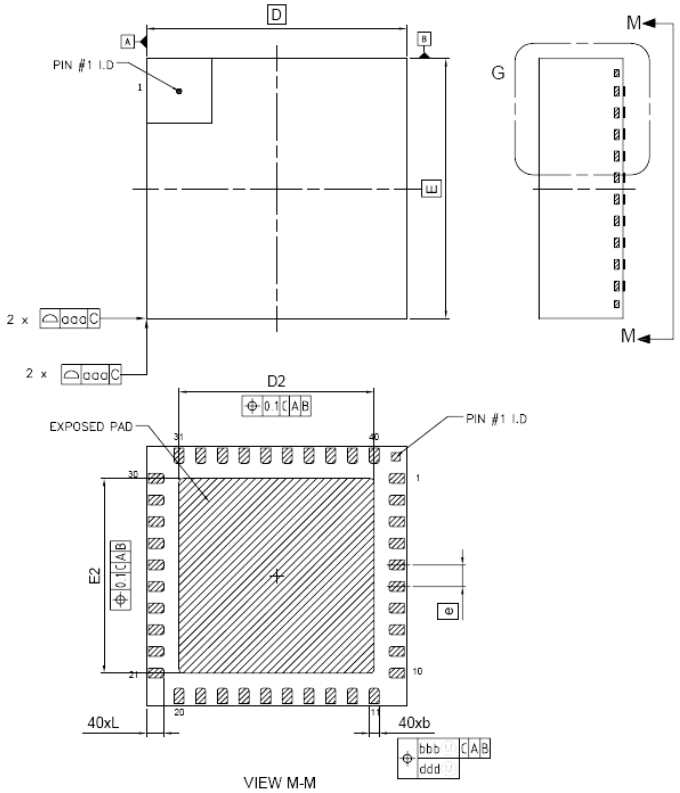
The operation range specifies the electrical and environmental conditions of operation where all specified characteristics have to be fulfilled.

Environmental Specification

PARAMETER	MIN	MAX	UNIT	CONDITION
Ambient temperature	-40	85	° C	
Ambient temperature change rate	-5	5	° C / min	

The minimum operational Lifetime is 17 000 h in powered state, the total Lifetime is minimum 17 years.

1.3. Package



DIM	MIN	NOM	MAX
A	1.93	1.98	2.03
A1	0.00		0.05
A3		0.203 REF	
b	0.18	0.23	0.28
D		6.00 BSC	
E		6.00 BSC	
D2	4.40	4.50	4.60
E2	4.40	4.50	4.60
e		0.50 BSC	
L	0.35	0.40	0.45
L1	0.00		0.10
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

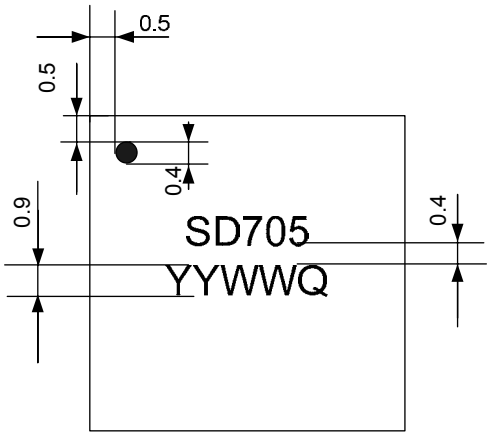
2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

1.4. Marking

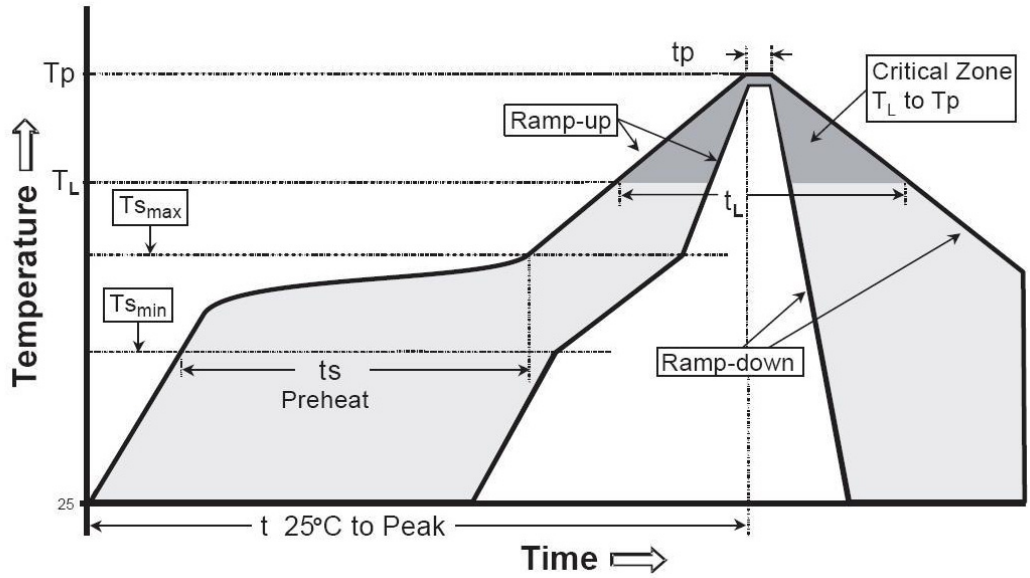


Drawing 1: dimensions and positioning of the marking in mm

FIELD	LINE	DIGITS	FIELD DESCRIPTION	MARKING
●			Pin 1 indicator	
Product No. (SDabc)	1	5	SensorDynamics Product No.	SD705 SD706 SD707 SD708
Date code	2	4	Date Code YYWW	[YYWW]
Manufacturer	2	1	Manufacturer code	

1.5. Reflow Solder Profile

Packaging concept, technology and materials are selected to allow for up to three solder cycles according to lead free solder profile with peak temperature of +245 °C, as described in the figure and tables below.



PROFILE FEATURES	VALUE / CONDITION
Profile type	Pb-free assembly
Average Rump-Up rate (Ts_{max} to Tp)	max 3 °C/s
Preheat	
Temperature min (Ts_{min})	150 °C
Temperature max (Ts_{max})	200 °C
Time (ts)	60-180 s
Time maintained above:	
Temperature min (T_L)	217 °C
Time (t_L)	60-150 s
peak temperature	
Peak/classification temperature (Tp)	245°C
time within 5°C from actual peak temperature (tp)	20-40 s
time above $T_{solidus}$ (min. 217 °C)	min. 90 s
Cooling	
ramp-down rate	max 6 °C/s
General	
time 25 °C to peak temperature	max. 480 s

1.6. Self Diagnosis Concept

The inertial module accomplishes a continuously working self diagnosis of the gyroscope. There is no need to switch to a certain diagnosis mode. If a failure of the gyroscope is detected a dedicated status flag (BIT_N, see section 6.1.2) in the measurement data telegram is set to “1”. If the failure is just temporary, e.g. due to a mechanical shock, the BIT_N is reset to “0” automatically. If the BIT_N remains “1” even after resetting the sensor a permanent damage must be considered.

2. SD705/SD706 Interface definition

2.1. Pin Description

The pin out includes digital/analog supply and ground, digital inputs and outputs for data and test signals. The following schematic depicts the pin assignment of the QFN package.

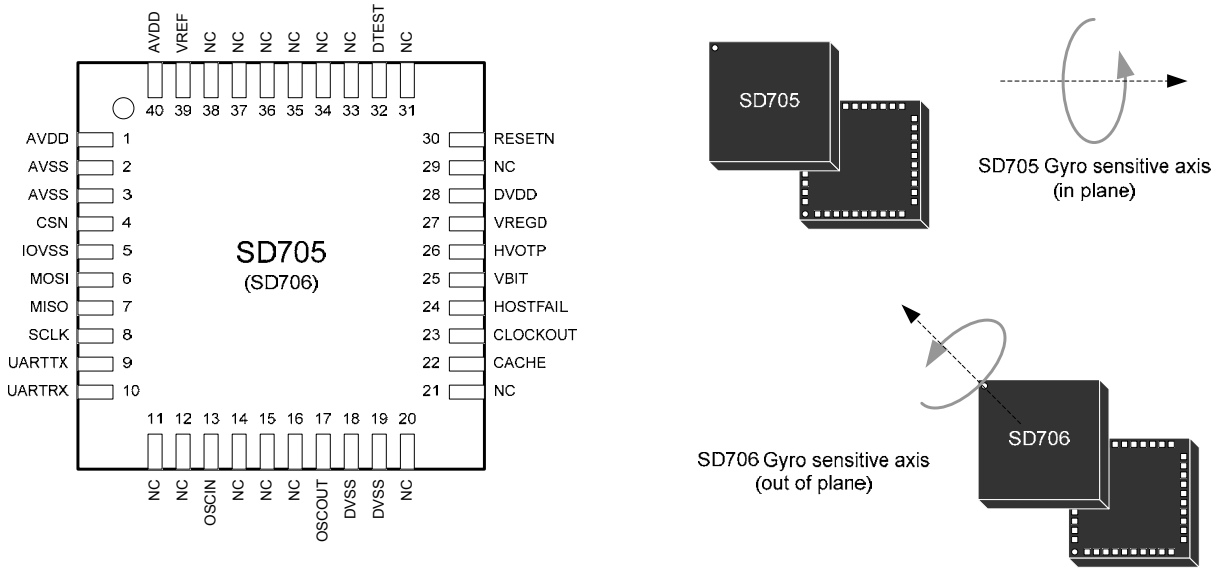


Fig. 2: Pin out of SD705/6 inertial module in QFN package

The pins are assigned according to the following table:

PIN	TYPE	NAME	NOTES
1	S	AVDD	3.3V analog power supply
2, 3	G	AVSS	analog ground
4	I	CSN	SPI interface (Chip Select, active low)
5	G	IOVSS	IO ground
6	I	MOSI	SPI interface (Master Output Slave Input)
7	O	MISO	SPI interface (Master Input Slave Output)
8	I	SCLK	SPI interface (Spi Clock)
9	O	UARTTX	Reserved
10	I	UARTRX	Reserved
11, 12	NC	NC	not connected
13	I, A	OSCIN	Ext. quartz connection or ext. clock input
14-16	NC	NC	not connected
17	A	OSCOUT	Ext. quartz connection
18, 19	G	DVSS	digital ground
20, 21	NC	NC	not connected
22	I/O	CACHE	Reserved
23	O	CLOCKOUT	Clock output (for driving other components)
24	O	HOSTFAIL	Alarm for handshaking with host
25	O	BIT	Built In Test (“high” means all ok)
26	S	HVOTP	Embedded OTP power supply
27	A	VREGD	1.8V regulated voltage, requires 100nF external cap

28	S	DVDD	3.3V digital power supply
29	NC	NC	not connected
30	I	RESETN	Reset_n (active low)
31	NC	NC	not connected
32	I	DTEST	Reserved
33-38	NC	NC	not connected
39	A	VREF	analog voltage reference, requires 100nF external cap
40	S	AVDD	3.3V analog power supply

Legend:

SYMBOL	DESCRIPTION
I	Digital Input
O	Digital Output
I/O	Digital Input/Output
A	Analog
S	Supply
G	Ground
NA	Not applicable
NC*	Not connected

* NC pins are not connected internally. They can be modelled as an open circuit.

2.2. Application Circuit

A few external components are needed as shown in the next picture. The blue capacitors can be omitted if the supply voltage is properly filtered and the supply source has low impedance.

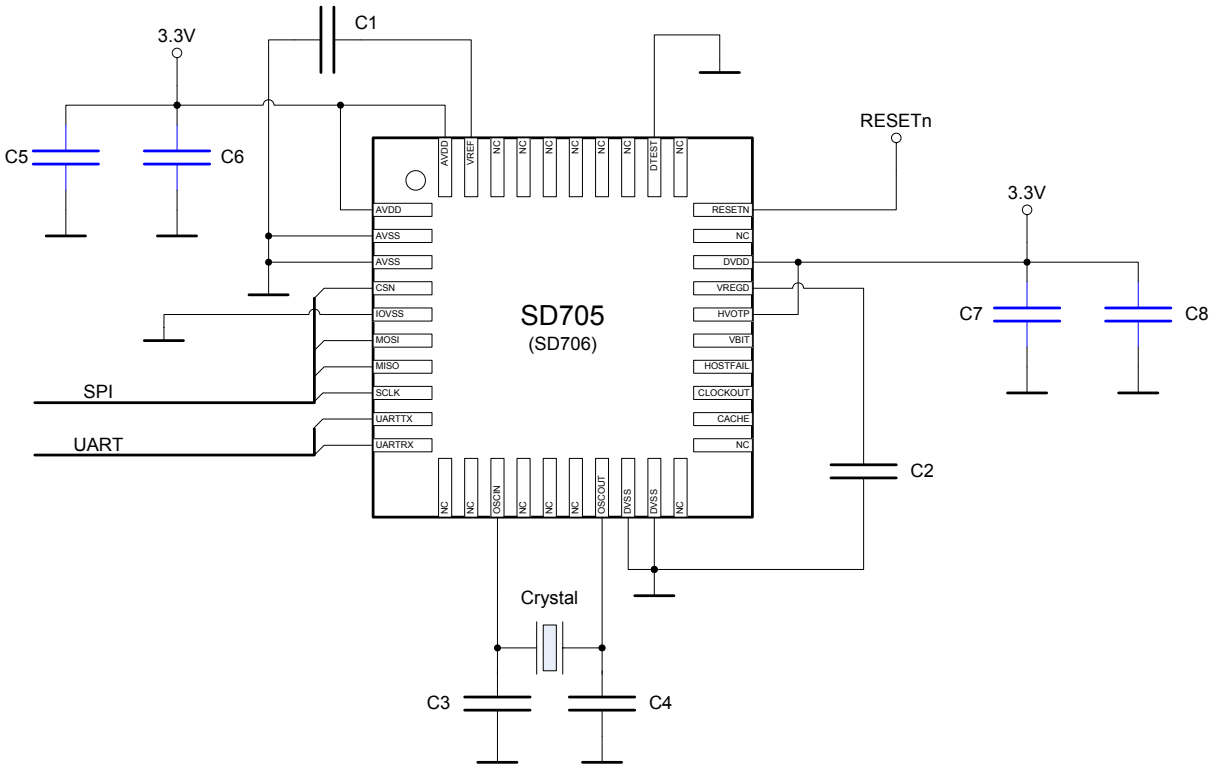


Fig. 3: Application circuit for integrated gyro module SD705/6.

External Components:

#	TYPE	NAME	VALUE	UNIT	NOTES
1	Cap	C1	100	nF	Mandatory.
2	Cap	C2	100	nF	Mandatory.
3	Cap	C3	10	pF	Board parasitic capacitance on OSCIN should be kept below 1pF
4	Cap	C4	10	pF	Board parasitic capacitance on OSCOUT should be kept below 1pF
5	Crystal	CRYSTAL	12.0	MHz	Mandatory. See below for further requirements of quartz crystal.
6	Cap	C5	100	nF	Optional. Required for not stabilized power supplies.
7	Cap	C6	470	pF	Optional. Required for not stabilized power supplies.
8	Cap	C7	470	pF	Optional. Required for not stabilized power supplies.
9	Cap	C8	100	nF	Optional. Required for not stabilized power supplies.

Quartz Crystal Requirements:

PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT	NOTES
ESR	Equivalent Series Resistance			150	Ω	
Cload	Load Capacitance		10	15	pF	
Driving Level	DrvLevel		10		µW	
Fres	Resonant frequency		12.0		MHz	
FreqTol	Frequency Tolerance	-0.3		0.3	%	Maximum over lifetime and temperature

Digital I/O Requirements:

PARAM	DESCRIPTION	MIN	MAX	UNIT	NOTES
Vil	Digital input low voltage level	-0.3	0.8	V	
Vih	Digital input high voltage level	2.0	5.5	V	5V tolerant
Vol	Digital output low voltage level		0.4	V	4mA current for CLOCKOUT, 2mA for the other outputs
Voh	Digital output high voltage level	2.4		V	4mA current for CLOCKOUT, 2mA for the other outputs

Pin 23 CLOCKOUT (digital output)
This Pin is by default disabled (high impedance). It can be enabled at end of production line (OTP) to provide the system clock to an external device.

Pin 24 Host Failure (digital output)
The Inertial Module contains a digital output (HOSTFAIL) for signalling a failure of the host µC detected by intelligent watchdog procedure between inertial module and host µC. Please contact SensorDynamics for more details on the intelligent watchdog functionality.

Pin 25 BIT (digital output)
The Inertial Module contains a digital output (BIT) for signalling an internal failure detected by embedded failsafe checks system. This signal is active low: when BIT voltage is low (Vol) an error is present in the module.

Pin 27 VREGD (analog output)
The Inertial Module generates an internally regulated voltage (1.8V) that requires external filtering by a 100nF capacitance.

Pin 30 RESETN
RESETN is active low. When RESETN is low (Vil) the device is under reset. When RESETN is high (Vih) the device is in functional mode, if powered.

Case 1: customer application needs to reset the device on demand.

In this case RESETN has to be driven by external device/controller.

Case 2: customer application doesn't need to reset the device on demand.

RESETN can be either connected directly to power supply (3.3V) or pulled-up to 3.3V through dedicated resistor. SD705/6 will be automatically reset by internal POR circuitry at every power-up sequence.

Pin 39 VREF (analog output)
The Inertial Module generates an internal voltage reference (1.5V) that requires external filtering by a 100nF capacitance.

3. SD707/8 Interface definition

3.1. Pin Description

The pin out includes digital/analog supply and ground, digital inputs and outputs for data and test signals. The following schematic depicts the pin assignment of the QFN package.

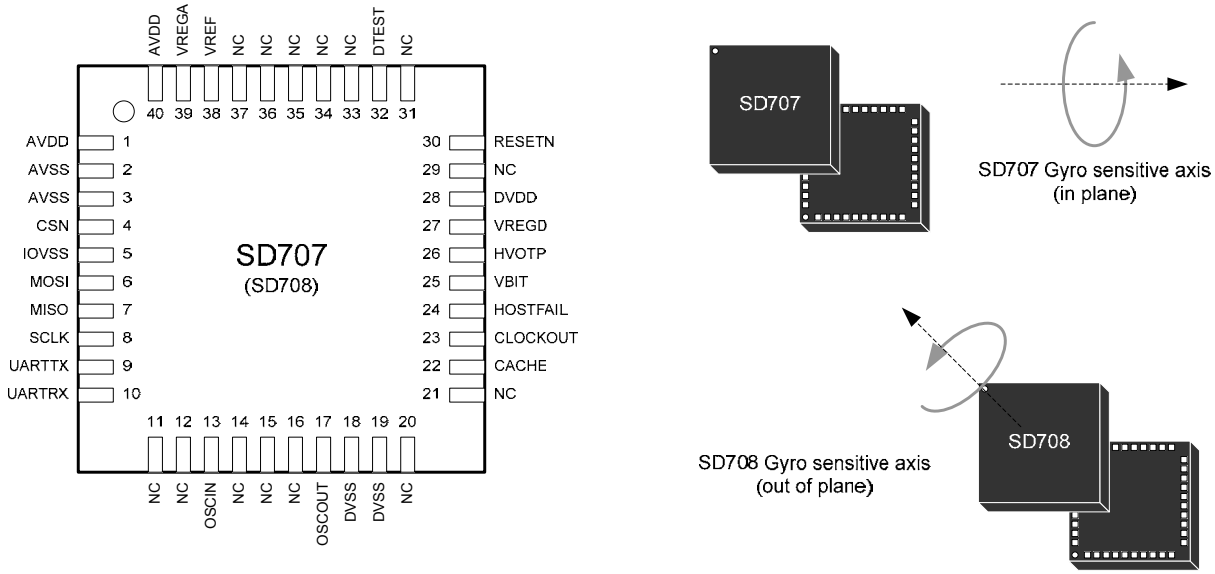


Fig. 4: Pin out of SD707/8 inertial module in QFN package

The pins are assigned according to the following list:

PIN	TYPE	NAME	NOTES
1	S	AVDD	3.3V analog power supply
2, 3	G	AVSS	analog ground
4	I	CSN	SPI interface (Chip Select, active low)
5	G	IOVSS	IO ground
6	I	MOSI	SPI interface (Master Output Slave Input)
7	O	MISO	SPI interface (Master Input Slave Output)
8	I	SCLK	SPI interface (Spi Clock)
9	O	UARTTX	Reserved
10	I	UARTRX	Reserved
11, 12	NC	NC	not connected
13	I, A	OSCIN	Ext. quartz connection or ext. clock input
14-16	NC	NC	not connected
17	A	OSCOUT	Ext. quartz connection
18, 19	G	DVSS	digital ground
20, 21	NC	NC	not connected
22	I/O	CACHE	Reserved
23	O	CLOCKOUT	Clock output (for driving other components)
24	O	HOSTFAIL	Alarm for handshaking with host
25	O	BIT	Built In Test (“high” means all ok)
26	S	HVOTP	Embedded OTP power supply
27	A	VREGD	1.8V regulated voltage, requires 100nF external cap
28	S	DVDD	3.3V digital power supply

29	NC	NC	not connected
30	I	RESETN	Reset_n (active low)
31	NC	NC	not connected
32	I	DTEST	Reserved
33-37	NC	NC	not connected
38	A	VREF	Analog regulator output, requires 100nF external cap
39	A	VREGA	5V regulated voltage, requires 100nF external cap
40	S	AVDD	3.3V analog power supply

Legend:

SYMBOL	DESCRIPTION
I	Digital Input
O	Digital Output
I/O	Digital Input/Output
A	Analog
S	Supply
G	Ground
NA	Not applicable
NC*	Not connected

* NC pins are not connected internally. They can be modeled as an open circuit.

3.2. Application Circuit

A few external components are needed as shown in the next picture. The blue capacitors can be omitted if the supply voltage is properly filtered and the supply source has low impedance.

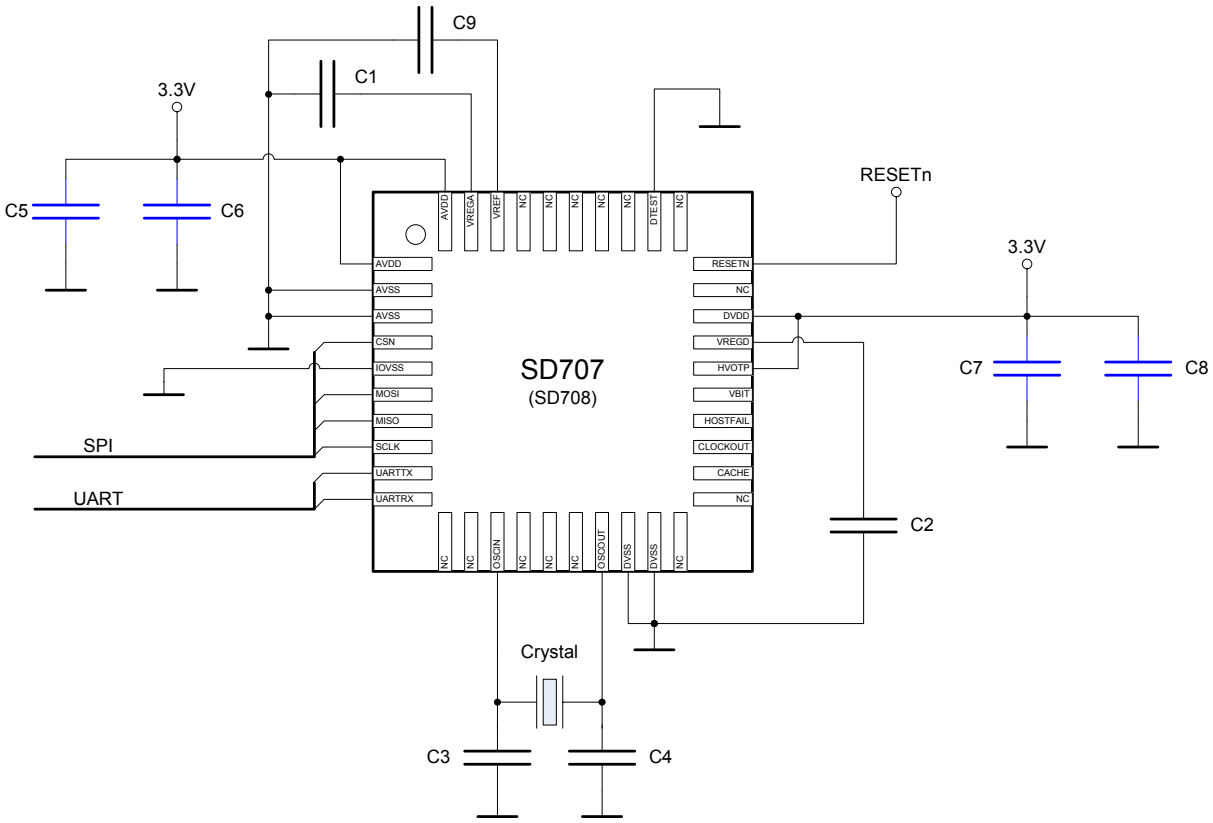


Fig. 5: Application circuit for integrated gyro module SD707/8.

External Components:

#	TYPE	NAME	VALUE	UNIT	NOTES
1	Cap	C1	100	nF	Mandatory.
2	Cap	C2	100	nF	Mandatory.
3	Cap	C3	10	pF	Board parasitic capacitance on OSCIN should be kept below 1pF
4	Cap	C4	10	pF	Board parasitic capacitance on OSCOUT should be kept below 1pF
5	Crystal	CRYSTAL	12.0	MHz	Mandatory. See below for further requirements of quartz crystal
6	Cap	C5	100	nF	Optional. Required for not stabilized power supplies.
7	Cap	C6	470	pF	Optional. Required for not stabilized power supplies.
8	Cap	C7	470	pF	Optional. Required for not stabilized power supplies.
9	Cap	C8	100	nF	Optional. Required for not stabilized power supplies.
10	Cap	C9	100	nF	Mandatory.

Quartz Crystal Requirements:

PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT	NOTES
ESR	Equivalent Series Resistance			150	Ω	
Cload	Load Capacitance		10	15	pF	
Driving Level	DrvLevel		10		µW	
Fres	Resonant frequency		12.0		MHz	
FreqTol	Frequency Tolerance	-0.3		0.3	%	Maximum over liferime and temperature

Digital I/O Requirements :

PARAMETER	DESCRIPTION	MIN	MAX	UNIT	NOTES
Vil	Digital input low voltage level	-0.3	1	V	
Vih	Digital input high voltage level	4	5.5	V	
Vol	Digital output low voltage level	-	0.4	V	4mA current for CLOCKOUT, 2mA for the other outputs
Voh	Digital output high voltage level	4.4	-	V	4mA current for CLOCKOUT, 2mA for the other outputs

Pin 23 CLOCKOUT (digital output)
This Pin is by default disabled (high impedance). It can be enabled at end of production line (OTP) to provide the system clock to an external device.

Pin 24 Host Failure (digital output)
The Inertial Module contains a digital output (HOSTFAIL) for signalling a failure of the host µC detected by intelligent watchdog procedure between inertial module and host µC. Please contact SensorDynamics for more details on the intelligent watchdog functionality.

Pin 25 BIT (digital output)
The Inertial Module contains a digital output (BIT) for signalling an internal failure detected by embedded failsafe checks system. This signal is active low: when BIT voltage is low (Vol) an error is present in the module.

Pin 27 VREGD (analog output)
The Inertial Module generates an internally regulated voltage (1.8V) that requires external filtering by a 100nF capacitance.

Pin 30 RESETN
RESETN is active low. When RESETN is low (Vil) the device is under reset. When RESETN is high (Vih) the device is in functional mode, if powered.

Case 1: customer application needs to reset the device on demand.

In this case RESETN has to be driven by external device/controller.

Case 2: customer application doesn't need to reset the device on demand.

RESETN can be either connected directly to power supply (3.3V) or pulled-up to 3.3V through dedicated resistor. SD707/8 will be automatically reset by internal POR circuitry at every power-up sequence.

Pin 38 VREF (analog output)
The Inertial Module generates an internal voltage reference (1.5V) that requires external filtering by a 100nF capacitance.

Pin 39 VREGA (analog output)
The Inertial Module generates an internally regulated voltage (3.3V) that requires external filtering by a 100nF capacitance.

4. Clock source

4.1. General

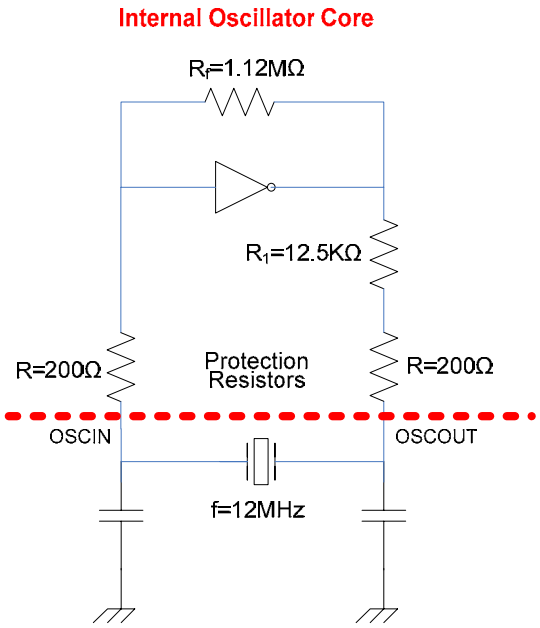
SD recommends using a 12 MHz quartz for SD705/6/7/8 as indicated in the application circuits. Alternatively an external 12 MHz ceramic resonator can be used instead of the quartz:

Ceramic resonator requirements

PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT	NOTES
ESR	Equivalent Series Resistance			150	Ω	Also specified as Resonant Impedance
Cload	Load Capacitance		10	15	pF	Additional capacitor not required if the load capacitor embedded in the ceramic resonator component

4.2. Internal oscillator circuit schematic

The following figure shows a schematic diagram of the internal oscillator circuit implemented in SD705 and SD706 products, with the indication of the nominal values of the resistances.



A maximum tolerance of 20% has to be considered for the actual value of the internal resistances.

5. Electrical and Physical Characteristics

5.1. Operation and performance parameters

Operation Specification

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Supply voltage SD705, SD706	3.1		3.5	V	
Supply voltage SD707, SD708	4.75		5.25	V	
Supply current SD705, SD706		16		mA	
Supply current SD707, SD708		18		mA	
Start up time			400	ms	incl. Start up checks
SPI Communication Speed	100		10000	kHz	64 bits telegram (see appendix)
Total mass			0.2	grams	

Gyro Performance Specification *

PARAMETER	MR1	MR2	UNIT	CONDITION
Measurement range	± 100	± 300	°/s	
Resolution	0.0039	0.0156	(°/s)/LSB	true 16 bit
RMS noise	0.07	0.2	°/s	typical
Bandwidth (-3dB)	10	75	Hz	± 25%
Zero rate bias	0 ± 0.5		°/s	typical
Temperature drift zero rate bias	± 2		°/s	typical
Sensitivity error	± 2.5		%	typical over temp
Linearity error	± 1		%	versus best fit
Micro linearity	± 10		%	
Cross Axis Sensitivity	± 2.0		%	against angular rates about other axes
In run drift of rate bias	± 1		°/s	during 5 min after start-up at RT
Digital value range	± 128	± 512	°/s	16 bit message
Total zero rate error	± 3.0		°/s	
Zero rate temperature drift velocity	± 0.2		(°/s) / min	± 5 K/min maximum temperature shift
Phase response @ 5 Hz	-18		°	
Signal Update time	1		ms	SPI message

PARAMETER	MR1	MR2	UNIT	CONDITION
Acceleration Cross Sensitivity	0.1		°/s/g	during/after 10 ms half-sine: @ 10g, 25g, 50g,100g
Output value on over-range	± 128	± 512	°/s	
Recovery time after over-range	50		ms	normal operation after 300 °/s for MR1 and 900 °/s for MR2
Recovery time after shock	5		ms	For shocks up to 50g, 10 ms
Temperature signal tolerance	± 10		K	SPI message

* The figures in the table are for nominal supply voltage (3.3V for SD705/706 and 5V for SD707/708)

Definitions and Explanations:

Supply Current

The specified value represents the maximum current consumption under all operating conditions. Its value is given by the sum of the currents going through the pins AVDD and DVDD.

Startup time

The startup time is the elapsed time between power up (reset) and the transition to locked status.

Measurement Range

The measurement range is the range of rotation conditions where the module works according to the specified performance.

Resolution

The physical resolution is the minimum representable value.

RMS noise

Standard deviation of the rate output, computed on at least 500 readings, collected on a time interval of 5s, with zero input rate applied, and according to the formula:

$$OutputNoise = \sqrt{\frac{1}{N}\sum_{1}^{N}\left(OutputSignal - \overline{OutputSignal}\right)^2}$$

where $N \geq 500$ and $\overline{OutputSignal}$ denotes the average over all collected samples of the rate output signal.

Noise density

The noise density is the spectral density at a given frequency, measured with a filter of 1 Hz noise bandwidth. Given the RMS noise as defined above, the noise density is given by:

$$Dnoise = OutputNoise / \sqrt{Filter\_band}$$

where $Filter\_band$ is the bandwidth in Hz of the relevant filter.

Bandwidth

The bandwidth is the frequency at which the output rate is attenuated by -3dB compared to the DC value. The bandwidth is programmable at ROM level.

Zero rate bias

Maximum deviation from zero rate output signal at zero physical input rate, acceptable after calibration at RT (= 25 °C ±5 °C) and after the manufacturing process (populating, soldering). The bias is computed as the average of at least 500 samples, collected after the signal is valid for 5 sec.

Temperature drifts zero rate bias

Maximum deviation of rate output at zero physical input rate over the full temperature range. The bias is computed as the average of at least 500 samples, collected after the signal is valid for 5 sec.

Sensitivity error

The sensitivity error is the maximum deviation between ideal sensitivity and the linear best fit measured in 5°/s steps from Ω_{min} to Ω_{max} (-100 °/s to + 100°/s) for MR1, respectively measured in 20°/s steps from Ω_{min} to Ω_{max} (-300 °/s to + 300 °/s) for MR2. For both ranges the sensitivity error is given by the following formula:

$$SensError = 100 \bullet \left(\frac{Slope_{computed}}{Slope_{ideal}} - 1 \right)$$

where $Slope_{ideal} = 1$.

Linearity error

The linearity error is the maximum deviation of the rate measured between (-100 °/s to + 100°/s) in 5°/s steps (resp. between -300 °/s to + 300 °/s in 20°/s steps for MR2) from the value obtained by linear best fit, divided by Ω_{max} = 100 °/s (resp. Ω_{max} = 300 °/s for MR2):

$$Le = Max\left\{ \frac{YR(\Omega_i) - YR_{best\_fit}(\Omega_i)}{\Omega_{\max}} \middle| \Omega_i \in \left\{ -\Omega_{\max}, -\Omega_{\max} + step°/s, ..., \Omega_{\max} - step°/s, \Omega_{\max} \right\} \right\} \bullet 100$$

Cross axis sensitivity

This is the sensitivity of the module to angular rates applied to the non-sensitive axes, which are perpendicular to the sensitive axis and where the module is mounted with negligible angle error to a defined reference mark of the housing. The cross axis sensitivity is then defined as the percentage of the off-axis input rate around (along) the non-sensitive axes seen at the output. The specified limit refers to an applied rate of ±900°/s.

Signal update time

The signal update time is the time elapsed between the start of one data transmission and the next. The specified value is guaranteed by design. Note: data transmission time must be much shorter than the signal update time (see SPI communication speed limits in the table above).

Temperature Signal Tolerance

The temperature signal is provided by a silicon temperature sensor integrated into the ASIC. The temperature signal tolerance indicates the maximum error between the environment temperature and the temperature of the silicon.

Micro linearity

The micro linearity MLe error is the maximum deviation of the gradient between two adjacent rates from the gradient $Slope_{best\_fit}$ of the linear best fit $YR_{best\_fit}(\cdot)$

$$MLe = Max\left\{ \frac{YR(\Omega_i + step°/s) - YR(\Omega_i)}{step°/s \bullet Slope_{best\_fit}} - 1 \middle| \Omega_i \in \left\{ -\Omega_{\max}, -\Omega_{\max} + step°/s, ..., \Omega_{\max} - step°/s \right\} \right\} \bullet 100$$

Recovery time after over-range

The recovery time is the time elapsed between the instant when the physical applied rate enters the measurable range (from an out of range value) and the time when the circuit delivers a rate output value within specifications.

In-run drift of rate bias

This is the maximum drift of the rate output within the first 5 minutes after power-on at constant ambient temperature and zero rate applied, compared to the bias value measured at the end of the startup. During these 5 min, the rate output is recorded at intervals of 10ms or less and the bias is computed using a moving average of 128 samples.

Zero rate temperature drift velocity

Maximum rate drift under worst case temperature change 5 K/min, i.e. at maximum heat up or cool down rate.

Total zero rate error

Maximum deviation of zero rate output at zero physical input rate including all errors from temperature, power supply, ageing, and other.

Phase response

This parameter refers to the maximum phase shift between physical input rate (sinusoidal signal with 5Hz frequency) and the corresponding output rate signal.

Additional phase shifts due to communication time via SPI (and additionally e.g. CAN in the application) have to be taken into consideration.

Output value on over-range

Under applied physical angular rates exceeding the specified range, the value of the rate output saturates at the maximum value (±128°/s for MR1 and ±512°/s for MR2, with the sign depending on the direction of the rate applied) and stays in saturation up to physical rates of ± 900 °/s.

Recovery time after shock

The recovery time after shock defines the maximum time allowed to the gyro module to return in normal operating conditions, after the decay of a half-sine shock excitation of 50g amplitude and 10ms duration. The “normal operating conditions” is the state in which all the module parameters are in agreement with the present specification.

Acceleration cross sensitivity / vibration susceptibility

To avoid erroneous output signals under automotive operation conditions, the gyro module offers special shock and vibration resistivity. The requirements are based on the ISO standard 16750-3 for passenger cars. The power spectral density of the relevant vibration on gyro module level is given by

f / Hz	g² / Hz
10	0.21
55	0.21
1000	0.015

As equivalent total acceleration 6.9 g is assumed. The signal deterioration does not exceed ± 2 °/s offset shift and 1.5 °/s rms noise level under these vibration levels.

In the frequency range 0 Hz to 10 kHz the acceleration cross sensitivity of the sensor element is less than 0.01 (°/s)/(m/s²) for static and dynamic accelerations.

Acceleration cross sensitivity / Shock sensitivity

The acceleration cross sensitivity limits the maximum allowed rate output change related to static and dynamic linear accelerations. It is defined as the rate output change divided by the applied acceleration amplitudes for the defined test shock pulses with half sine waves of 10 ms duration and with amplitudes of 10 g, 25 g, 50 g, and 100 g.

No sticking effects of the moving MEMS structures occur under high shock levels like direct impact or drop from 1.2m onto concrete floor according to the standard automotive drop test requirements.

6. SPI Communication

6.1. General information

The SD70x SPI communication channel allows the host to get information of various types from the ASIC. Physical settings of the communication need phase to be set to 1 and polarity to 0. Some more words about phase and polarity can be found at the end of this document. The SPI communication is managed according to a master-slave paradigm where the host always acts as the master and the ASIC as the slave. The SPI communication must conform to a protocol obeying to the following rules:

- The communication can be thought as based on a per-session mode: the master (host) starts a session by sending a message to the slave (ASIC) which in turn replies with the answer related to the query received in the previous session. The very first answer - since can not rely on a previous one - is simply the state (see below) of the ASIC. The ASIC answer ends the session.
- All messages (in both directions) are fixed size (64 bits);
- All messages (in both directions) are formatted accordingly to the following overall structure:

General message structure

Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0
Hinfo1	Hinfo2	Payload					Tinfo

- Bit-order: bit 63 is the first one sent, bit 0 the last one.
- Hinfo1, Hinfo2 and Tinfo are mandatory fields for all message types. Payload is the portion specifically arranged for any particular message.

6.1.1. Hinfo1

Hinfo1 content adheres to the following structure:

Command sent by the Host

Hinfo1 (RX by SPI Interface)

bit 7	*bit 6*	*bit 5*	*bit 4*	*bit 3*	*bit 2*	*bit 1*	*bit 0*
Acnt			Opcode				

Acnt is a counter incremented by 1 at each sent telegram. Its value can be checked by the ASIC. The host must increment this value every telegram sending (modulo 8: after "111" the counter restarts from 0).
Opcode: This field tells the ASIC which action has to be performed (it is the command code).

Answer sent by the ASIC

Hinfo1 (TX by SPI Interface)

bit 7	*bit 6*	*bit 5*	*bit 4*	*bit 3*	*bit 2*	*bit 1*	*bit 0*
Acnt			Opcode				
HW			*HW(STATB, RATE) or Register(iWDOGB, DIAGB)*				

Acnt: this value is incremented modulo 8 every telegram sending.
Opcode: The value of this field is the opcode of the telegram which this answer is related to.

6.1.2. Hinfo2

For the purposes of this document, the host has not to take care of this field (it can be filled with 0).
Hinfo2 content from the ASIC adheres to the following structure:

Answer sent by the ASIC

Hinfo2 (TX by SPI Interface)							
bit 7	*bit 6*	*bit 5*	*bit 4*	*bit 3*	*bit 2*	*bit 1*	*bit 0*
BIT_N	LMS	Diag_Buf_valid	iWD	WARN	SW status		
Input	*HW*	*HW*	*reserved*	*reserved*	*APB register/HW*		

Here is a summarized description of the fields as filled by the ASIC. It is beyond the purposes of this document to deeply explain the meaning of each field.

BIT_N	Set by the hardware. BIT_N=0 no internal failure (Physical pin BIT=1). BIT_N=1 internal failure (Physical pin BIT=0).
LMS	Set by the hardware. LMS=1 CRC or Frame error in previous telegram. LMS=0 no errors in previous telegram.
Diag_Buf_valid	Set by the hardware. Reserved.
iWD	Set by the hardware. Reserved.
WARN	Set by the hardware. Reserved
SW status	Current status of the software application. Possible status values are reported in the table below

SW Status	Value	Description
InitMode	0x00	System initialization phase. Check of self diagnosis functions started. SPI SW commands not available. BIT_N is forced to 1 (fail); rate values are not meaningful.
ReadyForSpi	0x01	All SPI commands available. BIT_N is forced to 1 (fail); rate values are not meaningful.
ReadyForFsEnable	0x02	Check of self diagnosis functions completed. Agc/pll lock still not reached. BIT_N is forced to 1 (fail); rate values are not meaningful.
NormalMode	0x03	First agc/pll lock reached. BIT_N is "0" if the self-diagnosis does not detect any failure. Rate values are valid if BIT_N = 0.
Rreserved	0x04	-
Reserved	0x05	-
Overrun error	0x06	This value is directly imposed by the hardware in case of SPI overrun errors (a SW command has been received too early, while previous SW command was still in progress, so it will be ignored).
ResetOngoing	0x07	The ASIC is going to perform an auto-reset in no more than 25 ms.

6.1.3. Tinfo

Tinfo contains the cyclic redundancy (CRC) code of the telegram. The host and the ASIC use the same algorithm to compute the CRC. The algorithm used is explained near the end of this document.

6.2. ReadRate Opcode (0x01)

This command is used to get rate and temperature values from the ASIC.

Command sent by the Host

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	Reserved	Reserved	Reserved	Reserved	Reserved	Tinfo

All 'Reserved' fields can be filled with 0es.
Example of a rate telegram (bytes are space separated and in hexadecimal format):
21 00 00 00 00 00 00 38

Answer sent by the ASIC

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	Temp	RateMR1 MSB	RateMR1 LSB	RateMR2 MSB	RateMR2 LSB	Tinfo

Temp type is an unsigned integer over 8 bits. It reports the temperature in °C (T°) according to the following formula:

$$T° (°C) = Temp - 80\ °C$$

RateMR1/ RateMR2 are signed integers over 16 bits. They report the angular speed in °/s, according to the following formulas:

$$RateMR1 (°/s) = RateMR1 / 256$$
$$RateMR2 (°/s) = RateMR2 / 64$$

6.3. ReadStatus Opcode (0x02)

This command is used to get the current status of the self-diagnosis..

Command sent by the Host

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	Reserved	Reserved	Reserved	Reserved	Reserved	Tinfo

All 'Reserved' fields can be filled with 0es.
Example of a status telegram (bytes are space separated and in hexadecimal format):
02 00 00 00 00 00 00 B0

Answer sent by the ASIC

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	StatusInfo				HWInfo (reserved)	Tinfo
		MSB	...	...	LSB		
	StatusInfo bits	31 ... 24	23 ... 16	15 ... 8	7 ... 0		

StatusInfo is an unsigned integer over 32 bits. The *StatusInfo* bits are related to the current status (real-time) of the internal self-diagnosis functions. The meaning of the status bits is listed in the following table:

	Bit position in SPI telegram 0x02	Bit position in 32-bits Status Info word	short bit name	Event source description	example in alarm word
HW sources	16	0	-	*reserved*	0x00000001
	17	1	-	*reserved*	0x00000002
	18	2	-	*reserved*	0x00000004
	19	3	-	*reserved*	0x00000008
	20	4	-	*reserved*	0x00000010
	21	5	-	*reserved*	0x00000020
	22	6	-	*reserved*	0x00000040
	23	7	pll_fail	PLL_lock_error	0x00000080
	24	8	-	*reserved*	0x00000100
	25	9	agc_fail	AGC_lock_error	0x00000200
	26	10	-	*reserved*	0x00000400
	27	11	-	*reserved*	0x00000800
	28	12	-	*reserved*	0x00001000
	29	13	-	*reserved*	0x00002000
	30	14	-	*reserved*	0x00004000
	31	15	-	*reserved*	0x00008000
	32	16	-	*reserved*	0x00010000
	33	17	-	*reserved*	0x00020000
	34	18	-	*reserved*	0x00040000
SW sources	35	19	-	*reserved*	0x00080000
	36	20	-	*reserved*	0x00100000
	37	21	otp_fail	*OTP check routine*	0x00200000
	38	22	-	*reserved*	0x00400000
	39	23	-	*reserved*	0x00800000
	40	24	-	*reserved*	0x01000000
	41	25	-	*reserved*	0x02000000
	42	26	-	*reserved*	0x04000000
	43	27	-	*reserved*	0x08000000
	44	28	-	*reserved*	0x10000000
	45	29	-	*reserved*	0x20000000
	46	30	-	*reserved*	0x40000000
	47	31	-	*reserved*	0x80000000

Example of answer from the ASIC
82 03 02 00 00 00 50 D1

6.4. AsicOperation Opcode (0x0B)

This is the general telegram format that can be used for several subcommands, obtained by specifying different action types.

Command sent by the Host

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	ActionType	...	...	...	...	Tinfo

ActionType: one of the following available actions

Action Type	Short name	Description
0x00	*ReadSysParam*	*Reserved for production tests.*
0x01	*ReadOtp*	*Reserved for production tests.*
0x30	*ReadVersionInfo*	Read version information.
0x40	*Reserved*	*Reserved*
0x50	*Reserved*	*Reserved*
0x70	*SetSpiPhPo*	Set new phase and polarity for the SPI interface
0x80	*TriggerReset*	Trigger an auto-reset of the asic in the next 25 ms.

The meaning of the other bytes is related to the action type. Telegram format for each different action type is detailed after this general format description.

Answer sent by the ASIC

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	ActionType Echo	...	...	...	...	Tinfo

ActionTypeEcho: echo of the *ActionType* related to this answer.
The meaning of the other bytes is related to the action type. Telegram format for each different action type is detailed after this general format description.

6.4.1. AsicOperation (0x30): ReadVersionInfo (action type 0x30)

This command is used to read the values of several identifiers related to the version of HW and SW. The details are shown in the table below. Some of the following entries are intended for production/debug only and are not detailed here.

Offset	Short name	Description
0	*Sysparam_layout_id*	Value of SYSPARAM_LAYOUT_ID system parameter
1	*Sysparam_family_id*	Value of SYSPARAM_FAMILY_ID system parameter
2	*Sysparam_sub_id*	Value of SYSPARAM_SUB_ID system parameter
3	*Filter_version_id*	Version of the dspbank config file
4	*Asic_redo_id*	Asic identifier embedded in the ASIC hardware.
5	*App_name_id*	Firmware application identifier

6	*App_primary_id*	Firmware application primary ID
7	*App_secondary_id*	Firmware application secondary ID
8	*Module_id byte 0 (msb)*	Module ID identifier
9	*Module_id byte 1*	
10	*Module_id byte 2*	
11	*Module_id byte 3 (lsb)*	
12	*Trimming_version_id*	Trimming firmware version

Command sent by the Host

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	0x30	Offset		Reserved	Reserved	Tinfo
			msb	lsb			

Offset is the 16 bits start address offset of the version bytes to be read (related to the beginning of the internal xdata variable that hosts all the version data structure).
All 'Reserved' fields can be filled with 0es.

Example of a ReadVersionInfo telegram (bytes are space separated and in hexadecimal format):
0B 00 30 00 08 00 00 1C

Answer sent by the ASIC

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	0x30	Version byte [Offset]	Version byte [Offset+1]	Version byte [Offset+2]	Version byte [Offset+3]	Tinfo

Version bytes are 4 bytes from the internal version data structure.
Note: only the values related to the version data reported in the table are meaningful. Values related to offsets greater than the dimension of version data structure are undefined and can be ignored.

Example of answer from the ASIC
CB 23 30 00 00 01 22 7C

6.4.2. AsicOperation (0x0B): SetSpiPhPo (action type 0x70)

This command is used to change on the fly the phase and polarity (Ph/Po) settings of the ASIC SPI interface. Request telegram (containing MOSI command) must be exchanged with the current (old) settings, while answer telegram (containing MISO answer) must be exchanged using the new settings.
Note: the required PH-PO settings can be directly programmed into OTP parameters, so this command should not be needed. Anyway it is provided for more complex situations where the host wants to decide at run-time which are the preferred settings to be used.

Command sent by the Host

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	0x70	0x2B	0xCA	PhPo	Reserved	Tinfo
			ActionKeyPhPo				
			msb	lsb			

ActionKeyPhPo is the 16 bits key that must be provided to prevent unintentional Ph/Po changes. The expected key is 0x2BCA. In case of different key value the command will be rejected and the Ph-Po settings will not be changed.

PhPo: Bit 1 : SPI phase (0=sample on first edge, 1=sample on second edge)
Bit 0 : SPI polarity (logic value of SCLK when idle)
See dedicated section about SPI phase and polarity.

All 'Reserved' fields can be filled with 0es.

Example of a SetSpiPhPo telegram (bytes are space separated and in hexadecimal format):
0B 00 70 2B CA 02 00 D4

Answer sent by the ASIC

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	0x70	ActionKeyPhPoEcho		CurrPhPo	Reserved	Tinfo
			msb	lsb			

ActionKeyPhPoEcho is the echo of the 16 bits key received in the MOSI command.
CurrPhPo are the current (new) settings of SPI phase and polarity after the execution of this command (same format as PhPo above)
Example of answer from the ASIC
CB 23 70 2B CA 02 00 49

6.4.3. AsicOperation (0x0B): TriggerReset (action type 0x80)

This command is used to trigger an auto-reset of the ASIC. The auto reset will occur from 0ms to 25 ms after receiving the command, and will be performed only if the action key matches the expected value.
If the auto-reset command is accepted, the Hinfo2 status is set to 0x07 (*ResetOngoing*); then it will restart from 0x00 after reset.

Command sent by the Host

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	0x80	0xE1	0x64	Reserved	Reserved	Tinfo
			ActionKeyReset				
			msb	lsb			

ActionKeyReset is the 16 bits key that must be provided to prevent unintentional resets. The expected key is 0xE164. In case of different key value the command will be rejected and no auto-reset will be performed.
All 'Reserved' fields can be filled with 0es.

Example of a TriggerReset telegram (bytes are space separated and in hexadecimal format):
0B 00 80 E1 64 00 00 3C

Answer sent by the ASIC

byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	0x70	ActionKeyResetEcho		Reserved	Reserved	Tinfo
			msb	lsb			

ActionKeyResetEcho is the echo of the 16 bits key received in the MOSI command.
Example of answer from the ASIC
CB 27 80 E1 64 00 00 A4

6.5. ReadDiagBuf Opcode (0x0D)

This command is used to get the content of the diagnostic buffer, i.e. the answer of a previously sent software command.

Command sent by the Host

Byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	Reserved	Reserved	Reserved	Reserved	Reserved	Tinfo

All 'Reserved' fields can be filled with 0es.
Example of a ReadDiagBuf telegram (bytes are space separated and in hexadecimal format):
2D 00 00 00 00 00 00 83

Answer sent by the ASIC

Byte 7	byte 6	byte 5	byte 4	byte 3	byte 2	byte 1	byte 0
63 ... 56	65 ... 48	47 ... 40	39 ... 32	31 ... 24	23 ... 16	15 ... 8	7 ... 0
Hinfo1	Hinfo2	DiagBuf [47..40]	DiagBuf [39..32]	DiagBuf [31..24]	DiagBuf [23..16]	DiagBuf [15..8]	Tinfo

DiagBuf contains the answer to the previous software command (if ready and still not sent to the host). If the answer has been already sent in the telegram just after the software command, *DiagBuf* is replaced with the ReadStatus answer (see examples on section about SPI command types)

6.6. SPI commands types

All the previously described SPI commands can be grouped in two types, with different timing constraints.

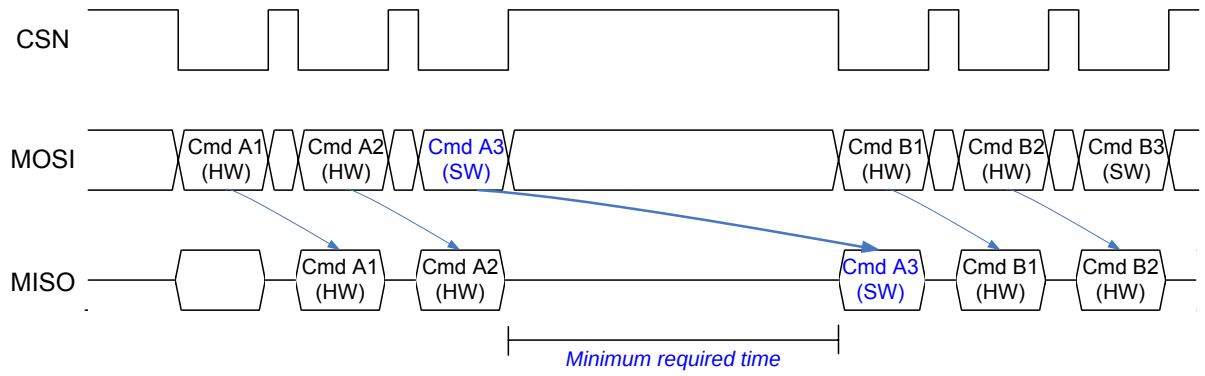
MNEMONIC	OPCODE	TYPE	INTERNAL ANSWER CREATION TIME
ReadRate	0x01	Hardware Command	Immediate
ReadStatus	0x02		
ReadDiagBuf	0x0D		
AsicOperation	0x0B	Software Command low priority	≤ 5.0 ms

Timing constraints for a single SPI telegram are specified in section 5.10.
For hardware command types, no further timing constraints have to be considered.
For software command types (i.e. *AsicOperation)*, an additional constraint is the time needed by the software to prepare the answer (to be exchanged in the subsequent telegram).

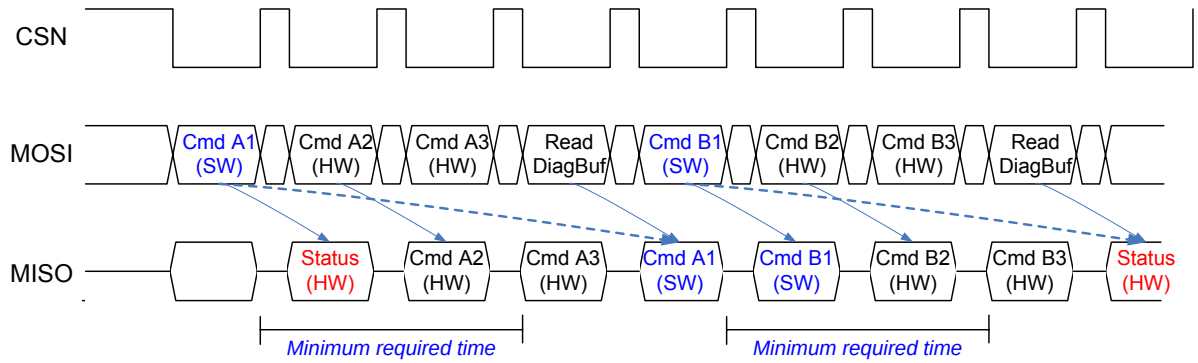
After a software command (here named CMD_A) has been sent by the host there are two possible cases:

1. The host waits for at least the maximum required time (see table) before sending another SPI command. In this case the reply telegram will contain the answer to the previous software command.
2. The host sends a hardware command without waiting for the maximum required time. In this case the reply telegram can contain one of the following answers:
    a) The answer to the previous software command, if already available.
    b) The STATUS telegram (0x02), if the software answer is not yet prepared. In this case the host can get the answer to the software command later, after the maximum required time, by sending the ReadDiagBuf command (the answer to the software command will then be available in the telegram exchanged after this ReadDiagBuf command)

Note: is not allowed to send another software command before the maximum required time from previous software command is elapsed.



Time diagram example for case 1



Time diagram for case 2 (example of both possible situations)

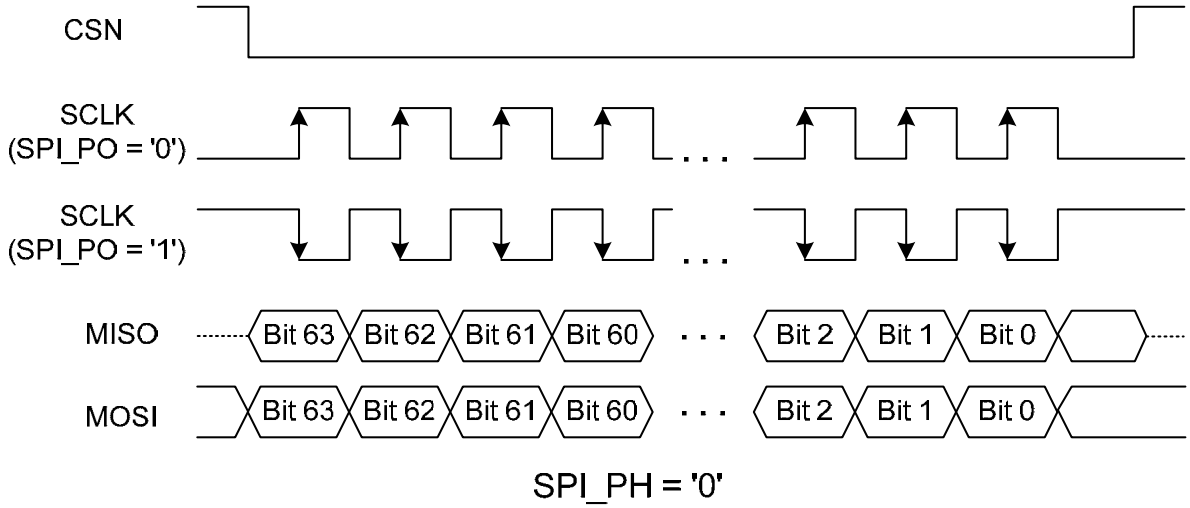
6.8. CRC

The correct CRC value has to be provided by the host in the Tinfo field in order to have the ASIC accept and process the command telegram. Any error in the CRC value makes the ASIC reject the incoming telegram and reply with the extended status telegram. The algorithm that has to be used to compute the CRC value is showed by means of a real programming language (ANSI standard C). It can be used as is in an appropriate programming context. The source code simply contains a vector – the lookup table – as well as a function taking a 7 bytes array input and returning the CRC value of the input array.

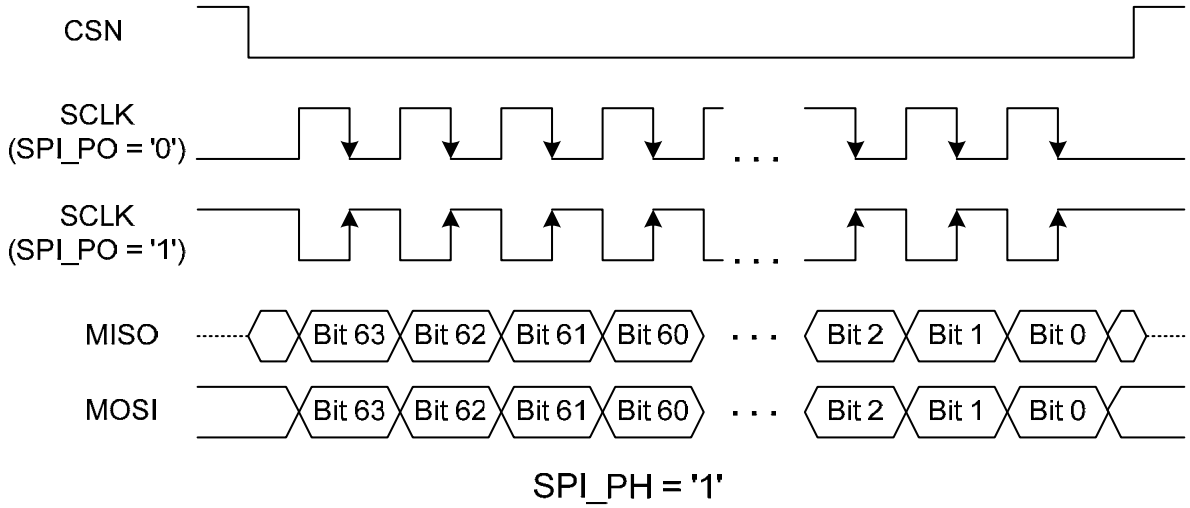
```
/*****************************************************************
Begin of CRC Lookup Table
*****************************************************************/

unsigned char crctable [256] = {

        0x00, 0x1D, 0x3A, 0x27, 0x74, 0x69, 0x4E, 0x53,
        0xE8, 0xF5, 0xD2, 0xCF, 0x9C, 0x81, 0xA6, 0xBB,
        0xCD, 0xD0, 0xF7, 0xEA, 0xB9, 0xA4, 0x83, 0x9E,
        0x25, 0x38, 0x1F, 0x02, 0x51, 0x4C, 0x6B, 0x76,
        0x87, 0x9A, 0xBD, 0xA0, 0xF3, 0xEE, 0xC9, 0xD4,
        0x6F, 0x72, 0x55, 0x48, 0x1B, 0x06, 0x21, 0x3C,
        0x4A, 0x57, 0x70, 0x6D, 0x3E, 0x23, 0x04, 0x19,
        0xA2, 0xBF, 0x98, 0x85, 0xD6, 0xCB, 0xEC, 0xF1,
        0x13, 0x0E, 0x29, 0x34, 0x67, 0x7A, 0x5D, 0x40,
        0xFB, 0xE6, 0xC1, 0xDC, 0x8F, 0x92, 0xB5, 0xA8,
        0xDE, 0xC3, 0xE4, 0xF9, 0xAA, 0xB7, 0x90, 0x8D,
        0x36, 0x2B, 0x0C, 0x11, 0x42, 0x5F, 0x78, 0x65,
        0x94, 0x89, 0xAE, 0xB3, 0xE0, 0xFD, 0xDA, 0xC7,
        0x7C, 0x61, 0x46, 0x5B, 0x08, 0x15, 0x32, 0x2F,
        0x59, 0x44, 0x63, 0x7E, 0x2D, 0x30, 0x17, 0x0A,
        0xB1, 0xAC, 0x8B, 0x96, 0xC5, 0xD8, 0xFF, 0xE2,
        0x26, 0x3B, 0x1C, 0x01, 0x52, 0x4F, 0x68, 0x75,
        0xCE, 0xD3, 0xF4, 0xE9, 0xBA, 0xA7, 0x80, 0x9D,
        0xEB, 0xF6, 0xD1, 0xCC, 0x9F, 0x82, 0xA5, 0xB8,
        0x03, 0x1E, 0x39, 0x24, 0x77, 0x6A, 0x4D, 0x50,
        0xA1, 0xBC, 0x9B, 0x86, 0xD5, 0xC8, 0xEF, 0xF2,
        0x49, 0x54, 0x73, 0x6E, 0x3D, 0x20, 0x07, 0x1A,
        0x6C, 0x71, 0x56, 0x4B, 0x18, 0x05, 0x22, 0x3F,
        0x84, 0x99, 0xBE, 0xA3, 0xF0, 0xED, 0xCA, 0xD7,
        0x35, 0x28, 0x0F, 0x12, 0x41, 0x5C, 0x7B, 0x66,
        0xDD, 0xC0, 0xE7, 0xFA, 0xA9, 0xB4, 0x93, 0x8E,
        0xF8, 0xE5, 0xC2, 0xDF, 0x8C, 0x91, 0xB6, 0xAB,
        0x10, 0x0D, 0x2A, 0x37, 0x64, 0x79, 0x5E, 0x43,
        0xB2, 0xAF, 0x88, 0x95, 0xC6, 0xDB, 0xFC, 0xE1,
        0x5A, 0x47, 0x60, 0x7D, 0x2E, 0x33, 0x14, 0x09,
        0x7F, 0x62, 0x45, 0x58, 0x0B, 0x16, 0x31, 0x2C,
        0x97, 0x8A, 0xAD, 0xB0, 0xE3, 0xFE, 0xD9, 0xC4};

/*****************************************************************
End of CRC Lookup Table
*****************************************************************/

   //! \brief crc8_poly1D calculates crc8 checksum
   //! \param A 7 bytes long array whose CRC has to be computed. The 0 indexed byte is the
most significant byte
   //! \return an unsigned char that represents the CRC value
   //! \pre Actual parameter contains at least 7 elements
   //! \post

   //! This function generates the CRC checksum for the 7 input bytes using
   //! Polinomial \f$x^8+x^4+x^3+x^2+1\f$.*/
unsigned char crc8_poly1D (const unsigned char * p_data){

   unsigned char crc = 0xFF, i;

   for (i = 7; i > 0; --i){
         // Every byte is xored with table value 'addressed' on the basis of its own value
      crc = crctable [crc ^ p_data [i]];
   }

   return ( ~ crc );  // final NOT
}
```

6.9. SPI Phase and Polarity

The sd_rate_spi mode is programmable resulting in the following possible behaviors:



SPI_PH = '0'

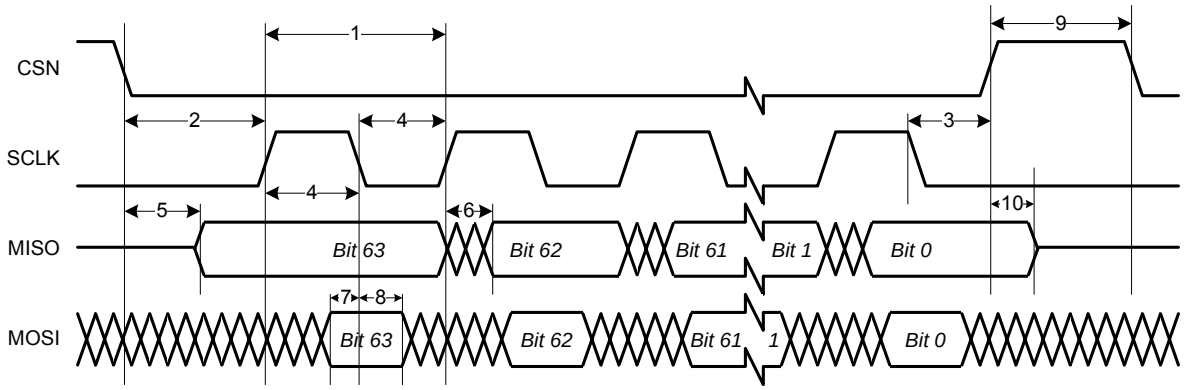


SPI_PH = '1'

The MOSI pin (SPI data input for sd705) is sampled in correspondence of the SCLK edge indicated with an arrow. The MISO pin (SPI data output for sd705) is updated at the opposite edge.

The default configuration for the SPI interface of SD705 is phase set to 1 and polarity to 0.

6.10. SPI Timing specification



N	PARAMETER	SYMBOL	MIN	MAX	UNIT	COMMENT
1	SCLK period	t_{SCLK_PER}	150		ns	
2	Enable lead time	t_{EN_LEAD}	280		ns	4 Tsys_clk
3	Enable lag time	t_{EN_LAG}	20		ns	Same as 8 (MOSI hold time)
4	SCLK low, high time	t_{SCLK_LOW}, t_{SCLK_HIGH}	75		ns	
5	MISO activation time	t_{MISO_ACT}	210	280	ns	3 - 4 Tsys_clk
6	SCLK to MISO time	t_{MISO_SU}		20	ns	
7	MOSI setup time	t_{MOSI_SU}		20	ns	
8	MOSI hold time	t_{MOSI_HOLD}		20	ns	
9	CSN high time	t_{CSN_HIGH}	210		ns	3 Tsys_clk
10	CS high to MISO HZ	t_{CSN_HZ}	0	20	ns	

Notes:

1. Some of the numerical values are dependent on the internal clock period Tsys_clk (assumed as 70 ns in this table)
2. Some values are still under characterization
3. MISO and MOSI data are asynchronously shifted
4. The figure refers to the case in which the SPI configuration is phase set to 1 and polarity set to 0.
5. Miso activation time is due to some actions performed in the sys_clk domain on the shift registers before switching to the asynchronous clocking using SCLK.
6. The minimum SCLK period can be calculated as follows:
   T_{HO} : Delay of the output pad of the Host module
   T_{HI} : Delay of the input pad of the Host module
   T_L: Delay of the interconnections
   T_{GO} : Delay of the output pad of the Gyro module
   T_{GI} : Delay of the input pad of the Gyro module
   T_{REG} : additional time for internal sampling operations

   $$T_{HO} + 2T_L + T_{GI} + T_{REG} + T_{GO} + T_{HI} < \tfrac{1}{2} T_{SCLK}$$

   A raw estimation could be:
   T_{HO}, T_{GO}: 1-3 ns
   T_{HI}, T_{GI}: 3-10 ns
   T_{REG} : 20 ns

   $$\text{Max} \sim= (90 \text{ ns} + 4T_L) < T_{SCLK}$$