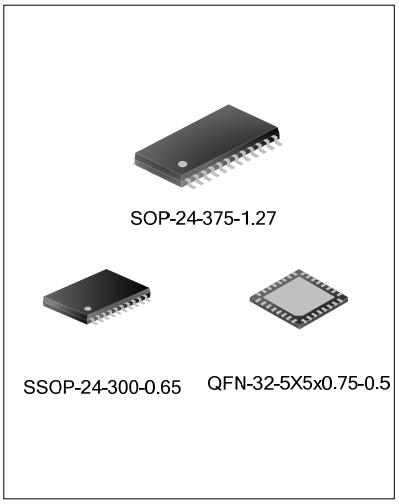
I²C-BUS CONTROLLED SINGLE AND MULTISTANDARD ALIGNMENT-FREE IF-PLL DEMODULATORS

DESCRIPTION

The SD9885 is an alignment-free multistandard (PAL and NTSC) vision and sound IF signal PLL demodulator for negative modulation only and FM processing.

The SD9886 is an alignment-free multistandard(PAL, SECAM and NTSC) vision and sound IF signal PLLdemodulator for positive and negative modulation,including sound AM and FM processing.



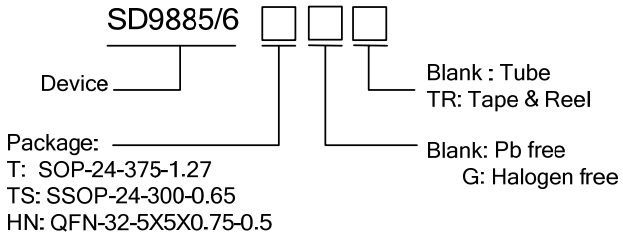
FEATURES

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier, AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I²C-bus
- Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75, and 58.75 MHz
- 4 MHz reference frequency input
- VIF Automatic Gain Control (AGC) detector for gain control
- External AGC setting via pin OP1
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter, AFC bits readable via I²C -bus
- TakeOver Point (TOP) adjustable via I²C -bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0, and 6.5 MHz, controlled by FM-PLL oscillator

APPLICATIONS

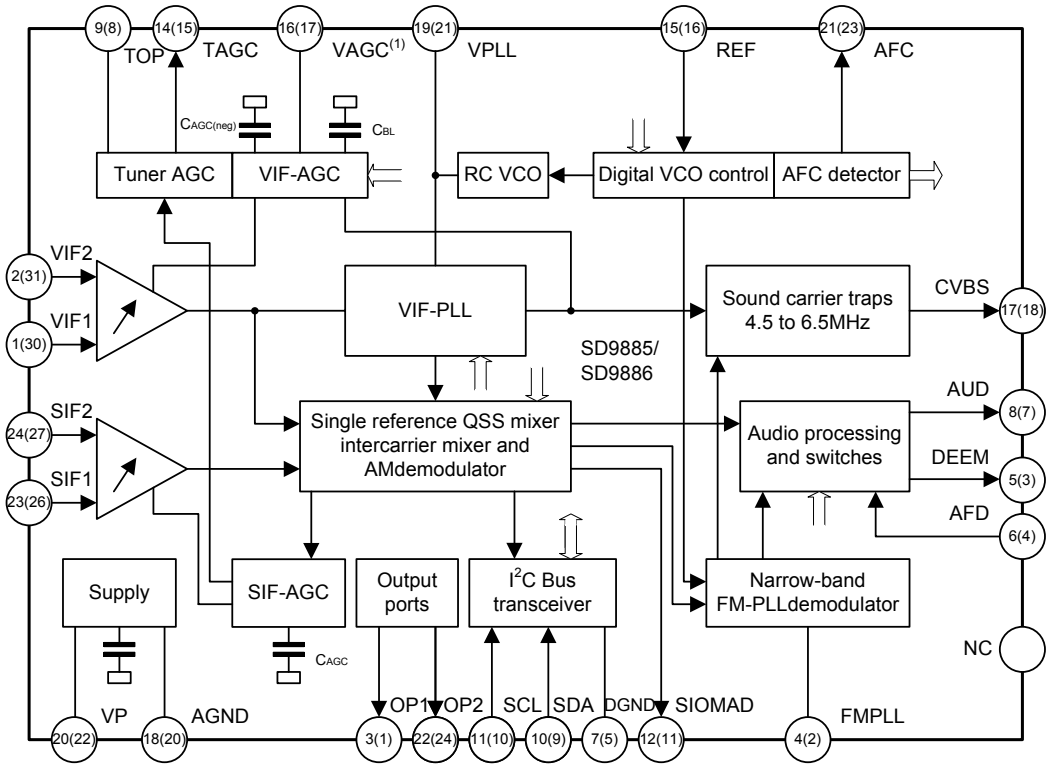
- TV, VTR, PC and STB applications.

ORDERING INFORMATION



Part No.	Package	Marking	Material	Package Type
SD9885T	SOP-24-375-1.27	SD9885T	Pb free	Tube
SD9885TTR	SOP-24-375-1.27	SD9885T	Pb free	Tape& Reel
SD9885TS	SSOP-24-300-0.65	SD9885TS	Pb free	Tube
SD9885TSTR	SSOP-24-300-0.65	SD9885TS	Pb free	Tape& Reel
SD9885HN	QFN-32-5*5*0.75-0.5	SD9885HN	Pb free	Tube
SD9885HNTR	QFN-32-5*5*0.75-0.5	SD9885HN	Pb free	Tape& Reel
SD9886T	SOP-24-375-1.27	SD9886T	Pb free	Tube
SD9886TTR	SOP-24-375-1.27	SD9886T	Pb free	Tape& Reel
SD9886TS	SSOP-24-300-0.65	SD9886TS	Pb free	Tube
SD9886TSTR	SSOP-24-300-0.65	SD9886TS	Pb free	Tape& Reel
SD9886HN	QFN-32-5*5*0.75-0.5	SD9886HN	Pb free	Tube
SD9886HNTR	QFN-32-5*5*0.75-0.5	SD9886HN	Pb free	Tape& Reel

BLOCK DIAGRAM



Pin numbers for SD9885HN and SD9886HNin parenthesis

ABSOLUTE MAXIMUM RATING In accordance with the Absolute Maximum Rating System (IEC 134).

Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Voltage	V_P		0	5.5	V
pins VIF1, VIF2, SIF1, SIF2, OP1, OP2, VP, and FMPLL	V_n		0	V_P	V
Pin TAGC			−	8.8	V
Maximum Short-Circuit Time	$t_{sc(max)}$	to ground or VCC	−	10	s
Storage Temperature	T_{stg}		−25	+150	°C
Ambient Temperature SD9885T (SOP24), SD9885TS (SSOP24), SD9886T (SOP24) and SD9886TS (SSOP24)	T_{amb}		−20	+70	°C
SD9885HN (QFN32) and SD9886HN (QFN32)			-20	+85	°C

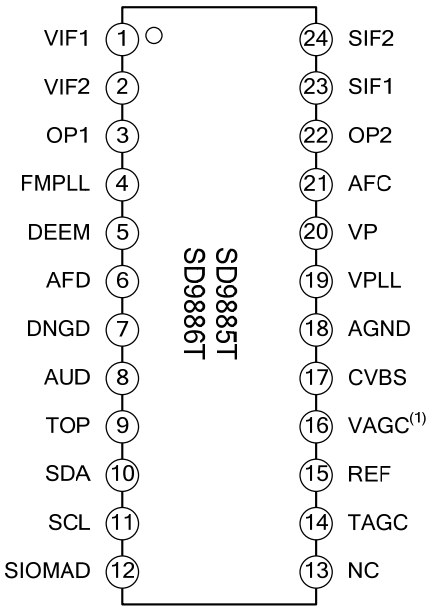
ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_P		4.5	5.0	5.5	V
Supply Current	I_P		52	63	70	mA
Video part						
VIF Input Voltage Sensitivity (RMS Value)	$V_{i(VIF)(rms)}$	−1 dB video at output;	−	60	100	μV
VIF Gain Control Range	$G_{VIF(cr)}$		60	66	−	dB
Vision Carrier Operating Frequencies	f_{VIF}		− − − − − −	33.4 33.9 38.0 38.9 45.75 58.75	− − − − − −	MHz MHz MHz MHz MHz MHz
VIF Frequency Window Of Digital Acquisition Help	Δf_{VIF}	Related to f_{VIF};	−	±2.3	−	MHz
Video Signal Output Voltage (Peak-To-Peak Value)	Vo(v)(p-p)	normal mode trap bypass mode	1.7 0.95	2.0 1.10	2.3 1.25	V
Differential Gain	Gdif	"CCIR 330" B/G standard L standard	 − −	− −	 5 7	 % %
Differential Phase	φdif	"CCIR 330"	−	2	4	deg
−1 dB Video Bandwidth	Bv(−1dB)	trap bypass mode; AC load; CL < 20 pF; RL >1kΩ	5	6	−	MHz
−3 dB Video Bandwidth Including Sound Carrier Trap	Bv(-3dB)(trap)	f_{trap} = 4.5 MHz f_{trap} = 5.5 MHz f_{trap} = 6.0 MHz f_{trap} = 6.5 MHz	3.95 4.90 5.40 5.50	4.05 5.00 5.50 5.95	− − − −	MHz MHz MHz MHz
Trap Attenuation At first Sound Carrier	αSC1	M/N standard B/G standard	30 30	36 36	− −	dB dB
Weighted Signal-To-Noise Ratio	S/NW	weighted in accordance with "CCIR 567"	56	59	−	dB
Power Supply Ripple Rejection At Pin CVBS	PSRRCVBS	f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation;	20	25	−	dB
AFC Control Steepness	AFCstps	definition: $\Delta IAFC/\Delta f_{VIF}$	0.85	1.05	1.25	μA/kHz

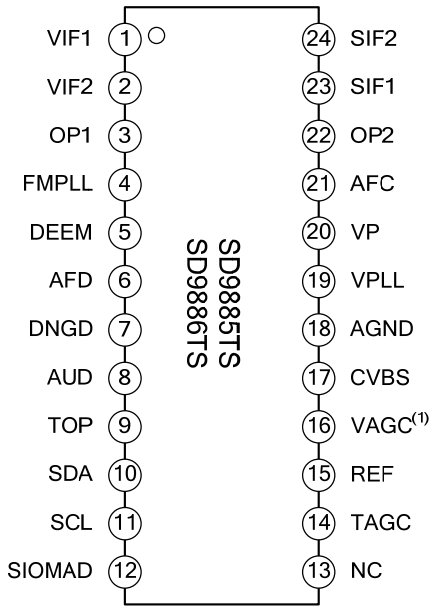
Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Audio part						
AF Output Voltage (RMS Value)	$V_{o(AF)(rms)}$	27 kHz FM deviation; 50 µs de-emphasis	430	540	650	mV
Total Harmonic Distortion Of Audio Signal	THD	FM: 27 kHz FM deviation; 50 µs de-emphasis AM: m = 54 %	– –	0.15 0.5	0.5 1	% %
-3dB AF Bandwidth	BAF(-3dB)	without de-emphasis; dependent on FM-PLL filter	80	100	–	KHz
Weighted Signal-To-Noise Ratio Of Audio Signal	S/NW(AF)	FM: 27 kHz FM deviation; 50 µs de-emphasis; vision carrier unmodulated AM: m = 54 %	52 45	56 50	– –	dB dB
AM Suppression Of FM Demodulator	$\alpha_{AM(sup)}$	50 µs de-emphasis; AM: f = 1 kHz and m = 54 %; referenced to 27 kHz FM deviation	40	46	–	dB
Power Supply Ripple Rejection On Pin AUD	PSRRAUD	f_{ripple} = 70 Hz; for AM for FM	 20 14	 26 20	 – –	 dB dB
IF Intercarrier Output Level (RMS Value)	$V_{o(intc)(rms)}$	QSS mode; SC1; SC2 off	90	140	180	mV
		L standard; without modulation	90	140	180	mV
		intercarrier mode; PC/SC1 = 20 dB; SC2 off;		75		mV
Reference Frequency						
Reference Signal Frequency	f_{ref}		–	4	–	MHz
Reference Signal Voltage (RMS Value)	$V_{ref(rms)}$	operation as input terminal	90[(1)]	–	400	mV

(1) The minimum reference signal voltage is 90mV, higher than TDA9885/6 by 10mV.

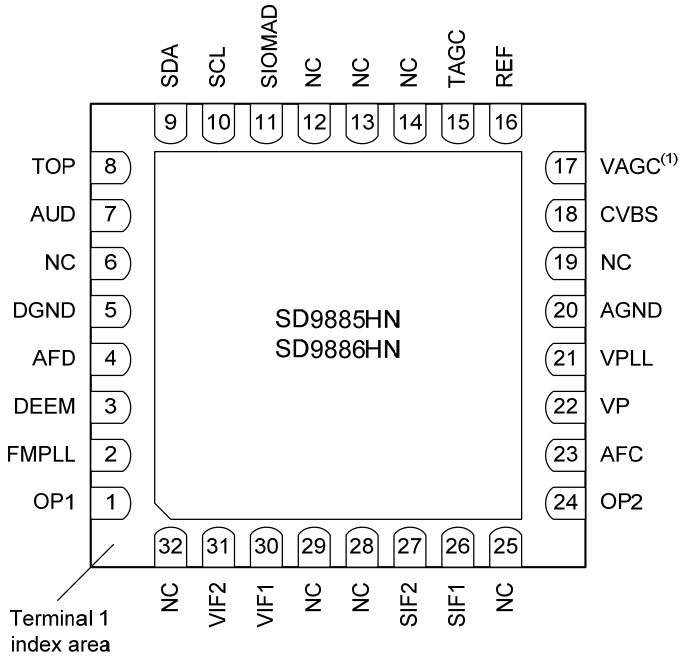
PIN CONFIGURATION



(1) not connected for SD9885T



(1) not connected for SD9885TS



Bottom view

(1) not connected for SD9885HN

PIN DESCRIPTION

Pin No.				Pin Name	I/O	Pin Descriptions
SD9885T SD9885TS	SD9886T SD9886TS	SD9885HN	SD9886HN			
1	1	30	30	VIF1	I	VIF differential input 1
2	2	31	31	VIF2	I	VIF differential input 2
-	-	32	32	NC	--	not connected
3	3	1	1	OP1	I	output port 1; open-collector
4	4	2	2	FMPLL	O	FM-PLL for loop filter
5	5	3	3	DEEM	I	de-emphasis output for capacitor
6	6	4	4	AFD	I	AF decoupling input for capacitor
7	7	5	5	DGND	G	digital ground
-	-	6	6	NC	--	not connected
8	8	7	7	AUD	O	audio output
9	9	8	8	TOP	I	tuner AGC TakeOver Point (TOP) for resistor adjustment
10	10	9	9	SDA	I/O	I^2C-bus data input and output
11	11	10	10	SCL	I	I^2C-bus clock input
12	12	11	11	SIOMAD	O	sound intercarrier output and MAD select with resistor
-	-	12	12	NC	--	not connected
13	13	13	13	NC	--	not connected
-	-	14	14	NC	--	not connected
14	14	16	15	TAGC	O	tuner AGC output
15	15	16	16	REF	I	4 MHz crystal or reference signal input
-	16	-	17	VAGC	O	VIF-AGC for capacitor
16	-	17	-	NC	--	not connected
17	17	18	18	CVBS	O	composite video output
-	-	19	19	NC	--	not connected
18	18	20	20	AGND	G	analog ground
19	19	21	21	VPLL	O	VIF-PLL for loop filter
20	20	22	22	VP	P	supply voltage
21	21	23	23	AFC	O	AFC output
22	22	24	24	OP2	O	output port 2;
-	-	25	25	NC	--	not connected
23	23	26	26	SIF1	I	SIF differential input 1 and MAD select with resistor
24	24	27	27	SIF2	I	SIF differential input 2 and MAD select with resistor
-	-	28	28	NC	--	not connected
-	-	29	29	NC	--	not connected

FUNCTION DESCRIPTION

1. Video demodulation

Before the video demodulator, An VIF amplifier with AGC amplifies the VIF signal; The true synchronous video demodulator is realized by a linear multiplier which is designed for low distortion and wide bandwidth. The vision IF input signal is multiplied with the 'in phase' component of the VCO output. The demodulator output signal is fed via an integrated low-pass filter (fg = 12 MHz) for suppression of the carrier harmonics to the video amplifier.

After demodulator, video signal is fed into a sound trap filter. The accurate frequency position for the different standards is set by the sound carrier reference signal through an internal PLL. The differential trap output signal is converted and amplified by the following postamplifier. The video output level at pin CVBS is 2 V (p-p). In the bypass mode the output signal of the preamplifier is fed directly through the postamplifier to pin CVBS. The output video level is 1.1 V (p-p) for using an external sound trap with 10 % overall loss. Noise clipping is provided in both cases.

2. Sound demodulation

After a three-stages AC-coupled SIF amplifier, Amplitude Modulated signal is fed both to a two-stage limiting amplifier that removes the AM and to a linear multiplier. The result of the multiplication of the SIF signal with the limiter output signal is AM demodulation. The demodulator output signal is fed via a low-pass filter that attenuates the carrier harmonics.

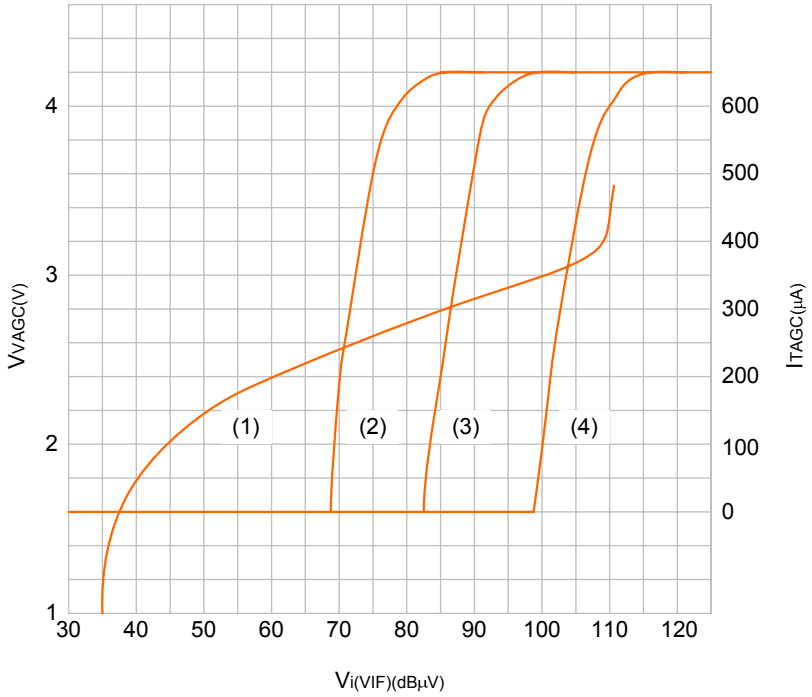
Generated by a single reference QSS mixer, the 2nd FM sound intercarrier signal is fed to an AC-coupled gain controlled amplifier. The gain controlled output signal is fed to the phase detector of the narrow-band FM-PLL to generates AF signal which is fed via a buffer to the audio amplifier.

The audio amplifier with internal feedback is designed for high gain and high common-mode rejection. The low-level AF signal output from the FM-PLL demodulator is amplified and buffered in a low-ohmic audio output stage. An external decoupling capacitor CDAF removes the DC voltage from the audio amplifier input.

Switching to the mute state is controlled automatically.

3. Tuner AGC and VIF-AGC

This block adapts the voltages, generated at the VIF-AGC and SIF-AGC detectors, to the internal signal processing at the VIF and SIF amplifiers and performs the tuner AGC control current generation. The onset of the tuner AGC control current generation can be set either via the I^2C-bus (see Table 13) or optionally by a potentiometer at pin TOP (in case that the I^2C -bus information cannot be stored, related to the device). The presence of a potentiometer is automatically detected and the I^2C -bus setting is disabled.

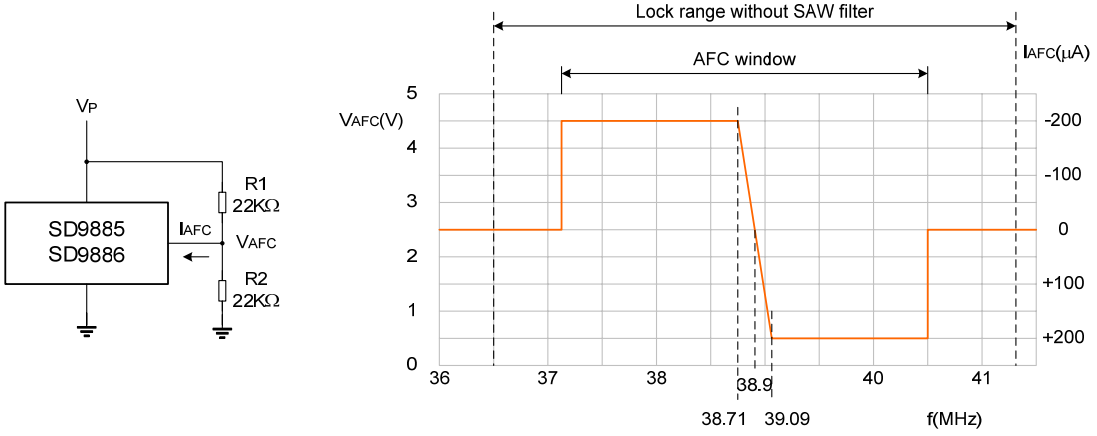


(1) V_{VAGC} is VIF-AGC voltage and can only be measured at pin OP2 controlled by the I^2C-bus .
(2) I_{TAGC} is tuner current in TV mode with R_{TOP}=22KΩ or setting via I^2C-bus at -15dB.
(3) I_{TAGC} is tuner current in TV mode with R_{TOP}=10KΩ or setting via I^2C-bus at 0dB.
(4) I_{TAGC} is tuner current in TV mode with R_{TOP}=0KΩ or setting via I^2C-bus at +15dB.

Typical VIF and tuner AGC characteristic.

4. AFC and digital acquisition help

Each relaxation oscillator of the VIF-PLL and FM-PLL demodulator has a wide frequency range. To prevent false locking of the PLLs and with respect to the catching range, the digital acquisition help provides an individual control, until the frequency of the VCO is within the preselected standard dependent lock-in window of the PLL. The in-window and out-window control at the FM-PLL is additionally used to mute the audio stage (if auto mute is selected via the I^2C-bus).



Typical analog AFC characteristic.

5. I²C-bus transceiver and module address

The device can be controlled via the 2-wire I^2C-bus by a microcontroller. To avoid conflicts in a real application with other devices providing similar or complementing functions, there are four possible slave addresses available. These Module Addresses (MADs) can be selected by connecting resistors on pin SIOMAD and/or pins SIF1 and SIF2 (Pin SIOMAD relates with bit A0 and pins SIF1 and SIF2 relate with bit A3). The slave addresses of this device are given in Table 1.

Table 1 Slave address detection

SLAVE ADDRESS	SELECTABLE ADDRESS BIT		RESISTOR ON PIN	
	A3	A0	SIF1 AND SIF2	SIOMAD
MAD1	0	1	no	no
MAD2	0	0	no	yes
MAD3	1	1	yes	no
MAD4	1	0	yes	yes

I²C BUS CONTROL

1. Read register

1) SLAVE ADDRESS

The first module address MAD1 is the standard address (see Table 1). **Table 2** Slave addresses.

Table 2 Slave addresses

SLAVE ADDRESS		BIT						
NAME	VALUE (HEX)	A6	A5	A4	A3	A2	A1	A0
MAD1	43	1	0	0	0	0	1	1
MAD2	42	1	0	0	0	0	1	0
MAD3	4B	1	0	0	1	0	1	1
MAD4	4A	1	0	0	1	0	1	0

2) DATA BYTE

Table 3 Data read register (status register)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
AFCWIN	VIFLEV	CARRDET	AFC4	AFC3	AFC2	AFC1	PONR

Table 4 Description of status register bits

BIT	VALUE	DESCRIPTION
AFCWIN	1 0	**AFC window** VCO in ±1.6 MHz AFC window; VCO out of ±1.6 MHz AFC window
VIFLEV	1 0	**VIF input level** high level; VIF input voltage ≥200 μV (typically) low level
CARRDET	1 0	**FM carrier detection** Detection no detection
AFC[4:1]		**Automatic frequency control** see Table 5
PONR	1 0	**Power-on reset** after Power-on reset or after supply breakdown after a successful reading of the status register

Table 5 Automatic frequency control bits.

BIT				fVIF
AFC4	AFC3	AFC2	AFC1	
0	1	1	1	≤ (f0 − 187.5 kHz)
0	1	1	0	f0 − 162.5 kHz
0	1	0	1	f0 − 137.5 kHz
0	1	0	0	f0 − 112.5 kHz
0	0	1	1	f0 − 87.5 kHz
0	0	1	0	f0 − 62.5 kHz
0	0	0	1	f0 − 37.5 kHz
0	0	0	0	f0 − 12.5 kHz
1	1	1	1	f0 + 12.5 kHz
1	1	1	0	f0 + 37.5 kHz
1	1	0	1	f0 + 62.5 kHz
1	1	0	0	f0 + 87.5 kHz
1	0	1	1	f0 + 112.5 kHz
1	0	1	0	f0 + 137.5 kHz
1	0	0	1	f0 + 162.5 kHz
1	0	0	0	≥ (f0 + 187.5 kHz)

2. Write register

1) SUBADDRESS

If more than one data byte is transmitted, then auto-increment is performed: starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 6.

Table 6 Definition of the subaddress (second byte after slave address).

REGISTER	MSB							LSB
	A7(2)	A6(3)	A5(3)	A4(3)	A3(3)	A2(3)	A1	A0
SAD for switching mode	0	X	X	X	X	X	0	0
SAD for adjust mode	0	X	X	X	X	X	0	1
SAD for data mode	0	X	X	X	X	X	1	0

2) DATA BYTE FOR SWITCHING MODE

Table 7 Bit description of SAD register for switching mode (SAD = 00)

BIT	VALUE	DESCRIPTION
B7		**Output port 2 for SAW switching or monitoring**
	1	high-impedance, disabled or HIGH
	0	low-impedance, active or LOW
B6		**Output port 1 for SAW switching or external input**
	1	high-impedance, disabled or HIGH
	0	low-impedance, active or LOW
B5		**Forced audio mute**
	1	on
	0	off
B4 and B3		**TV standard modulation**
	00	positive AM TV; note 1
	01	not used
	10	negative FM TV
	11	not used
B2		**Carrier mode**
	1	QSS mode
	0	intercarrier mode
B1		**Auto mute of FM AF output**
	1	active
	0	inactive
B0		**Video mode (sound trap)**
	1	sound trap bypass
	0	sound trap active

Note : 1. For positive AM TV choose 6.5 MHz for the second SIF.

3) DATA BYTE FOR ADJUST MODE

Table 8 Bit description of SAD register for adjust mode (SAD = 01)

BIT	VALUE	DESCRIPTION
C7	1 0	**Audio gain** −6dB 0 dB
C6	1 0	**De-emphasis time constant** 50 μs 75 μs
C5	1 0	**De-emphasis** on off
C4 to C0		**Tuner takeover point adjustment** see Table 9

Table 9 Tuner takeover point adjustment bits

BIT					TOP ADJUSTMENT (dB)
C4	C3	C2	C1	C0	
1	1	1	1	1	+15
1	1	1	1	0	+14
1	1	1	0	1	+13
1	1	1	0	0	+12
1	1	0	1	1	+11
1	1	0	1	0	+10
1	1	0	0	1	+9
1	1	0	0	0	+8
1	0	1	1	1	+7
1	0	1	1	0	+6
1	0	1	0	1	+5
1	0	1	0	0	+4
1	0	0	1	1	+3
1	0	0	1	0	+2
1	0	0	0	1	+1
1	0	0	0	0	0(1)
0	1	1	1	1	−1
0	1	1	1	0	−2
0	1	1	0	1	−3
0	1	1	0	0	−4
0	1	0	1	1	−5
0	1	0	1	0	−6

BIT					TOP ADJUSTMENT (dB)
C4	C3	C2	C1	C0	
0	1	0	0	1	−7
0	1	0	0	0	−8
0	0	1	1	1	−9
0	0	1	1	0	−10
0	0	1	0	1	−11
0	0	1	0	0	−12
0	0	0	1	1	−13
0	0	0	1	0	−14
0	0	0	0	1	−15
0	0	0	0	0	−16

Note: 0 dB is equal to 17 mV (RMS).

4) DATA BYTE FOR DATA MODE

Table 10 Bit description of SAD register for data mode (SAD = 10)

BIT	VALUE	DESCRIPTION
E7		**VIF-AGC and port features** dependent on bit E5; see Table 11
E6	1 0	**L standard PLL gating** gating in case of 36 % positive modulation gating in case of 0 % positive modulation
E5		**VIF, SIF and tuner minimum gain** dependent on bit E7; see Table 11
E4 to E2		**Vision intermediate frequency selection** see Table 12
E1 and E0	00 01 10 11	**Sound intercarrier frequency selection (sound 2nd IF)** f_{FM} = 4.5 MHz f_{FM} = 5.5 MHz f_{FM} = 6.0 MHz f_{FM} = 6.5 MHz; note 1

Note: For positive modulation choose 6.5 MHz

Table 11 Options in extended TV mode; bit B3 = 0 of SAD 00 register

FUNCTION	BIT E7 = 0		BIT E7 = 1	
	BIT E5 = 0	BIT E5 = 1	BIT E5 = 0	BIT E5 = 1
Pin OP1	port function	port function	port function	VIF-AGC external input(1)
Pin OP2	port function	port function	VIF-AGC output(1)	port function
Gain	normal gain	minimum gain	normal gain	external gain

Note:

1. The corresponding port function has to be disabled (set to ‘high-impedance’); see Table 7.

Table 12 TV standard selection for VIF

VIDEO IF SELECT BITS			f_{VIF} (MHz)
E4	E3	E2	
0	0	0	58.75(1)
0	0	1	45.75(1)
0	1	0	38.9
0	1	1	38.0
1	0	0	33.9
1	0	1	33.4
1	1	0	not applicable
1	1	1	not applicable

Note :

1. Pin SIOMAD can be used for the selection of the different NTSC standards without I^2C-bus. With a resistor on pin SIOMAD, f_{VIF} = 58.75 MHz; without a resistor on pin SIOMAD, f_{VIF} = 45.75 MHz (NTSC-M).

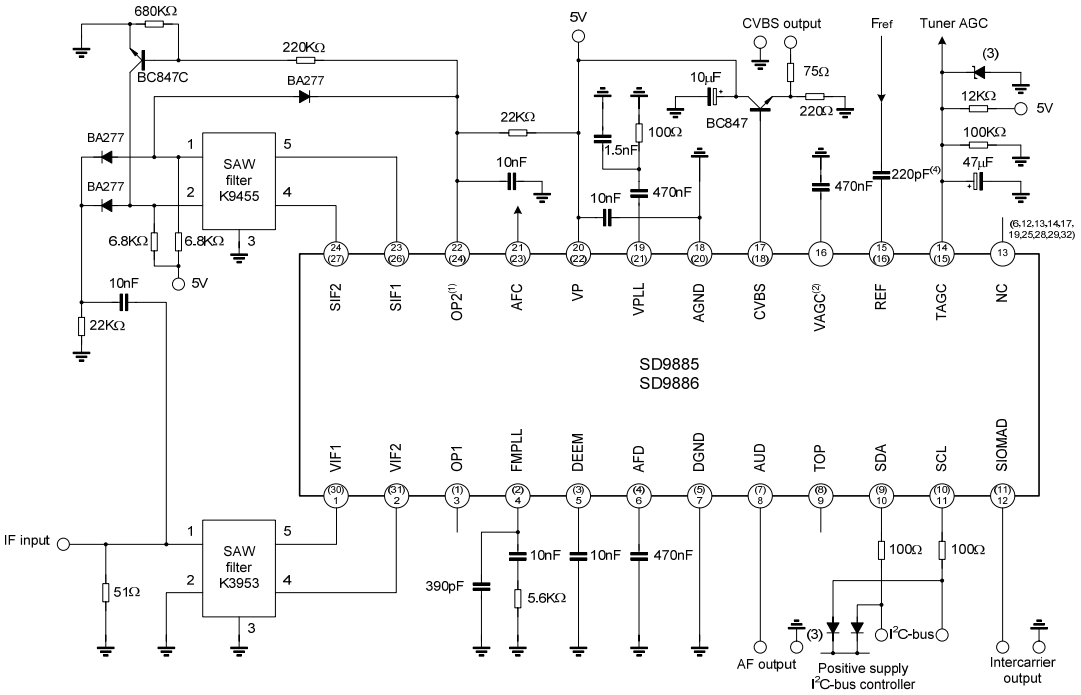
Table 13 Data setting after power-on reset (default setting with a resistor on pin SIOMAD)

REGISTER	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Switching mode	1	1	0	1	0	1	1	0
Adjust mode	0	0	1	1	0	0	0	0
Data mode	0	0	0	0	0	0	0	0

Table 14 Data setting after power-on reset (default setting without a resistor on pin SIOMAD)

REGISTER	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Switching mode	1	1	0	1	0	1	1	0
Adjust mode	0	0	1	1	0	0	0	0
Data mode	0	0	0	0	0	1	0	0

TYPICAL APPLICATION CIRCUIT

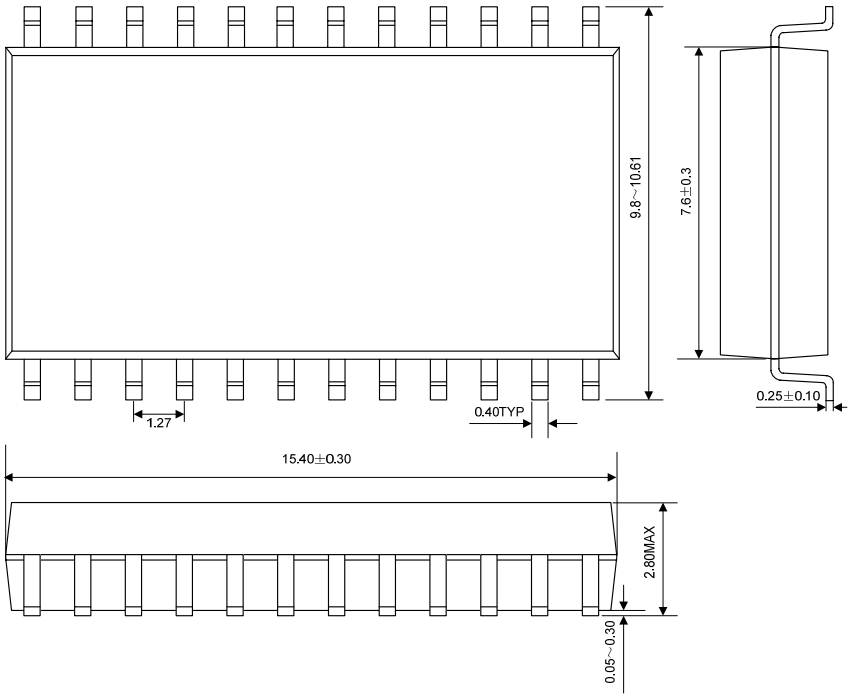


Pin numbers for SD9885HN and SD9886HN in parenthesis.
(1) If pin OP2 outputs VIF-AGC voltage, then pin OP1 can be used for SAW switching.
(2) Not connected for SD9885.
(3) Optional measures to improve ESD performance within a TV-set application.
(4) In order to ensure the performance, there is a little difference between the peripheral components of SD9885/6 and those of TDA9885/6.

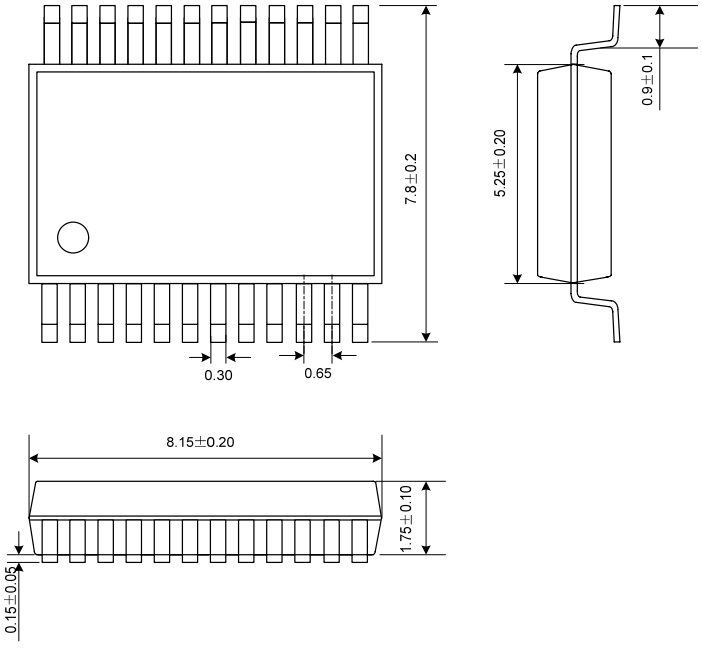
Components	TDA9885,6	SD9885,6
C1	220nF	470nF
R1	150~330Ω	100Ω
C2	>100pF	>200pF

PACKAGE OUTLINE

SOP-24-375-1.27 UNIT: mm

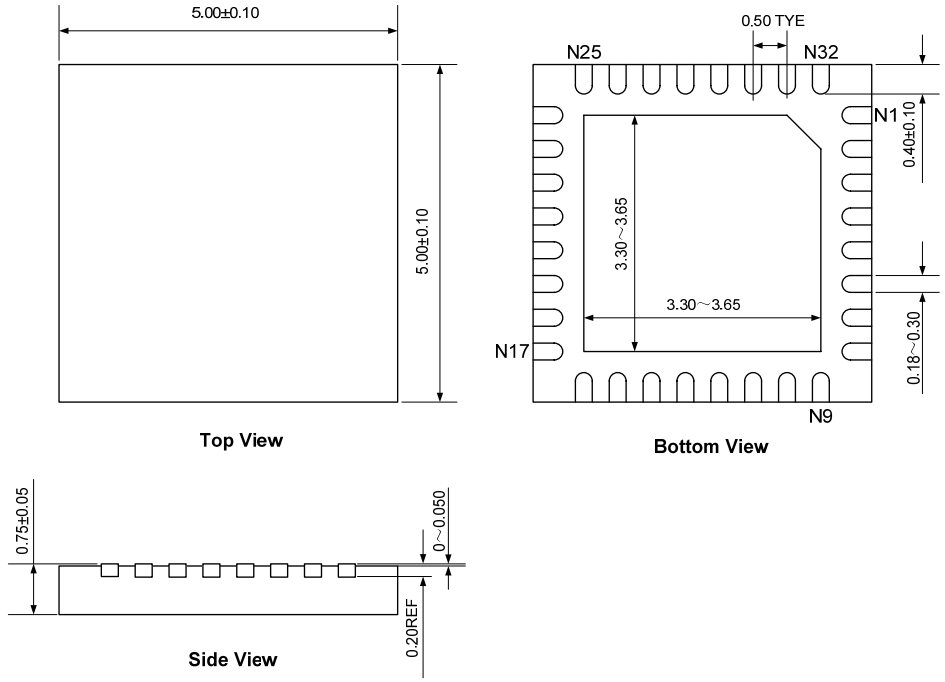


SSOP-24-300-0.65 UNIT: mm



PACKAGE OUTLINE

QFN-32-5×5×0.75-0.5 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

Disclaimer:

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice!
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!