Microprocessor-Compatible 10-Bit A/D Converters with 8-Channel Multiplexer

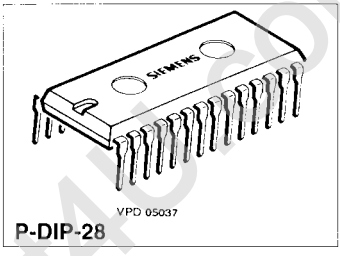
SDA 0810
SDA 1810

Preliminary Data

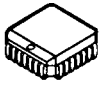
ACMOS IC

Features

- Advanced **CMOS** (ACMOS) technology
- 10-bit resolution
- Total unadjusted error ± 1/2 LSB
- No missing codes
- Fast conversion time (15 µs)
- SDA 1810 D with 66-kHz sampling frequency
- Single 5 V DC supply voltage
- 8-channel multiplexer with latched control logic
- Easy interfacing to all microprocessors, or stand-alone operation
- No offset or gain adjustments required
- Latched tristate outputs
- TTL-compatible output voltages
- Low power consumption (15 mW)



P-DIP-28



P-LCC-28-2

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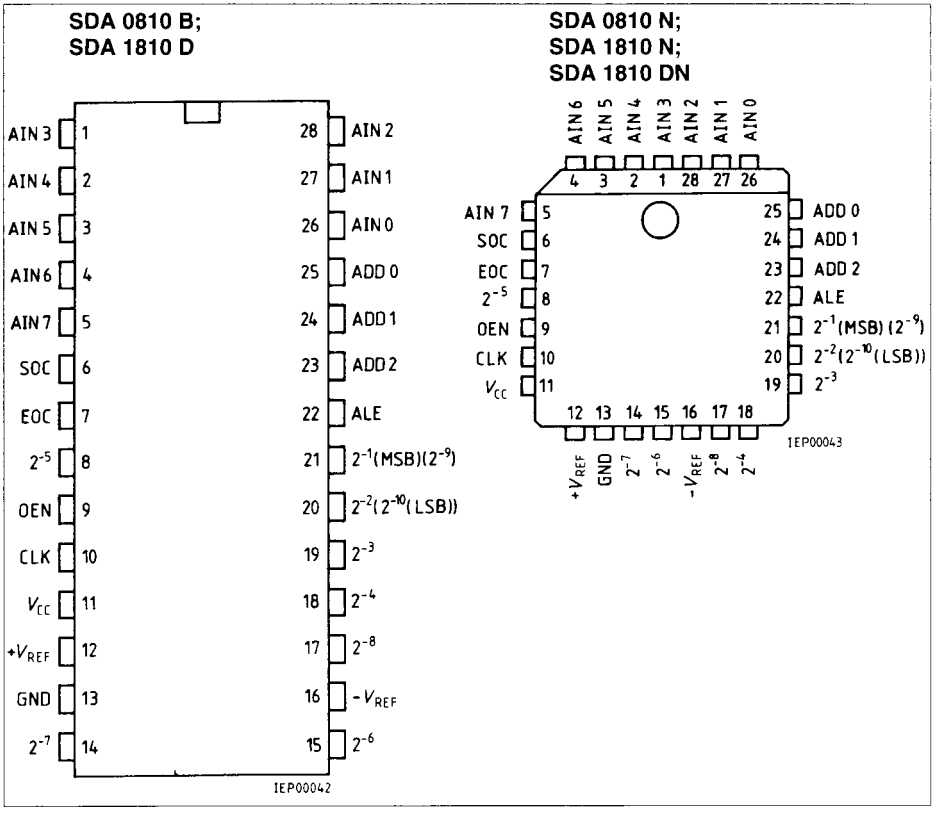
	Type	Ordering Code	Package
S	SDA 0810 B	Q67100-A8144	P-DIP-28
	SDA 0810 N	Q67100-A8207	P-LCC-28-2 (SMD)
	SDA 1810 D	Q67100-H8730	P-DIP-28
	SDA 1810 N	Q67100-A8230	P-LCC-28-2 (SMD)
	SDA 1810 DN	Q67100-H8735	P-LCC-28-2 (SMD)

SDA 0810 and SDA 1810 are monolithic 10-bit CMOS A/D converters with an 8-channel analog multiplexer and a single 5 V DC supply. They contain a microprocessor-compatible control logic and an 8-bit data bus and are pin-compatible with the industrial standard ADC 0808 and 0809. The 10-bit data stream is supplied in a 2-byte format for interfacing with 8-bit microprocessors. While the SDA 0810 can be operated at a clock frequency of 1 MHz, the SDA 1810 operates at a clock frequency of 2 MHz. SDA 1810 D offers enhanced dynamic performance for analog input frequencies up to 33 kHz.

The converters use the method of successive approximation by means of a capacitor network. The converters feature a temperature-stabilized comparator, an 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The converters need no external offset or gain adjustment. Easy interfacing to microprocessors is provided by 3-bit address latches, output latches and an 8-bit tristate data bus.

The temperature range of the SDA 0810 N and SDA 1810 N/D is – 40 °C to 85 °C, and that of the SDA 0810 B – 40 °C to 125 °C.



Pin Configurations
(top view)

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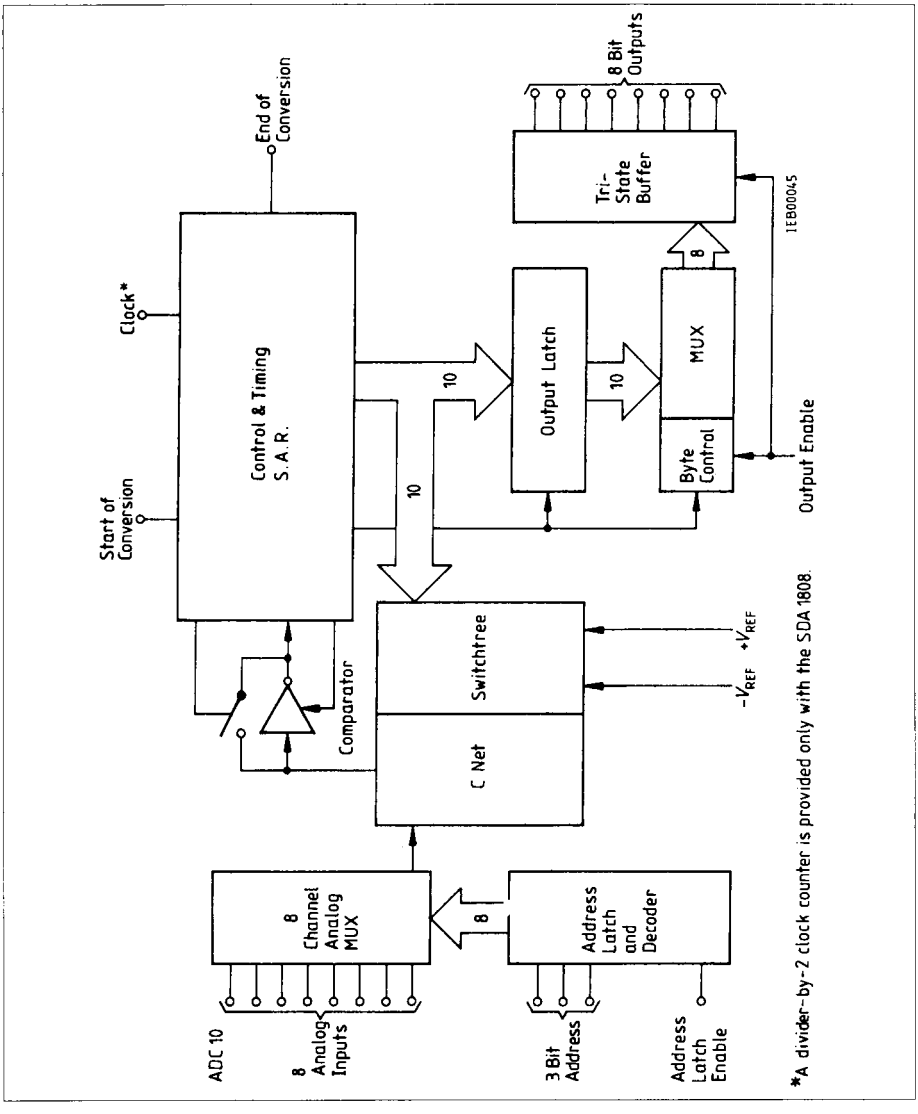
Pin Definitions and Functions

Pin	Symbol	Function
1 to 5	AIN 3 to AIN 7	Analog inputs
6 7	SOC EOC	Start of conversion End of conversion
8	2^{-5}	Digital output signal
9	OEN	Output enable signal
10	CLK	External clock input
11	V_{CC}	Positive supply voltage
12	$+ V_{REF}$	Positive reference voltage
13	GND	Ground
14 to 15	2^{-7}, 2^{-6}	Digital output signals
16	$- V_{REF}$	Negative reference voltage
17 to 21	2^{-8} to 2^{-1}	Digital output signals
22	ALE	Address latch enable
23 to 25 26 to 28	ADD 2 to ADD 0 AIN 0 to AIN 2	Address inputs Analog inputs



Block Diagram

Functional Description

Converter

The converter consists of three major parts: a capacitor network (approx. 50 pF) as a sample and hold circuit, a successive-approximation register and a comparator.

The A/D converter's successive-approximation register (SAR) is reset with the positive edge of the start of conversion (SOC) pulse. The conversion starts with the next rising edge of the external clock signal after the falling edge of the SOC pulse. A conversion in process will be interrupted by an SOC pulse.

Following the rising edge of the SOC pulse, the EOC output passes to the low level. It is set to logic one with the first rising edge of the external clock after the internal latch pulse.

The comparator is a differential comparator which is automatically set to zero; it has a high supply rejection factor.

A/D Converter Timing

The values stated apply to the SDA 0810, those in parentheses to the SDA 1810.

After a conversion has been started, the analog voltage at the selected input channel is sampled for 4 (8) external clock cycles which will then be kept at the sampled level for the remaining conversion time. The external analog source must be capable of supplying the current that is necessary to charge the sample and hold capacitance of approx. 50 pF within those 4 (8) clock cycles.

Conversion of the sampled analog voltage takes place between the 5th and 15th (10th and 30th) clock cycle after sampling has been completed. In the 15th (30th) clock cycle the result of the conversion is written into the output data latch. The EOC signal is set during the rising edge of the 16th (32nd) clock cycle.

Multiplexer

The converter provides eight multiplexed analog input channels. The input channels are selected by programming three address lines (AD2, AD1, AD0).

Table 1 shows the input states for the address lines that select a channel. The address is latched on the rising slope of the ALE signal.

Table 1

Address Lines			Selected Analog Channel
AD2	AD1	AD0	AIN
L	L	L	AIN 0
L	L	H	AIN 1
L	H	L	AIN 2
L	H	H	AIN 3
H	L	L	AIN 4
H	L	H	AIN 5
H	H	L	AIN 6
H	H	H	AIN 7

Reading the Conversion Results

The data is read as two 8-bit bytes. The digital outputs of the converters are positive true. Data is presented left-justified and high byte first. The first OEN high after completion of a conversion enables high byte (2^{-1} to 2^{-8}) to the output buffers, the second OEN pulse enables the low byte (2^{-9} to 2^{-10}), the unused bits of this byte are grounded. The byte control logic determines which byte is to be read. With each reading operation a flipflop is toggled so that in successive reading operations the bytes are output alternately. This flipflop is always reset to the high byte at the end of a conversion.

Data Bit Location

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
High byte	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
Low byte	2^{-9}	2^{-10}	0	0	0	0	0	0

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage [1]	V_{CC}		6.5	V
Input voltage range, any input	V_I	− 0.3	V_{CC} + 0.3	V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	− 65	125	°C
Thermal resistance system ambient				
P-DIP-28	$R_{th\,SA}$		50	K/W
P-LCC-28-2	$R_{th\,SA}$		70	K/W

Operating Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{CC}	4.5	5	6	V
Positive reference voltage [2]	$+ V_{REF}$		V_{CC}	V_{CC} +0.1	V
Negative reference voltage	$- V_{REF}$	− 0.1	0		V
Differential reference voltage [10]	$V_{REF} = + V_{REF} - (- V_{REF})$		5		V
Analog input range	V_{AIN}	V_{REF}		$+ V_{REF}$	V
Slew rate [11] (f_{CLK} = 1 MHz/2 MHz) SDA 0810 B/N; SDA 1810 N	SR			78	mV/µs
Start pulse duration	$t_{W\,(S)}$	200			ns
Address load control pulse width	$t_{W\,(ALE)}$	200			ns
Address setup time	t_{Setup}	50			ns
Address hold time	t_{Hold}	50			ns
Clock frequency SDA 0810	f_{CLK}	50	640	1000	kHz
SDA 1810	f_{CLK}	100	1280	2000	kHz
Ambient temperature					
SDA 0810 N; SDA 1810 N/D	T_A	− 40		85	°C
SDA 0810 B	T_A	− 40		125	°C

For notes refer to 3 pages hereafter.

Characteristics in the Operating Temperature Range
V_{CC} = 4.75 to 5.25 V, unless otherwise specified

Total Component

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High-level input voltage, control inputs	V_{IH}	V_{CC} – 1.5			V	V_{CC} = 5 V
Low-level input voltage, control inputs	V_{IL}			1.5	V	V_{CC} = 5 V
High-level output voltage	V_{QH}	V_{CC} – 0.4			V	I_Q = – 360 µA
Low-level output voltage, data outputs	V_{QL}			0.45	V	I_Q = 1.6 mA
End of conversion	V_{QL}			0.45	V	I_Q = 1.2 mA
OFF-state output current (high impedance-state)	I_{QZ}			3	µA	V_Q = 5 V
Output current	I_{QZ}			– 3	µA	V_Q = 0
Control input current at max. input voltage	I_I			1	µA	V_I = 5 V
Low-level control input current	I_{IL}			– 1	µA	V_I = 0
Supply current	I_{CC}		0.3	3	mA	f_{CLK} = f_{CLK} (typ)
Input capacitance, control inputs	C_I		10	15	pF	T_A = 25 °C
Output capacitance, data outputs	C_Q		10	15	pF	T_A = 25 °C
Resistance between pins 12 and 16	R	1	1000		kΩ	

Characteristics
Analog Multiplexer V_{CC} = 5 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Channel ON-state current[3]	I_{ON}					V_I = 5 V
				2	µA	f_{CLK} = f_{CLK} (typ)
						V_I = 0 V
				– 2	µA	f_{CLK} = f_{CLK} (typ)
Channel OFF-state current	I_{OFF}					V_{CC} = 5 V
			10	200	µA	T_A = 25 °C, V_I = 5 V
						V_{CC} = 5 V
			– 10	– 200	nA	T_A = 25 °C, V_I = 0
				1	µA	V_{CC} = 5 V, V_I = 5 V
				– 1	µA	V_{CC} = 5 V, V_I = 0

For notes refer to 2 pages hereafter.

Characteristics

T_A = 25 °C, V_{CC} = + V_{REF} = 5 V, – V_{REF} = 0 V, f_{CLK} = f_{CLK} (typ), unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage sensitivity[4]	k_{SVS}		± 0.05		%/V	V_{CC} = + V_{REF} = 4.75 V to 5.25 V T_A = – 40 °C to 85 °C
Linearity error[5]				± 0.5	LSB	
Zero error[6] (except SDA 1810 D)				± 0.5	LSB	
Total unadjusted error[7] SDA 0810 N SDA 0810 B SDA 1810 N				± 0.5 ± 0.5 ± 1	LSB LSB LSB	T_A = – 40 °C to 85 °C T_A = – 40 °C to 125 °C T_A = – 40 °C to 85 °C f_{CLK} = 1 MHz
Output enable time **(figure 1)**	t_{en}		80	150	ns	C_L = 50 pF, R_L = 10 kΩ
Output disable time **(figure 1)**	t_{dis}		40	95	ns	C_L = 10 pF, R_L = 10 Ω
Output turn-OFF time **(figure 1)**	t_{OFF}		20	60	ns	C_L = 10 pF, R_L = 10 kΩ
Conversion time[8] SDA 0810	t_{Conv}	15	25	320	µs	f_{CLK} = 1 MHz/ 640 kHz/50 kHz
Conversion time[8] SDA 1810/1810 D	t_{Conv}	15	25	320	µs	f_{CLK} = 2 MHz/ 1280 kHz/100 kHz
Delay time, output EOC[9]	$t_{D\,(EOC)}$	0		200	ns	

Characteristics SDA 1810 D only

T_A = 25 °C, V_{CC} = + V_{REF} = 5 V, – V_{REF} = 0 V, f_{CLK} = 1.28 MHz unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Total Unadjusted Error	*TUE*		± 0.5	± 1.25	LSB	T_A = – 40 °C to 85 °C
Integral nonlinearity	*INL*			± 0.5	LSB	T_A = – 40 °C to 85 °C
Differential nonlinearity	*DNL*		± 0.25	± 0.5	LSB	T_A = – 40 °C to 85 °C
Gain error	*GE*		± 0.125	± 0.5	LSB	T_A = – 40 °C to 85 °C
Zero error	*OFS*		± 0.25	± 1	LSB	T_A = – 40 °C to 85 °C
Sampling rate	f_s			66	kHz	f_{CLK} = 2 MHz
Effective resolution			8.8		bits	f_{AIN} = 30 kHz

For notes refer to next page.

Notes

1) All voltage values refer to the network's ground terminal.

2) Care must be taken that this rating is observed, even during power-up.

3) The channel on-state current is primarily generated by the current of the Schmitt trigger and varies directly with the clock frequency.

4) The supply voltage sensitivity relates to the ability of an A/D converter to maintain accuracy as the supply voltage varies. Supply voltage and + V_{REF} are changing together and the change of accuracy is measured with respect to full-scale deflection.

5) The linearity error is the maximum deviation from a straight line to the end points of the A/D transfer characteristic.

6) The zero error is the difference between the output of an ideal converter and that of the present A/D converter at zero input voltage.

7) The total unadjusted error is the total-of-linearity error, zero error, and full-scale error.

8) SDA 0810: $t_{Conv\ max} = 16 \times 1/f_{CLK}$, $t_{Conv\ min} = 15 \times 1/f_{CLK}$; including sampling time
SDA 1810: $t_{Conv\ max} = 32 \times 1/f_{CLK}$, $t_{Conv\ min} = 30 \times 1/f_{CLK}$; including sampling time

9) Refer to the operating pulse diagram.

10) For typical error versus reference voltage span refer to diagram next page.

11) Input signals with specified slew rates can be converted without external sample-and-hold. Input signals with higher slew rates may cause digital full-scale errors (not SDA 1810 D!) Filtering by a low pass ($R = 2$ kΩ, $C = 100$ nF) or use of an external sample-and-hold is then required.

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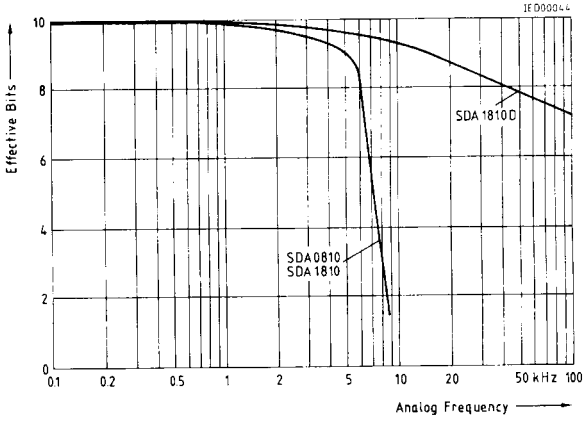
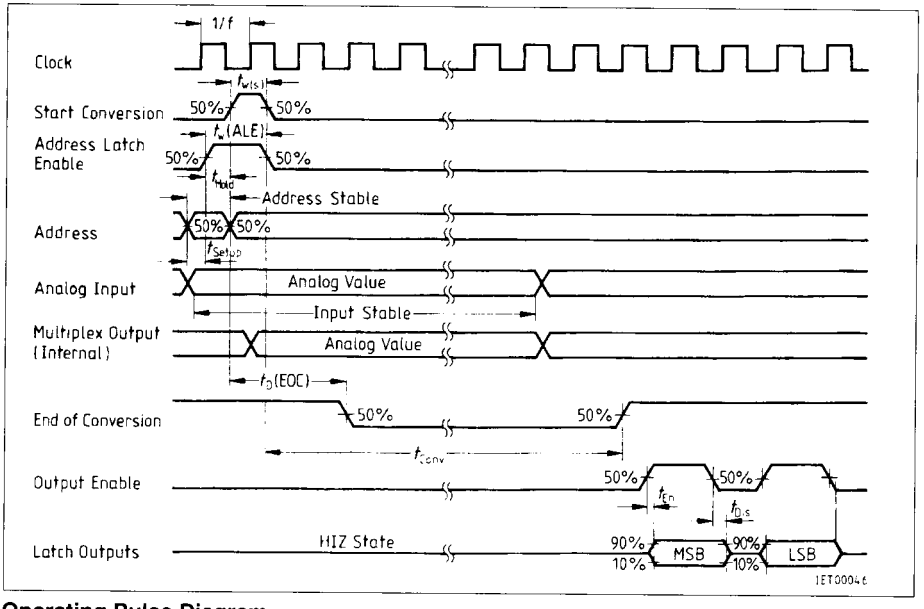
Effective Resolution versus Input Frequency

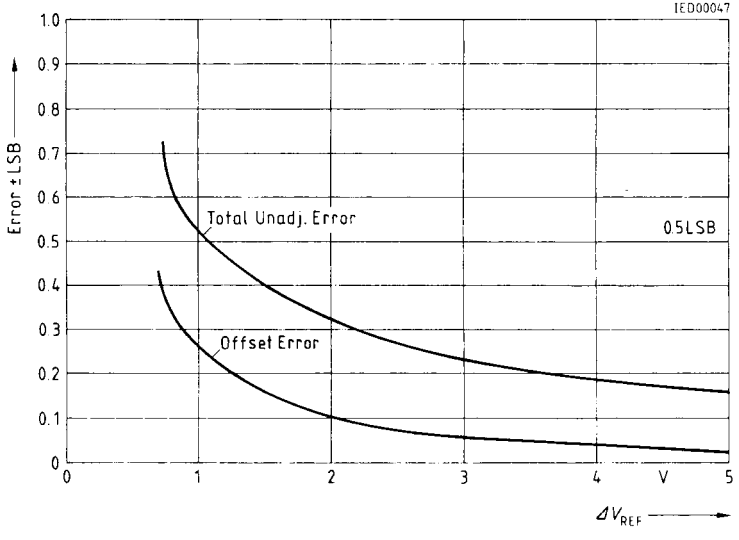
$V_{CC} = 5.0$ V, $+ V_{REF} = 5$ V, $- V_{REF} = 0$ V, $f_{CLK} = f_{CLK\ (typ)}$





Operating Pulse Diagram

Typical Error versus Reference Voltage Span (SDA 0810 A/B/N, SDA 1810 N)
(Total unadjusted error including offset errors, full-scale errors, linearity errors and multiplexer errors). V_{CC} = 5.0 V; $f_{CLK} = f_{CLK\,(typ)}$; $\Delta V_{REF} = +V_{REF} - (-V_{REF})$



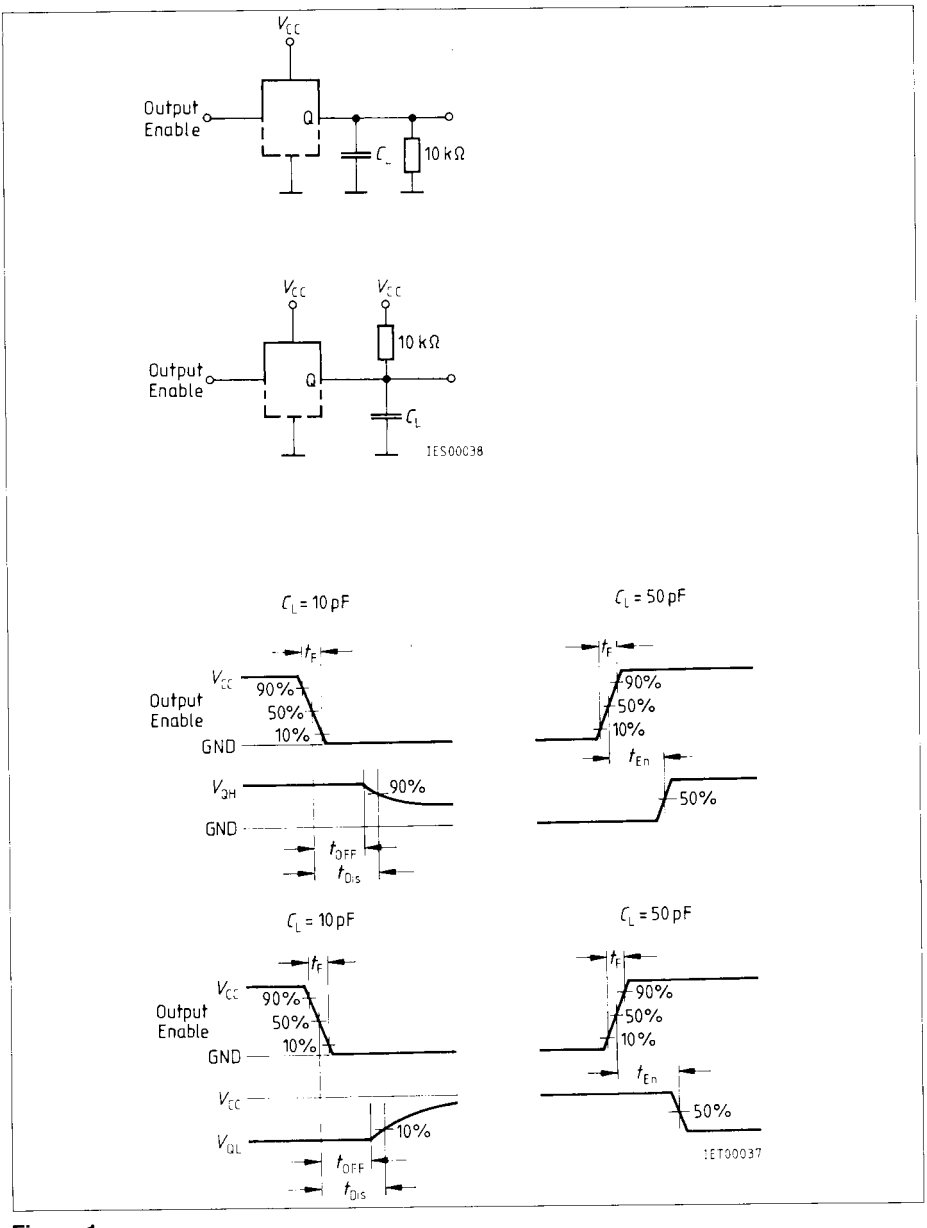


Figure 1
Tristate Measurement Circuits and Pulse Diagrams

Microprocessor Interface

Microprocessor interfacing is straightforward and requires only a few external gates.

INTEL Microprocessors

A typical interface is shown in **figure 2**.

Start of Conversion

A write instruction selects one of the analog input channels and starts the conversion.

Write address: ADC_CS

The end of conversion-signal (EOC) can be used for producing an interrupt in the microprocessor (INT or $\overline{\text{INT}}$).

Reading the Conversion Result

With the first read instruction the high byte is read from the $\overline{\text{ADC\_CS}}$ address, with the second read instruction the low byte is read.

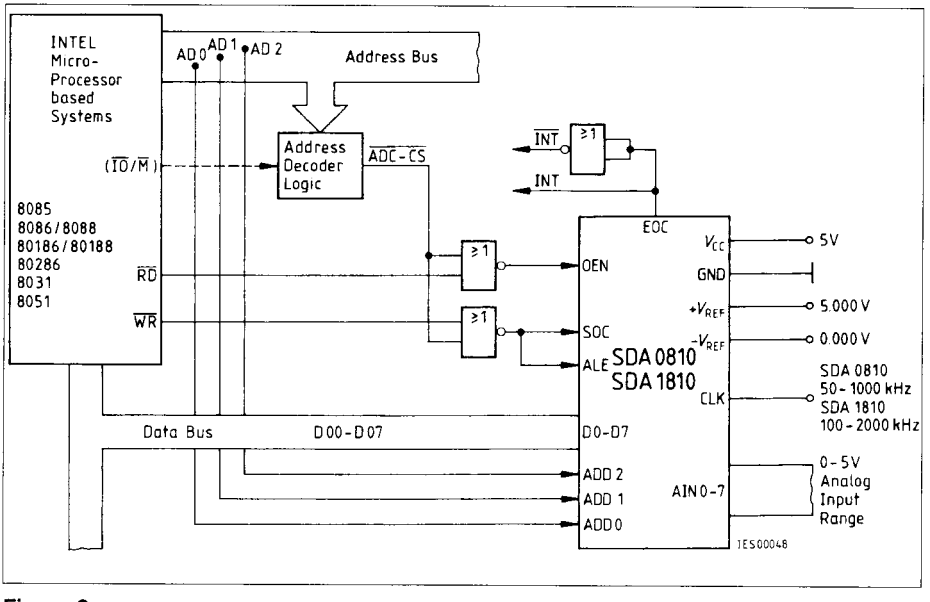


Figure 2

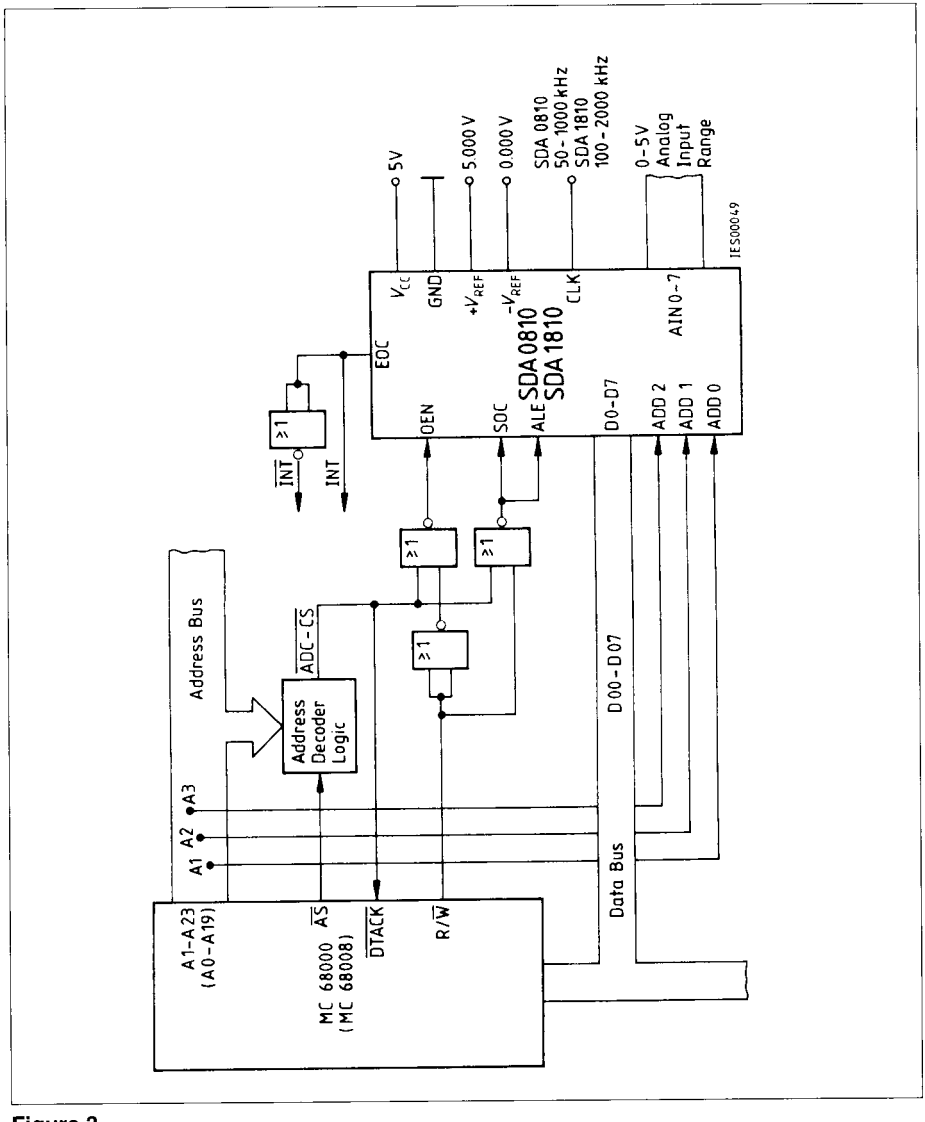


Figure 3
Motorola Microprocessors

A typical interface is shown in **figure 3**.

Application Hints

Power Supply Decoupling

The power supply should be connected with a 10 µF tantalum or an electrolytic capacitor. To ensure good HF performance this capacitor should be connected in parallel with an 0.01 µF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

Reference Voltage

To avoid dynamic errors, a 10 µF tantalum or electrolytic capacitor connected in parallel with an 0.01 µF ceramic capacitor should be placed as close as possible to the component between pins + V_{REF} and – V_{REF}. Also an 0.1 µF ceramic capacitor should be placed between pins – V_{REF} and GND.

Analog Input

The high input impedance of the analog channels AIN 0 to AIN 7 allows simple analog interfacing. Signal sources (– V_{REF} ≤ AIN ≤ + V_{REF}) can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 50 pF, within 4 clock cycles for the SDA 0810 and 8 clock cycles for the SDA 1810.

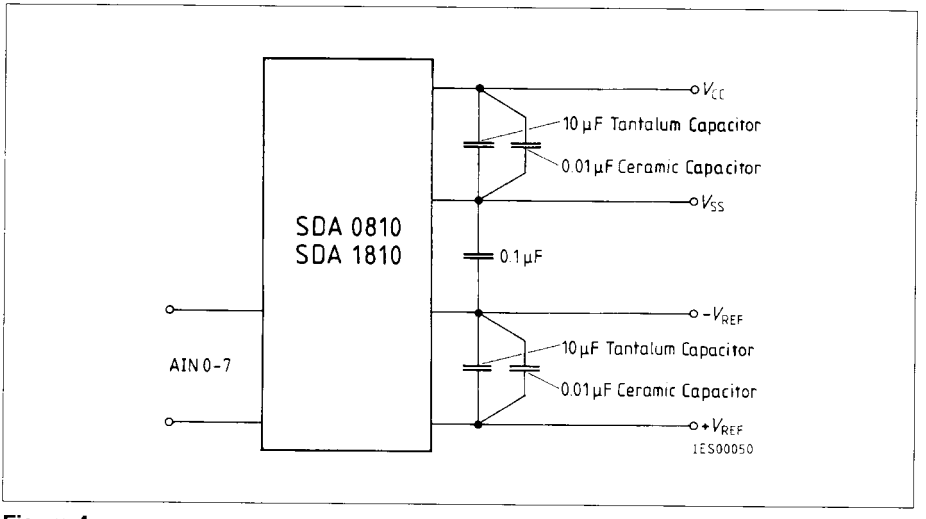


Figure 4
Capacitors