

Features

- Upgraded 8-bit CPU as compared to SAB 8051
- +5V supply voltage
- Program memory either 8 Kbyte internal ROM
or 64 Kbyte external ROM
- Data memory 128 byte internal RAM
64 Kbyte RAM can be connected externally
(internal and external RAM can be used simultaneously)
- 1 μ s internal cycle with 12 MHz clock frequency
- 34 bidirectional I/O ports:
 - two 8-bit ports
 - one 8-bit multifunction port
 - one 8-bit port with 15 mA current sink per output (suited for direct LED MUX control)
 - one serial I²C bus interface, suited for multi-master operation
- Input for direct modulated digital infrared signal processing
(optimum carrier frequency is approx. 30 kHz)
- Powerful interrupt structure with 5 sources and 2 hierarchy levels
- Instruction set downward-compatible with existing programs for SDA 2010/2030/2110
- Power-down mode with internal RAM data retention and reduced power consumption
- 16-bit timer/counter operation
- Instructions for direct multiplication or division, execution time only 4 μ s
- Boolean processor implementable for pure controlling tasks

Circuit description

A special application of the SDA 2082 lies in program development support for the SDA 2040/60/80, the circuitry is shown in the application examples described in the following.

A Siemens microcomputer development system (e.g. SME 232) can be used for SDA 2082 program development and system testing. Powerful edit, assembler and debug programs are available.

An additional application of the SDA 2082 arises for individual control tasks and small quantity series, for which the development of a user-specific program for SDA 2040/60/80 operation is too expensive. An external program memory can be put to good use in this case, also offering short development times and more flexible possibilities for application.

Architecture and instruction set are based on the SAB 8051 microcomputer. In the same manner as the SAB 8051, the SDA 2082 possesses a number of features that facilitate programming:

- variable allocation of RAM
- unrestricted stack location in RAM
- 4 register banks
- special function register
- memory mapped I/O

Individually addressable bits and a Boolean processor enable the programmer to improve software performance. Numeric problems can be solved in binary or in BCD arithmetic. The large number of instructions for processing binary functions also plays a part in increasing the performance of the computer as a controller. All of these features, when used appropriately, lead to a reduction of peripheral hardware, to a simplification of the software, and thus, to a reduction of development and component cost.

The SDA 2082 contains an on-chip 8 Kbyte program memory. Operation is optionally with internal program memory ($\overline{EA}$ = high, pin 35) or external ($\overline{EA}$ = low, pin 35). Furthermore, the SDA 2082 contains an internal 128 byte RAM (an additional 64 Kbyte can be added externally, ref. application example), two 16-bit timers/counters, a nested interrupt structure with two priority levels, and an integrated oscillator. Additionally, the computer can address 64 Kbyte of external data memory. The 34 digital I/O ports comprise four 8-bit ports and a serial interface with data and clock lines. The serial I/O interface fully complies with the I²C multimaster protocol. The IR input P3.0 can process modulated signals with a carrier frequency of approx. 30 kHz. It contains a digital demodulator for deriving the envelope curve of modulated and inverted digital signals. As the digital demodulator is software enabled and disabled, it is also possible to use the IR port as a normal digital, quasi-bidirectional I/O port. The multifunction port P3 comprises two interrupt inputs and two counter inputs.

The instruction set, consisting of 49 one-byte, 46 two-byte, and 16 three-byte instructions, ensures efficient utilization of program memory. If a 12 MHz crystal is used, the execution time for the instructions is either 1 μ s or 2 μ s. The execution time for the very complex instructions for "multiply" and "divide" is only 4 μ s. Information about the number of bytes and the execution time can be found in the SDA 2082 instruction set summary.

Maximum ratings

Voltage between any pin and ground
Total power dissipation
Storage temperature range

V	−0.5 to 7	V
P_{tot}	2	W
T_{stg}	−40 to 125	$^{\circ}C$

Operating range

Supply voltage
Ambient temperature

V_{CC}	$5 \pm 10\%$	V
T_A	0 to 70	$^{\circ}C$

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DC characteristics
 $T_A = 0 \text{ to } 70^\circ\text{C}; V_{CC} = 5 \text{ V} \pm 10\%; V_{SS} = 0 \text{ V}$

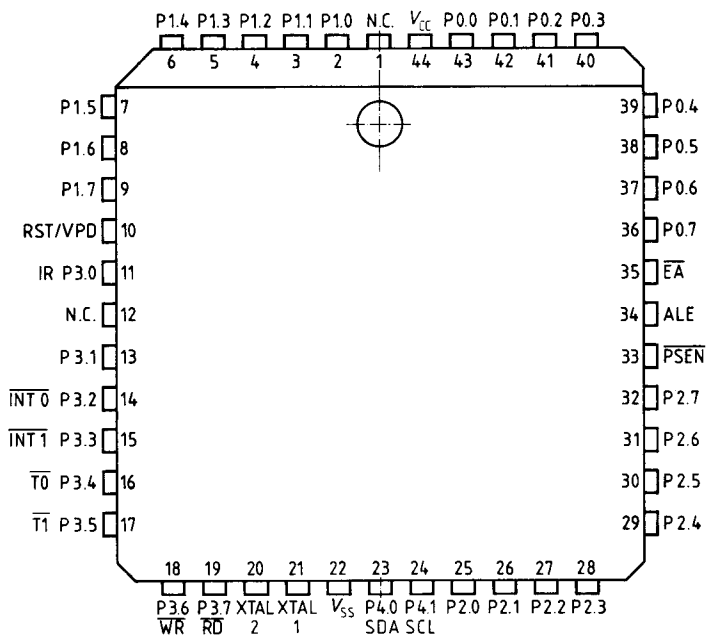
		Test conditions	min	max	
L input voltage (all inputs except XTAL 2, P 4)	V_{iL}		-0.5	0.8	V
L input voltage (XTAL 2)	V_{iL1}		-0.5	0.6	V
L input voltage (P 4)	V_{iL2}		-0.5	1.5	V
H input voltage (except XTAL 2, RST/ V_{PD} , P 4)	V_{iH}		2.0	$V_{CC} + 0.5$	V
H input voltage (XTAL 2)	V_{iH1}		2.5	$V_{CC} + 0.5$	V
H input voltage (RST)	V_{iH2}		2.5	$V_{CC} + 0.5$	V
H input voltage (V_{PD})	V_{iH3}	$V_{CC} = 0$	4.5	5.5	V
H input voltage (P 4)	V_{iH4}		3.0	$V_{CC} + 0.5$	V
L output voltage (port 0)	V_{oL}	$I_{qL3} = 3.2 \text{ A}$		0.45	V
L output voltage (port 0)	V_{oL1}	$I_{qL1} = 15 \text{ mA}$		1.0	V
L output voltage (ports 1, 2, 3, PSEN and ALE)	V_{oL2}	$I_{qL2} = 1.6 \text{ mA}$		0.45	V
L output voltage (port 1)	V_{oL3}	$I_{qL3} = 7.5 \text{ mA}$		1.0	V
L output voltage (port 4)	V_{oL4}	$I_{qL4} = 3.0 \text{ mA}$		0.4	V
H output voltage (ports 1, 2 and 3)	V_{oH}	$I_{qH} = -80 \mu\text{A}$	2.4		V
H output voltage (port 0, PSEN and ALE)	V_{oH1}	$I_{qH1} = -400 \mu\text{A}$	2.4		V
Current of internal pull-up resistance (P 1, P 2, P 3)	I_{LQ}	$0.45 \text{ V} \leq V_{IN} = V_{CC}$	-800		μA
Leakage current of outputs	I_{LQ1}	$0.45 \text{ V} \leq V_{IN} = V_{CC}$		± 10	μA
Current consumption (all outputs disconnected)	I_{CC}			150	mA
Current consumption (power-down mode)	I_{PD}	$V_{CC} = 0 \text{ V}, V_{PD} = 5 \text{ V}$		20	mA
Capacitance of inputs/outputs	C_{iQ}	$f_C = 1 \text{ MHz}$		10	pF

AC characteristics
 $T_A = 0 \text{ to } 70^\circ\text{C}; V_{CC} = 5 \text{ V} \pm 10\%; V_{SS} = 0 \text{ V}$
 $C_L = 100 \text{ pF}$ (for port 0, ALE and PSEN output)

 $C_L = 80 \text{ pF}$ (for all other outputs)

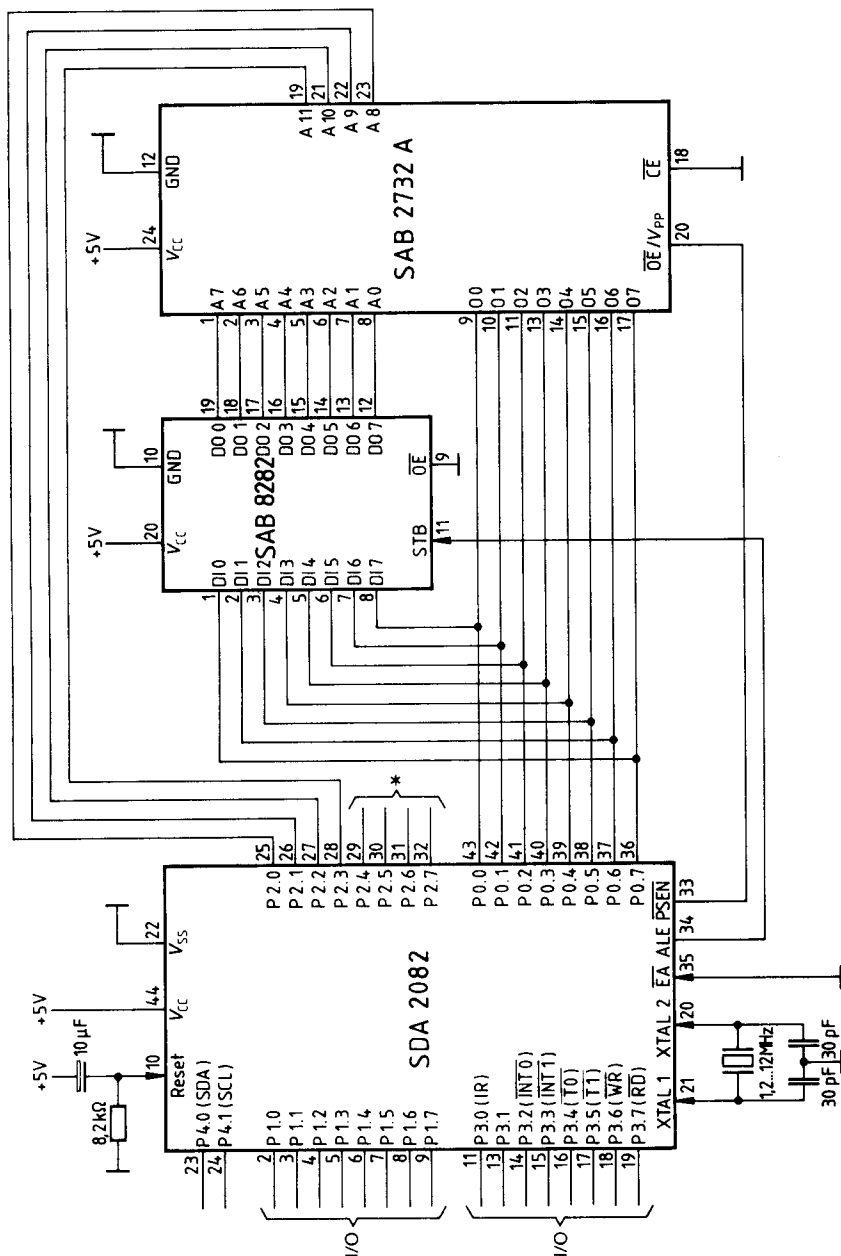
		Maximum ratings			
		Variable clock $1/t_{CLCL} = 1.2\text{--}12 \text{ MHz}$		12 MHz clock	
		min	max	min	max
Cycle time of oscillator	t_{CLCL}	83	833.3	83	ns
Min. cycle period	t_{CY}	12 t_{CLCL}	12 t_{CLCL}	1000	ns
ALE pulse width	t_{LHLL}	2 t_{CLCL}	40	127	ns
RD pulse width	t_{RLRH}	6 t_{CLCL}	100	400	ns
WR pulse width	t_{WLWH}	6 t_{CLCL}	100	400	ns

Pin configuration

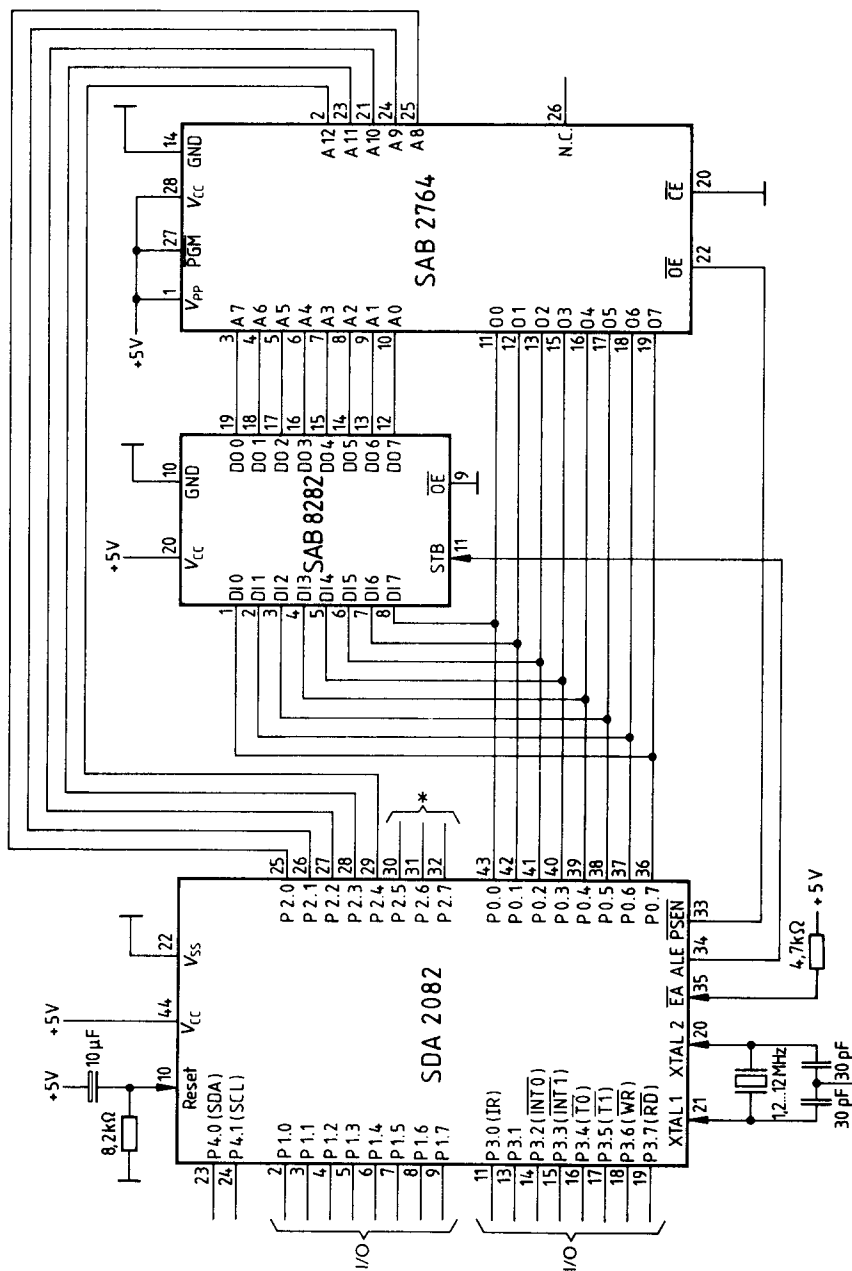


Pin description	
Symbol	Function
V_{SS}	GND 0 V
V_{CC}	+5 V
Port 0	Bidirectional 8-bit port with open drain outputs with 3.2 mA current sink at 0.45 V and 15 mA current sink at 1.0 V for direct LED control (static or MUX operation).
Port 1	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V and 7.5 mA current sink at 1.0 V for direct LED display.
Port 2	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V.
Port 3	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V. Also includes the inputs of the various interrupt and time controls. For a program-controlled enabling of the function, the corresponding latch must be active high. Allocation of the special function registers is as follows: – IR (P 3.0) Input of the digital demodulator to generate an envelope curve of a standard modulated IR signal – $\overline{INT\ 0}$ (P 3.2) Input for interrupt 0 or for enabling/disabling the counter input T 0 – $\overline{INT\ 1}$ (P 3.3) Input for interrupt 1 or for enabling/disabling the counter input T 1 – $\overline{T0}$ (P 3.4) Counter input T 0 – $\overline{T1}$ (P 3.5) Counter input T 1 – $\overline{WR}$ (P 3.6) Write strobe for external data memory (RAM) – $\overline{RD}$ (P 3.7) Read strobe for external data memory
Port 4	Bidirectional 2-bit port with 3 mA current sink at 0.4 V. Port 2 contains a bidirectional, serial interface with DATA (SDA, pin 21) and CLOCK line (SCL, pin 22). The serial interfaces fully meet the requirements of the I ² C bus protocol.
RST/ V_{PD}	At a connected supply voltage $V_{CC} = 5$ V, an edge transition from low to high (at approximately 3 V) resets the SDA 2082, i.e. the user program starts with address 0. When $V_{PD} =$ high (approx. +5V), a drop in V_{CC} triggers the processor's transition into the power-down mode. In this case, a current supply of max. 20 mA is provided to the RAM via pin RST/ V_{PD} . In the case $V_{PD} = 0$ V and $V_{CC} = 5$ V, the RAM is supplied via V_{CC} .
ALE	Address Latch Enable output for controlling external memory access during normal operation.
XTAL1	Oscillator input. Crystal or external source can be used
XTAL2	Oscillator output; required when crystal is used
PSEN	Program Store Enable output for external memory access
EA	External Access input; selects program memory operating mode EA high means internal program memory (8 Kbytes), EA low means external program memory (max. 64 Kbytes)

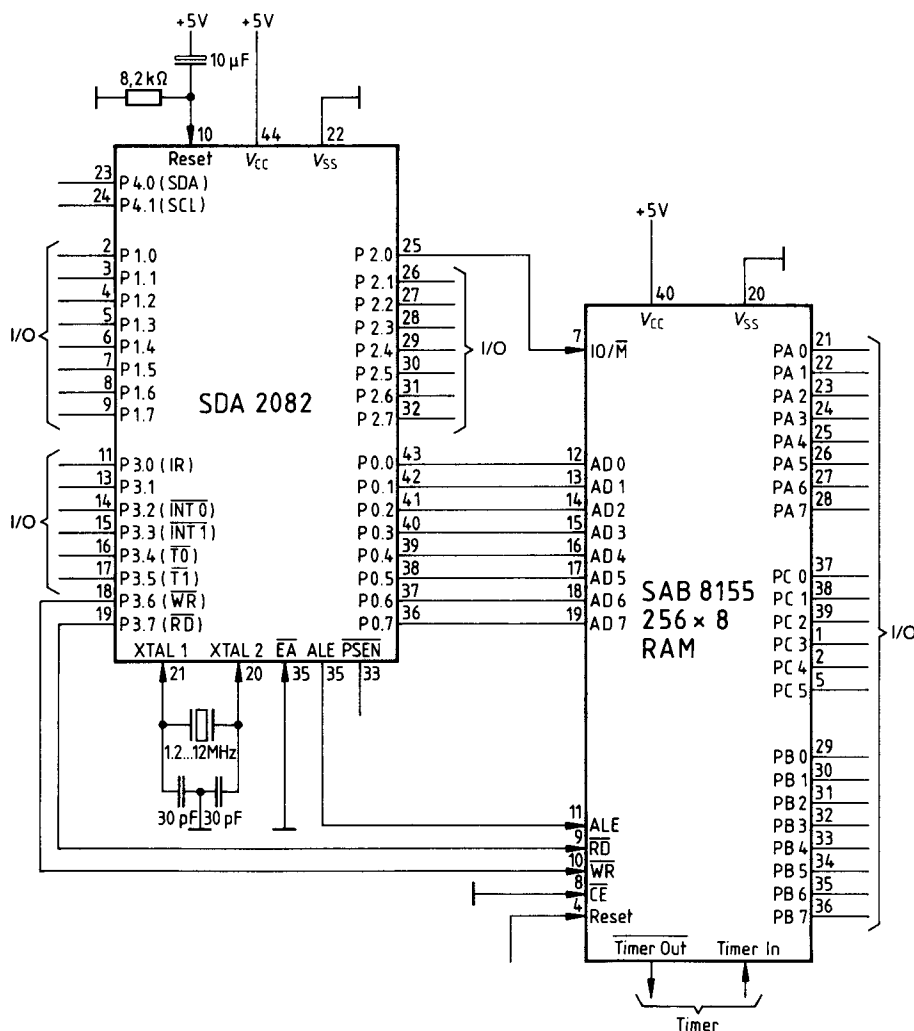
Application example for SDA 2082 with 4 Kbyte external program memory



Application example for SDA 2082 with 8 Kbyte external program memory



Application example for SDA 2082 with additional 256 byte external RAM and port expander



SDA 2082 instruction set

Arithmetic operations

Mnemonic	Description	Bytes	Cycles
ADD A, Rn	Add register to Accumulator	1	1
ADD A, direct	Add direct byte to Accumulator	2	1
ADD A, @ Ri	Add indirect RAM to Accumulator	1	1
ADD A, # data	Add immediate data to Accumulator	2	1
ADDC A, Rn	Add register to Accumulator with Carry flag	1	1
ADDC A, direct	Add direct byte to A with Carry flag	2	1
ADDC A, @ Ri	Add indirect RAM to A with Carry flag	1	1
ADDC C, # data	Add immediate data to A with Carry flag	2	1
SUBB A, Rn	Subtract register from A with Borrow	1	1
SUBB A, direct	Subtract direct byte from A with Borrow	2	1
SUBB A, @ Ri	Subtract indirect RAM from A with Borrow	1	1
SUBB A, # data	Subtract immediate data from A with Borrow	2	1
INC A	Increment Accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @ Ri	Increment indirect RAM	1	1
DEC A	Decrement Accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @ Ri	Decrement indirect RAM	1	1
INC DPTR	Increment Data Pointer	1	2
MUL AB	Multiply A&B	1	4
DIV AB	Divide A&B	1	4
DA A	Decimal Adjust Accumulator	1	1

SDA 2082 instruction set**Logical operations**

Mnemonic	Description	Bytes	Cycles
ANL A, Rn	AND register to Accumulator	1	1
ANL A, direct	AND direct byte to Accumulator	2	1
ANL A, @ Ri	AND indirect RAM to Accumulator	1	1
ANL A, # data	AND immediate data to Accumulator	2	1
ANL direct, A	AND Accumulator to direct byte	2	1
ANL direct, # data	AND immediate data to direct byte	3	2
ORL A, Rn	OR register to Accumulator	1	1
ORL A, direct	OR direct byte to Accumulator	2	1
ORL A, @ Ri	OR indirect RAM to Accumulator	1	1
ORL A, # data	OR immediate data to Accumulator	2	1
ORL direct, A	OR Accumulator to direct byte	2	1
ORL direct, # data	OR immediate data to direct byte	3	2
XRL A, Rn	Exclusive-OR register to Accumulator	1	1
XRL A, direct	Exclusive-OR direct byte to Accumulator	2	1
XRL A, @ Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL A, # data	Exclusive-OR immediate data to Accumulator	2	1
XRL direct, A	Exclusive-OR Accumulator to direct byte	2	1
XRL direct, # data	Exclusive-OR immediate data to direct	3	2
CLR A	Clear Accumulator	1	1
CPL A	Complement Accumulator	1	1
RL A	Rotate Accumulator left	1	1
RLC A	Rotate A left through the Carry flag	1	1
RR A	Rotate Accumulator right	1	1
RRC A	Rotate A right through Carry flag	1	1
SWAP A	Swap nibbles within the Accumulator	1	1

SDA 2082 instruction set

Data transfer operations

Mnemonic	Description	Bytes	Cycles
MOV A, Rn	Move register to Accumulator	1	1
MOV A, direct	Move direct byte to Accumulator	2	1
MOV A, @ Ri	Move indirect RAM to Accumulator	1	1
MOV A, # data	Move immediate data to Accumulator	2	1
MOV Rn, A	Move Accumulator to register	1	1
MOV Rn, direct	Move direct byte to register	2	2
MOV Rn, # data	Move immediate data to register	2	1
MOV direct, A	Move Accumulator to direct byte	2	1
MOV direct, Rn	Move register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	2
MOV direct, @ Ri	Move indirect RAM to direct byte	2	2
MOV direct, # data	Move immediate data to direct byte	3	2
MOV @ Ri, A	Move Accumulator to indirect RAM	1	1
MOV @ Ri, direct	Move direct byte to indirect RAM	2	2
MOV @ Ri, # data	Move immediate data to indirect RAM	2	1
MOV DPTR, # data 16	Load Data Pointer with a 16-bit constant	3	2
MOVC A @ A + DPTR	Move Code byte relative to DPTR to Accumulator	1	2
MOVC A @ A + PC	Move Code byte relative to PC to Accumulator	1	2
MOVX A, @ Ri	Move External RAM (8-bit addr) to Accumulator	1	2
MOVX A, @ DPTR	Move External RAM (16-bit addr) to Accumulator	1	2
MOVX @ Ri, A	Move A to External RAM (8-bit addr)	1	2
MOVX @ DPTR, A	Move A to External RAM (16-bit addr)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with Accumulator	1	1
XCH A, direct	Exchange direct byte with Accumulator	2	1
XCH A, @ Ri	Exchange indirect RAM with Accumulator	1	1
XCHD A, @ Ri	Exchange low-order digital indirect RAM with A	1	1

SDA 2082 instruction set**Boolean variable manipulation**

Mnemonic	Description	Bytes	Cycles
CLR C	Clear Carry flag	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set Carry flag	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement Carry flag	1	1
CPL bit	Complement direct bit	2	1
ANL C, bit	AND direct bit to Carry flag	2	2
ANL C,/bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to Carry flag	2	2
ORL C,/bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry flag	2	1
MOV bit, C	Move carry flag to direct bit	2	2

SDA 2082 instruction set**Program control operations**

Mnemonic	Description	Bytes	Cycles
ACALL addr 11	Absolute subroutine call	2	2
LCALL addr 16	Long subroutine call	3	2
RET	Return from subroutine	1	2
RETI	Return from interrupt	1	2
AJMP addr 11	Absolute jump	2	2
LJMP addr 16	Long jump	3	2
SJMP rel	Short jump (relative addr)	2	2
JMP @ A + DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if Accumulator is zero	2	2
JNZ rel	Jump if Accumulator is not zero	2	2
JC rel	Jump if Carry flag is set	2	2
JNC rel	Jump if Carry flag is not set	2	2
JB bit, rel	Jump if direct bit set	3	2
JNB bit, rel	Jump if direct bit not set	3	2
JBC bit, rel	Jump if direct bit is set and clear bit	3	2
CJNE A, direct, rel	Compare direct to A and jump if not equal	3	2
CJNE A, # data, rel	Compare immediate to A and jump if not equal	3	2
CJNE Rn, # data, rel	Compare immediate to register and jump if not equal	3	2
CJNE @ Ri, # data, rel	Compare immediate to indirect and jump if not equal	3	2
DJNZ Rn, rel	Decrement register and jump if not zero	2	2
DJNZ direct, rel	Decrement direct and jump if not zero	3	2
NOP	No operation	1	1

Symbols and abbreviations

A	Accumulator	Rr	Register label (r = 0-7)
adr	11-bit program memory address	Sn	S interface label (n = 0; 1)
CNT	Event counter	T	Timer
DA	D/A converter indication	T0, T1	Test 0, test 1
data	8-bit binary number	#	Refers to immediate data
P	Mnemonic for "in page" operation	@	Refers to indirect addressing
Pp	Port label (p = 0-3)		