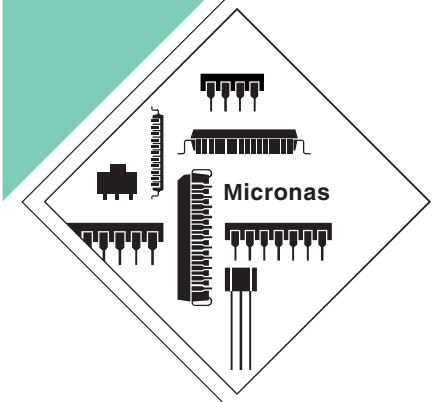

APPLICATION NOTE IC

SDA 555xFL TVText Pro Flash Programming Manual

Edition Dec. 19, 2001
6251-556-2AN

MICRONAS

Contents

TVText Pro Flash Programming Manual

1. Introduction

This manual describes the Flash variant of the TVText Pro family. For complete device reference, please refer to the SDA 55xx TVText Pro data sheet. The device has all the features of the SDA 55xx family and offers up to 128 KByte of Flash ROM to store the application software.

The SDA 55xxFL operates with a dual supply of 3.3 V and 2.5 V. DC characteristics on programming pins are the same as for normal TVText Pro port pins. No additional voltages are required for programming or erasing.

Flash ROM memories have access times in the range of x nsec. This allows the microcontroller to access Flash memory with nearly identical timing compared to the normal Mask ROM on chip.

For the programming process, the device uses a set of programming commands written to command registers for programming, erasing, and reading the data. Commands once written execute inside the flash module without external support to achieve the desired result.

The SDA 55xxFL provides a detection mechanism whereby user can read a test bit to determine whether the current program or erase operation has been completed or not.

An automatic low voltage protection circuit inhibits any write or erase operation if the supply voltage falls below a defined minimum level.

1.1. Flash Features

- Up to 128 KByte of integrated Flash ROM
- JEDEC (Joint Electron Device Engineering Council) compatible command set.
- Embedded program and erase logic.
- Up to 100,000 program/erase cycles.
- Complete flash erase mode.
- Command in progress detection.
- Low power protection
- Fast access time

2. Flash Mode

The flash programming interface (FPI) makes it possible to program the on-chip flash ROM. FPI is not active during normal device operation. It is activated by applying a sequence of signals as discussed below.

To activate the FPI, device $\overline{RST}$ pin is driven low, along with the low signal on P1.7 (fmod).

After a defined time period (see Fig. 4–3 on page 7), P3.6 is driven low to enter the FPI mode. Note that under normal reset sequence, it is forbidden to pull P3.6 low.

Note that Port 1.6 should by left open for proper operation.

Once the FPI interface is active, the ports P0 and P1 are used for flash programming, bypassing the normal port logic.

2.1. Flash Addressing

Address location of the flash memory can be inserted 8 bits at a time through port P0. P0 is shared for data and address insertion. To avoid bus conflict, the Ddir (Data direction signal for data buffer) must be driven high while writing the addresses to the address latch. The address bits are grouped: A0-A7, A8-A15, A16. The address select bits, ASEL0 and ASEL1, select the group of address bits which would be latched with the negative transition of ASEN (address select enable).

The address select bit combinations are shown in Table 2–1.

Please refer to the timing diagram illustrating the address and data bit insertion (Fig. 4–4 on page 7).

Once all the address bits A0-A16 have been set to a desired address, all the address group bits need not be changed; for example, incrementing the address from 0000h to 0001h, only A0-A7 need to be updated to access the next memory location.

Table 2–1: Address select bit combinations

Address Range	ASEL1	ASEL0
A0-A7	0	0
A8-A15	0	1
A16	1	0

2.2. Flash Data

Data bits (D0 - D7) are also read/write through port 0. The control signal associated with the data are $\overline{RD}$, $\overline{WR}$ and Ddir, where $\overline{RD}$ performs read from the flash memory and makes the result available at P0, and $\overline{WR}$ performs write to the flash memory of the data available on P0. Before the read or write operation is performed, Ddir (data direction) must be appropriately set, which selects the direction of the data buffer. Ddir = 0 means data can be read from the flash ROM and Ddir = 1 means data can be written to the flash ROM.

Note that before starting a read or write signal, the address must be set to the proper value as described above.

Note that either read or write or ASEN must be active to perform the desired operation. In order to have successful operation, two or more of these signals must not be active at the same time.

2.3. Internally Generated Control Signals

FPI internally generates the following signals to the Flash ROM.

2.3.1. Output Enable and Write Signals

Flash $\overline{OE}$ (output enable) and WR are associated with the Ddir, $\overline{RD}$ and $\overline{WR}$ pins of FPI. $\overline{OE}$ is also generated during normal operation to access instructions/data from the flash ROM by the CPU.

2.3.2. Flash Chip Enable

$\overline{CE}$ (chip enable) enables the flash module. Flash module is enabled during normal operation of the device and during the flash programing mode.

During normal reset, idle and power down mode, the flash module is disabled to save power consumption.

2.3.3. Flash ROM Reset

The flash module is reset during normal external reset (reset pin) and watch dog timer reset. During the flash programing mode, the flash module is not reset.

3. Flash Programing

3.1. Flash Read

During the flash programing mode, to read data, the address bits must be inserted as discussed in Section 2.2. Ddir must be driven low; read signal $\overline{RD}$ activation then starts the flash read cycle. No additional commands are necessary to perform this operation.

In the normal mode, the microcontroller internally generates the read signal to fetch instructions from the flash ROM.

3.2. Flash Write

During the flash programing mode, to write data, the address bits must be inserted as discussed in Section 2.2. Ddir must be driven high; write signal $\overline{WR}$ activation then starts the flash write cycle internally. Writing here refers to writing a command or command sequence. These commands are written to the internal programming registers which initiate the action (program/erase) based on the command.

3.3. Command Interface

Commands are written to the specific addresses (which do not occupy the flash ROM address space) with a specific data sequence. For specific commands, please refer to the appropriate flash specification.

3.3.1. Erase Flash

Erase flash command sequence erases the complete flash memory. It is a six cycle operation requiring six successive write operations to the command registers. The command sequence consists of two unlock write cycles, followed by a set up command. Two additional unlock write cycles are then followed to complete the flash erase command. Once the complete command sequence is written to the command register, internal circuitry starts the erase operation and does not require any further external support.

While the erase flash command is in progress, any further commands written to the chip are ignored.

When the erase operation is completed, it is indicated by raising the D7 to 1. After the erase command is finished, the flash ROM is automatically brought back into read access mode.

As a result of erase flash, complete memory is initialized, each bit holds logic level 1.

3.3.2. Program Flash

The program command sequence programs one data byte into the specified location of the the Flash ROM. It is a four cycle operation requiring four successive writes to the command register. The command sequence consists of two unlock write cycles, followed by program setup command, and data write cycle.

Once the complete command sequence is written to the command register, internal circuitry starts the program operation and does not require any further external support.

While the program flash command is in progress, any further commands written to the chip are ignored.

Please note that a data bit "0" cannot be programmed back to "1". Only an erase algorithm can set the data bit to "1". Attempting to do so may result in a device hang up.

4. Specification

4.1. Pin Configuration (PSDIP52)

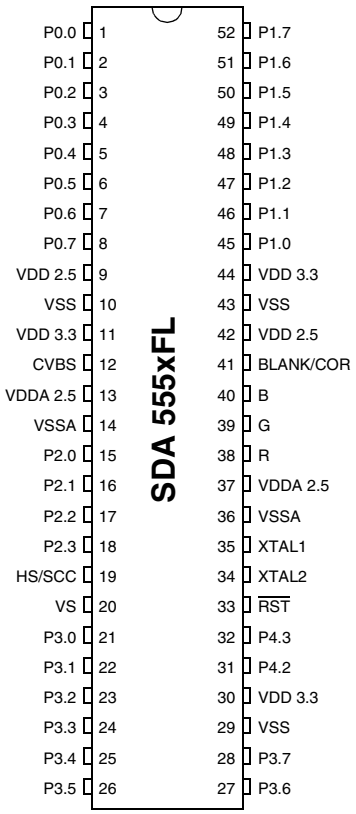

Fig. 4–1: PSDIP52 package

4.2. Pin Configuration (PMQFP64)

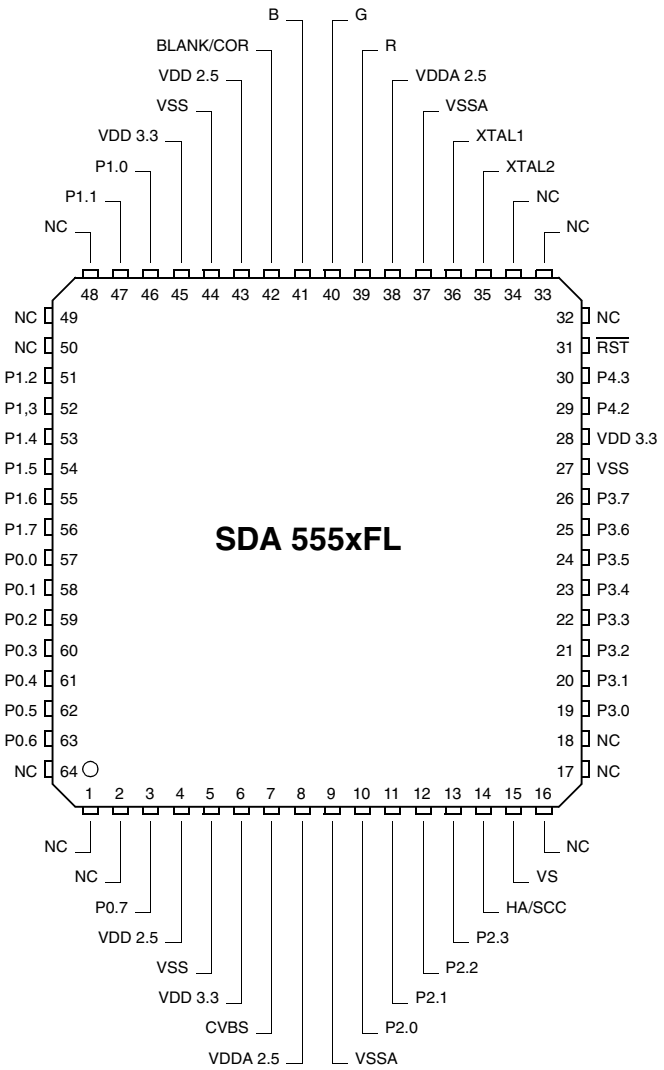

Fig. 4–2: PMQFP64 package

4.3. Multifunction Pins for Flash Mode

Table 4–1 describes the alternate modes of Port 0 and Port 1 in the flash programming mode. The alternate modes are described in the following sections. For normal functionality of port pins, please refer to the SDA 55xx data sheet.

Table 4–1: Alternate modes of Port 0 and Port 1 for flash programming

Original mode	P0.0	P0.1	P0.2	P0.3	P0.4	P0.5	P0.6	P0.7	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.7
Alternate Mode 1	D0	D1	D2	D3	D4	D5	D6	D7	wr	rd	Ddir	Asel1	Asel0	Asen	fmod
Alternate mode 2	A0	A1	A2	A3	A4	A5	A6	A7							
Alternate mode 2	A8	A9	A10	A11	A12	A13	A14	A15							
Alternate mode 3	A16														

4.4. Electrical Characteristics

4.4.1. Characteristics

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_1	Setup time reset(↓) before P1.7(↓) or P3.6(↓)	1000		ns	
t_2	Setup time FPI mode		90	ns	
t_3	Setup time ASEL(stable) before ASEN(↓)	40		ns	
t_4	Hold time ASEL(stable) after ASEN(↓)	40		ns	
t_5	ASEN pulse width	30		ns	
t_6	P0_data(stable) to WR_N()	90		ns	
t_7	P0_data(stable) after WR_N()	40		ns	
t_8	WR_N pulse width	70		ns	
t_9	ASEN(↓) to P0_data(stable)		170	ns	
t_{10}	RD_N(↓) to P0_data(stable)		150	ns	
t_{11}	Ddir(↓) before RD_N(↓)	40		ns	
t_{12}	Ddir rising after RD_N rising	40		ns	

4.4.2. Timing Diagrams

4.4.2.1. Entering FPI Mode

Entering FPI mode requires static low signal on control signals $\overline{RST}$, P1.7, and P3.7.

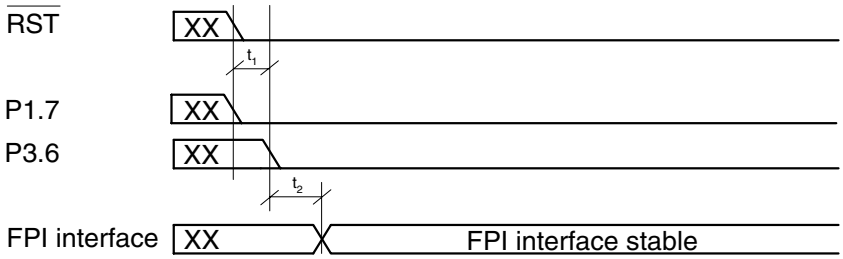

Fig. 4–3: Entering FPI mode

4.4.2.2. Inserting Address and Data

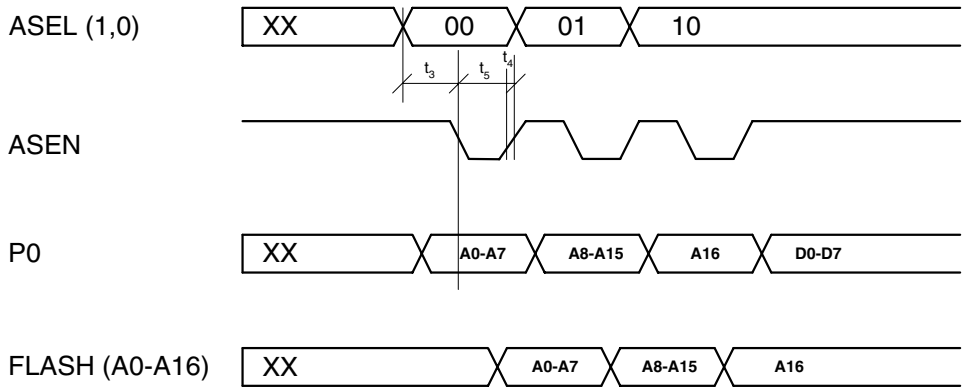

Fig. 4–4: Inserting address and data

4.4.2.3. FPI Write and Read Cycle

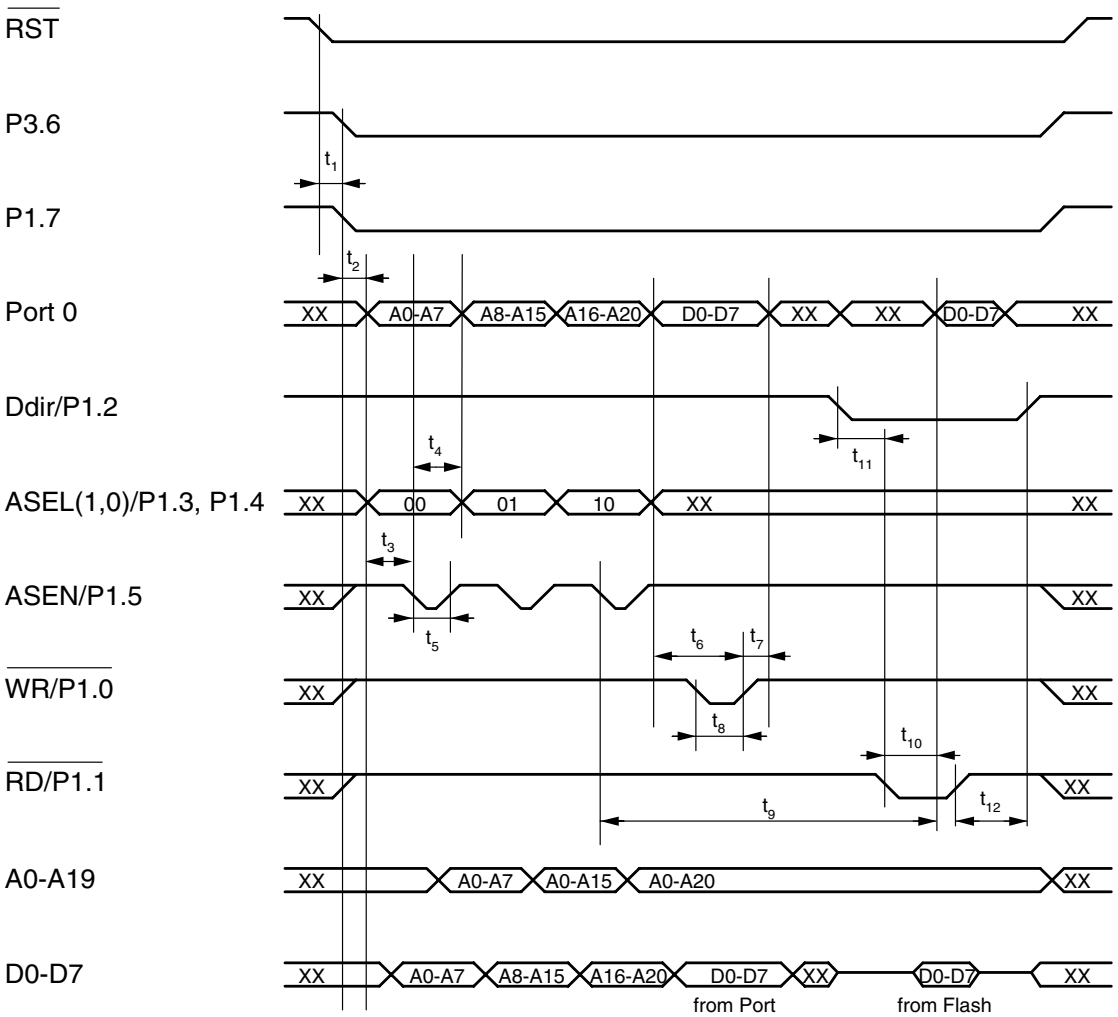

Fig. 4–5: A typical write and read cycle using FPI

5. Application Note History

1. Application Note IC: “SDA 555xFL TVText Pro Flash Programming Manual,” Dec. 19, 2001, 6251-556-2AN. First release of the application note IC.

Micronas GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@micronas.com
Internet: www.micronas.com

Printed in Germany
Order No. 6251-556-2AN