SIEMENS

2.6 MBit Dynamic Sequential Access Memory for Television Applications (TV-SAM) with On-chip Noise Reduction Filter

SDA 9254-2

Preliminary Data

CMOS IC

Features

- Stores a complete video field (4:1:1)
- On chip adaptive recursive noise reduction filter (4:1:1)
- 4 noise reduction classes selectable
- Special noise reduction mode for 4:2:2 applications
- 212 × 64 × 16 × 12-bit organization
- Triple port architecture
- One 16 × 12-bit input shift register
- Two 16 × 12-bit output shift registers
- Shift registers independently and simultaneously accessible (one output shift register is used internally for noise reduction filtering)
- Continuous data flow even at maximum speed
- 40-MHz shift rate - 0.96-Gbit/s total data rate
- All inputs and outputs TTL-compatible
- Tristate outputs
- Random access of groups of 16 × 12 bits for a wide range of applications
- Refresh-free operation possible
- 5 V ± 10 % power supply
- 0 … 70 °C operating temperature range
- Low power dissipation: 700 mW active, 28 mW standby
- Suitable for all common TV standards
- Allows flicker and noise reduction simultaneously with only one field memory
- Applications: TV, VCR, image processing, video printers, data compressors, delay lines, time base correctors, HDTV

P-MQFP-64-1

Type	Ordering Code	Package
SDA 9254-2	on request	P-MQFP-64-1

Functional Description

General

The SDA 9254-2 is a combination of the TV-SAM SDA 9253 and an adaptive recursive filter to achieve a reduction of noise for video signals. To get a closed loop one of the two output ports of the triple port memory is connected internally to the noise reduction filter. External access to this port is not possible. The characteristic of the noise reduction filter is adjustable via three pins (CLASS2, CLASS1, CLASS0).

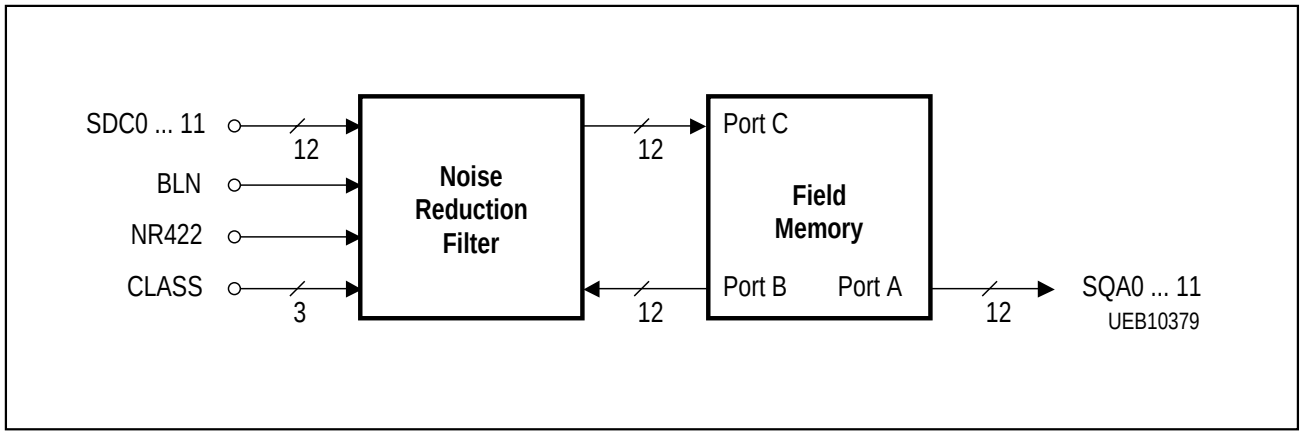


Figure 1
Block Diagram

The memory capacity of the SDA 9254-2 enables a field based filtering of 4:1:1 video signals (pin NR422 = ‘0’). 4:2:2 applications are supported by a special noise reduction mode (pin NR422 = ‘1’). In this mode filtering is applied only to the luminance signal, the chrominance signals are delayed by an internal delay line but remain unfiltered. For the storage of 4 bit planes of the chrominance signal a SDA 9251-2X is requested additionally.

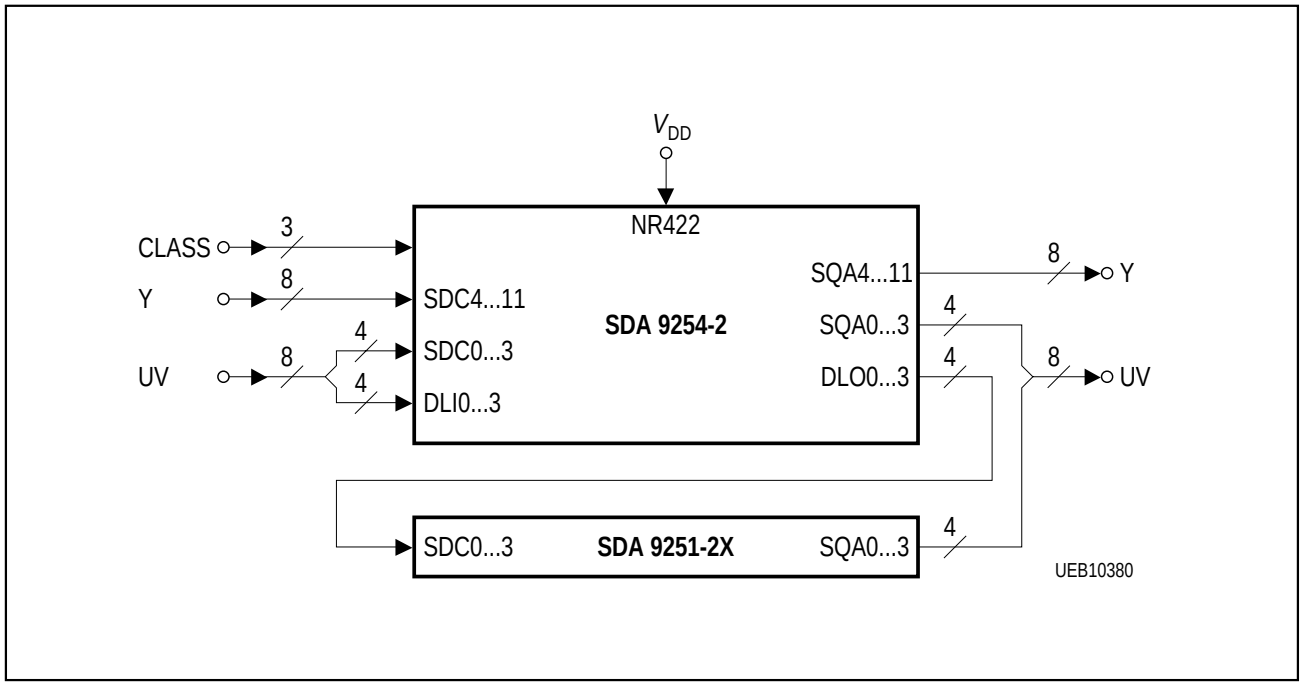


Figure 2
Noise Reduction with 4:2:2 Signals

Adaptive Field Based Noise Reduction

The reduction of noise is performed by recursive filtering. The filter has the following transfer function:

$$H(z) = \frac{K}{1 - \langle 1 - K \rangle \times z^{-1}}$$

$$z = e^{j\omega T_{FLD}}, \qquad T_{FLD} = \text{fielddelay}$$

For K = 1 the transfer function is H(z) = 1, that means no filtering is performed and the input data remains unchanged. For K < 1 noise reduction filtering is activated. The input data and the delayed data from the memory are combined according H(z).

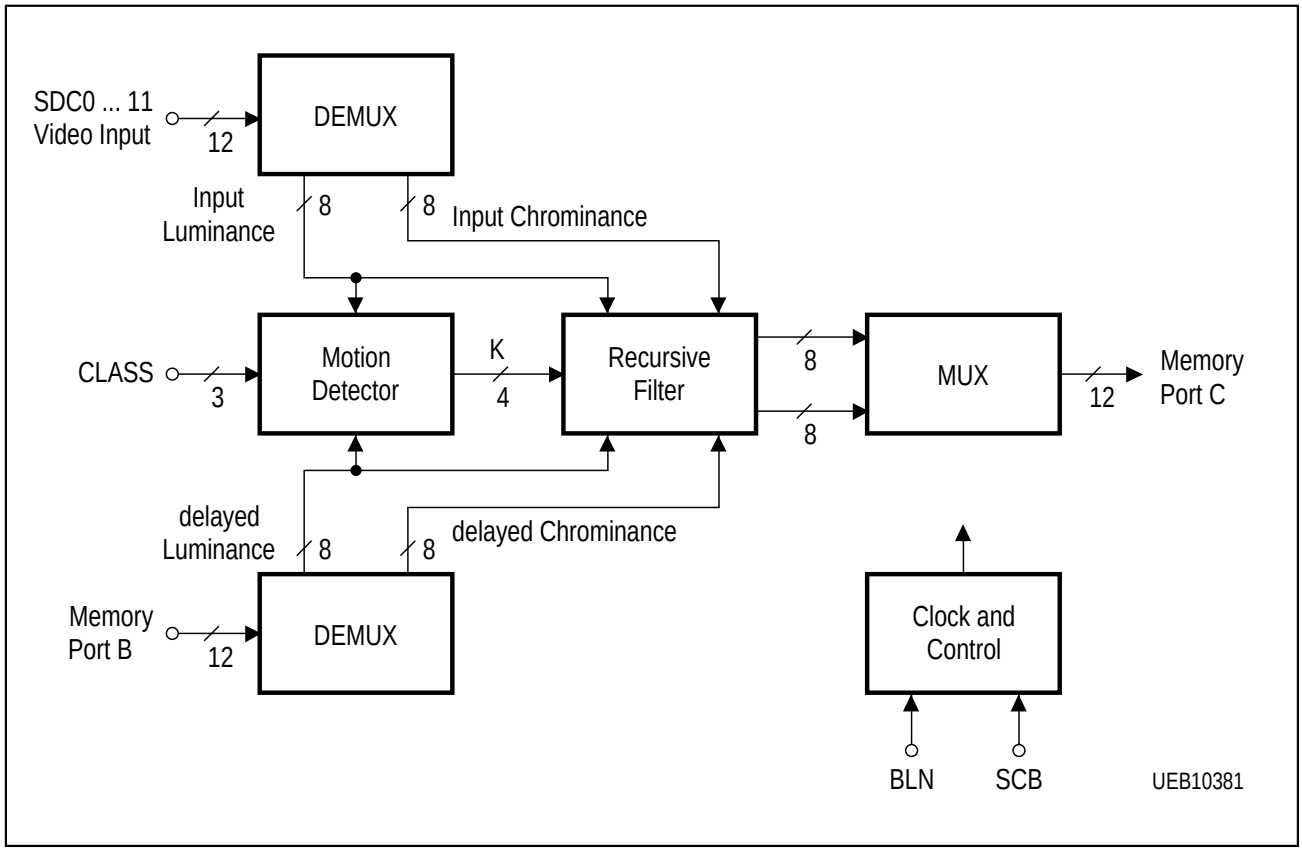


Figure 3
Block Diagram of the Noise Reduction Filtering

To avoid artefacts in moving parts of the picture a motion detector is implemented to control the filter coefficient K according to detected changes between two adjacent fields. The motion detector performs a low pass filtering of the field differences and builds the absolute values. The results control the filter coefficient K by choosing one of 13 predefined values between 1/4 and 1. The characteristic of this assignment influences the amount of noise reduction and is adjustable via the CLASS-pins. The calculation of the filter coefficient is practised for each pixel of the field.

Adjustment of the Characteristic of the Noise Reduction Filter

CLASS2	CLASS1	CLASS0	Amount of Noise Reduction
x	0	0	Low
x	0	1	Low-mid
0	1	0	Mid-high
1	1	0	High
x	1	1	Noise reduction off

These four possible adjustments put a wide field of different intensities of noise reduction at user's disposal.

The recursive filter also enables a reduction of cross color interference because the Motion Detector exploits only luminance data.

The following diagram shows the requested data format for 4:1:1 signals at the input SDC0 … SDC11. The output data format at pins SQA0 … SQA11 corresponds to the input format.

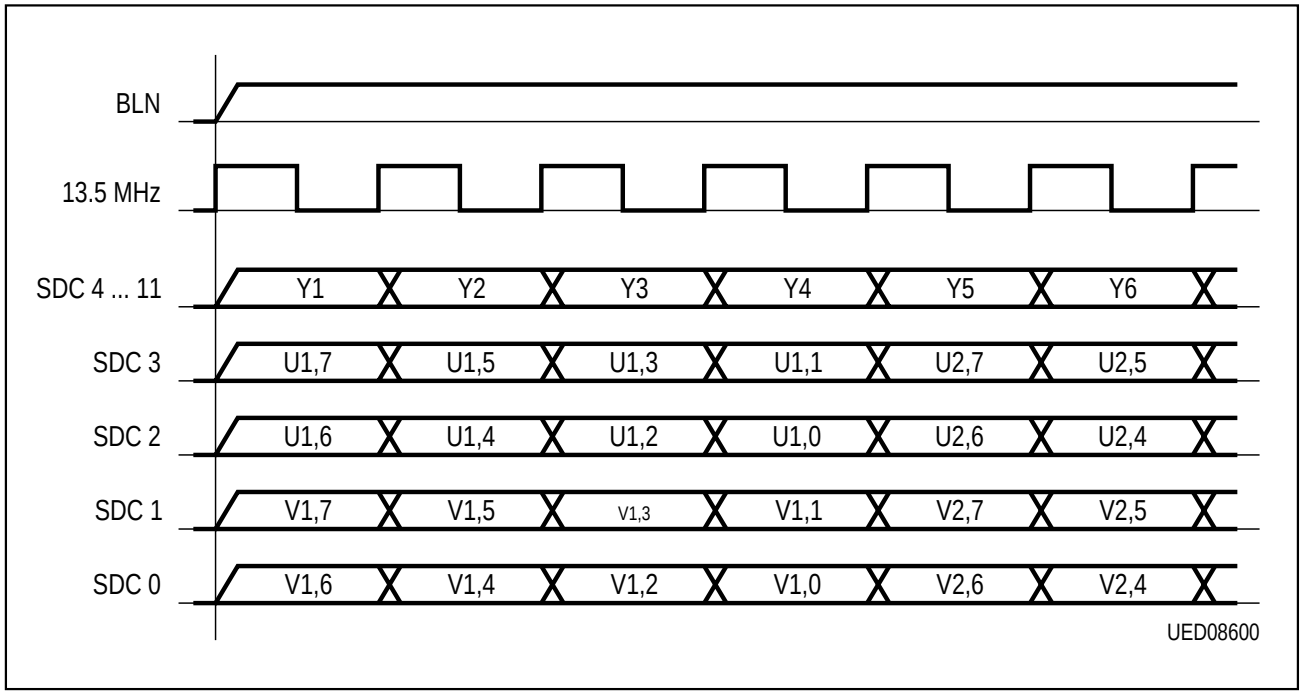


Figure 4
Input Data Format (4:1:1)

Memory

The memory has a capacity of 2605056 bit. It is organized as 212 rows by 64 columns by 16 arrays by 12 bit and allows the storage of the active part of a complete 4:1:1-TV field using a 13.5 MHz sample rate. The memory is fabricated using the same CMOS technology used for 4-Mbit standard dynamic random access memories.

The extremely high maximum data rate is achieved by three internal shift registers, each of 16-bit length and 12-bit width, which perform a serial to parallel conversion between the asynchronous input/output data streams and the memory array. The parallel data transfer from the 16 x 12-bit input shift register C to an addressed location of the memory array and from the memory array to one of the 16 x 12-bit output shift registers A or B is controlled by the serial row-(SAR) and column address (SAC) which contains the desired column address and an instruction code (mode bits) for transfer and refresh.

Circuit Description

Memory Architecture

As shown in the block diagram of the memory part (see **figure 7**), the TV-SAM comprises 192 memory arrays, which are accessed in parallel. Each memory array has a size of 212 rows by 64 columns. The rows and columns of the 192 arrays can be randomly addressed, reading or writing 16 x 12 bits at a time. To obtain the extremely high data rate at the 12-bit wide data input (port C) and outputs (port A and B), a parallel to serial conversion is done using shift registers of 16-bit length and 12-bit width. In this way the memory speed is increased by a factor of 16. (This is independent on the number of ports if the total data rate is regarded.)

Independent operation of the serial input and the two serial outputs is guaranteed by using three shift registers. The decoupling from the common 16 x 12-bit memory data bus is done by three latches which allow a flexible memory timing and a flying real-time data transfer.
A real-time data transfer is necessary to ensure a continuous data flow at the data pins even at maximum clock speed.

To save pins without loosing speed, the TV-SAM is addressed serially using a serial 8-bit row address and a serial 8-bit column address which includes two mode control bits. The serial row and column addresses are converted to parallel addresses internally, then latched and fed to the row and column decoders. The internal memory controller is responsible for the timing of the memory read/write access and the refresh operation.

Data Input (SDC, SCB)

The data pins SDC are connected to the input of the recursive filter. The delay time from SDC to the memory port C caused by the filter amounts 8 periods of the clock SCB. The delay time is to be considered for the generation of the signal $\overline{WT}$ (see **diagram 8**).

Data are shifted into the memory using the serial port C at the rising edge of the shift clock SCB. After 16 clock pulses the data have to be transferred from shift register C to latch C. If more than 16 clock pulses occur before latching the data, only the last sixteen 12-bit data values are accepted.

Data Input (DLI), Data Output (DLO, $\overline{OEDLO}$)

In 4:2:2-mode 4 bitplanes of the chrominance signals are connected to an internal delay line via the pins DLI. After 8 periods of clock SCB the input data are supplied at the delay line output DLO.

Via the output enable $\overline{OEDLO}$ the output buffers can be switched into tristate. In 4:1:1-mode the DLI pins should be connected to GND and pin $\overline{OEDLO}$ should be connected to V_{DD}.

Data Transfer from Shift Register C to Latch C ($\overline{WT}$)

The contents of the shift register C is transferred to latch C at the falling edge of the write transfer signal $\overline{WT}$. If the timing restrictions between $\overline{WT}$ and the clock SCB are respected, a continuous data flow at input port C is possible without loosing data. This transfer operation may be asynchronous to all other transfer operations except for a small forbidden window conditioned by the latch C to memory transfer, see **diagram 4**.

Write Transfer from Latch C to Memory ($\overline{RE}$)

The data of latch C are transferred to the preaddressed location of the memory array at the rising edge of $\overline{RE}$, if the mode bits were set to H (M1) and L (M0), see “Addressing and Mode Control.”

Addressing and Mode Control (SAR, SAC, SCAD, $\overline{RE}$)

The serial 8-bit row address SAR and the 8-bit column address/mode code SAC are serially shifted into the TV-SAM (LSB first) at rising edge of the address clock SCAD. After 8 SCAD cycles, the falling edge of $\overline{RE}$ internally latches SAR and SAC. The column address itself needs only 6 bits. The last 2 bits of SAC are defined as mode bits and determine the read/write and refresh operation of the memory arrays to be triggered by the $\overline{RE}$ signal.

Mode Bit M1	Mode Bit M0	Operation
L	L	Read transfer from memory to latch A
L	H	Read transfer from memory to latch B
H	L	Write transfer from latch C to memory
H	H	Refresh with internal row address

Read Transfer from Memory to Latch A or B ($\overline{RE}$)

Memory data from a preaddressed location are transferred to latch A or B at the falling edge of $\overline{RE}$, depending on the mode control bits, see “Addressing and Mode Control”.

Data Transfer from Latch A to Shift Register A ($\overline{RA}$)

The data of latch A are transferred to shift register A at the falling edge of the read transfer signal $\overline{RA}$. If the timing restrictions between $\overline{RA}$ and the shift clock SCA are taken into account, a continuous data flow at output SQA without interrupts is possible. This transfer operation is independent on all other transfer operations except for a small forbidden time window conditioned by the memory to latch A transfer.

Data Transfer from Latch B to Shift Register B ($\overline{RB}$)

The data of latch B are transferred to shift register B at the falling edge of the read transfer signal $\overline{RB}$. If the timing restrictions between $\overline{RB}$ and the shift clock SCB are taken into account, a continuous data flow at memory output port B without interrupts is possible. This transfer operation is independent on all other transfer operations except for a small forbidden time window conditioned by the memory to latch B transfer.

For correct operation of the recursive filtering the memory output data at port B must be in phase with the input data SDC. This restriction forces a fixed space of time between $\overline{RB}$ and $\overline{WT}$ of 25 clock periods of SCB (see **diagram 8**).

Data Output A (SQA, SCA, $\overline{OEA}$)

Data is shifted out through the serial port A (SQA0 … SQA11) at the rising edge of the shift clock SCA. After 16 clock cycles new data have to be transferred from latch A to shift register A. Otherwise data values are cyclically repeated.

Via the output enable $\overline{OEA}$ the output buffers can be switched into tristate.

The shift clock SCA may be completely independent on the shift clock for port B and C (SCB).

Memory Output (Port B, SCB)

Data is shifted out through the serial port B at the rising edge of the shift clock SCB. After 16 clock cycles new data have to be transferred from latch B to shift register B. Otherwise data values are cyclically repeated. The shift clock SCB is also used for the input port C.

Refresh

Either 256 refresh cycles (refresh with external row address) or read/write cycles on 212 consecutive row addresses beginning with address 0 have to be executed within an 16 ms interval to maintain the data in the memory arrays.

A refresh with internal row adress is determined by the mode control bits, see “Addressing and Mode Control”. In this refresh mode, the row and column addresses are ignored (see **diagram 6a and 6b**).

Initialization

The device incorporates an on-chip substrate bias generator as well as dynamic circuitry. Therefore an initial pause of 200 µs is required after power on, followed by eight $\overline{RE}$-cycles before proper device operation is achieved.

Typical Memory Cycle Sequence

A typical application of the TV-SAM is a real-time noise reduction filtering combined with flicker reduction. This can be achieved, for example, by writing and reading with 13.5-MHz clock rate via port C and B and by simultaneously reading port A with 27-MHz double speed clock. A main cycle of 4 consecutive $\overline{RE}$ cycles of transfer is needed:

1st.	$\overline{RE}$-cycle:	Read transfer from memory to latch A
2nd.	$\overline{RE}$-cycle:	Read transfer from memory to latch B
3rd.	$\overline{RE}$-cycle:	Same as 1st. $\overline{RE}$ cycle
4th.	$\overline{RE}$-cycle:	Write transfer from latch C to memory

Each transfer cycle is preceeded by an address cycle as shown in the diagram page 6:

For the clock rates mentioned this means a serial cycle time of 74 ns at port B and C and 37 ns at port A. The addressing cycle time for each port is given by 16 times the serial data rate. Thus we have an addressing cycle time of approx. 1184 ns for port B and port C. The address for port A must be loaded every 592 ns. Since all addresses are shifted in sequentially, a $\overline{RE}$ cycle time of approx. 296 ns is necessary.

The beginning of a block of 16 serial data at port A or B is determined by $\overline{RA}$ and $\overline{RB}$, respectively. The end of the serial input data block at port C is controlled by $\overline{WT}$. Since $\overline{RA}$, $\overline{RB}$ and $\overline{WT}$ can be independently chosen (except for small forbidden time windows when memory transfers are executed), the serial data streams can be shifted against each other without influencing the $\overline{RE}$ cycles.

For activated noise reduction the timing restrictions for $\overline{RB}$ and $\overline{WT}$ must be considered (see Data Transfer from latch B to Shift Register B).

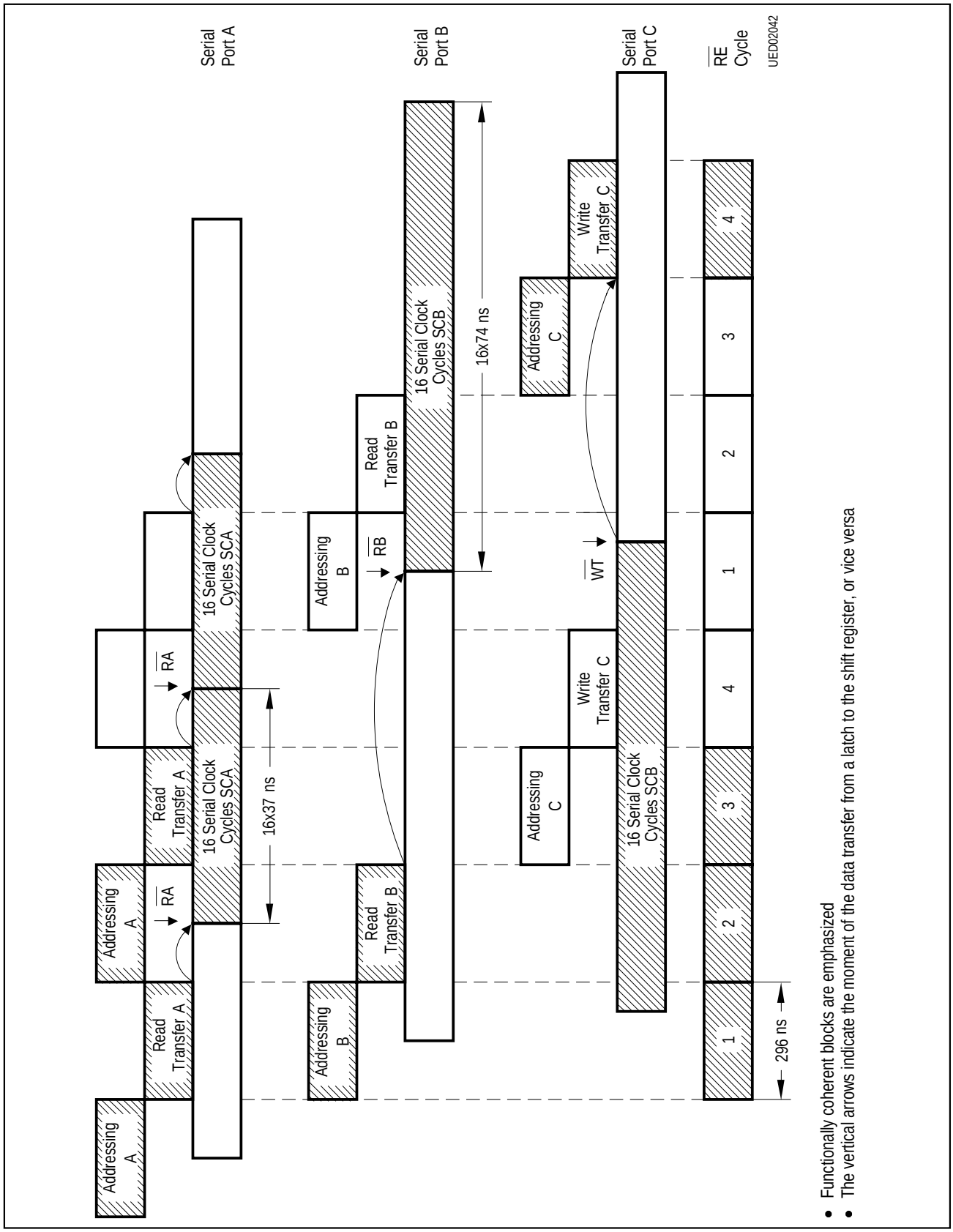


Figure 5
Typical Memory Cycle Sequence

Pin Configuration
(top view)

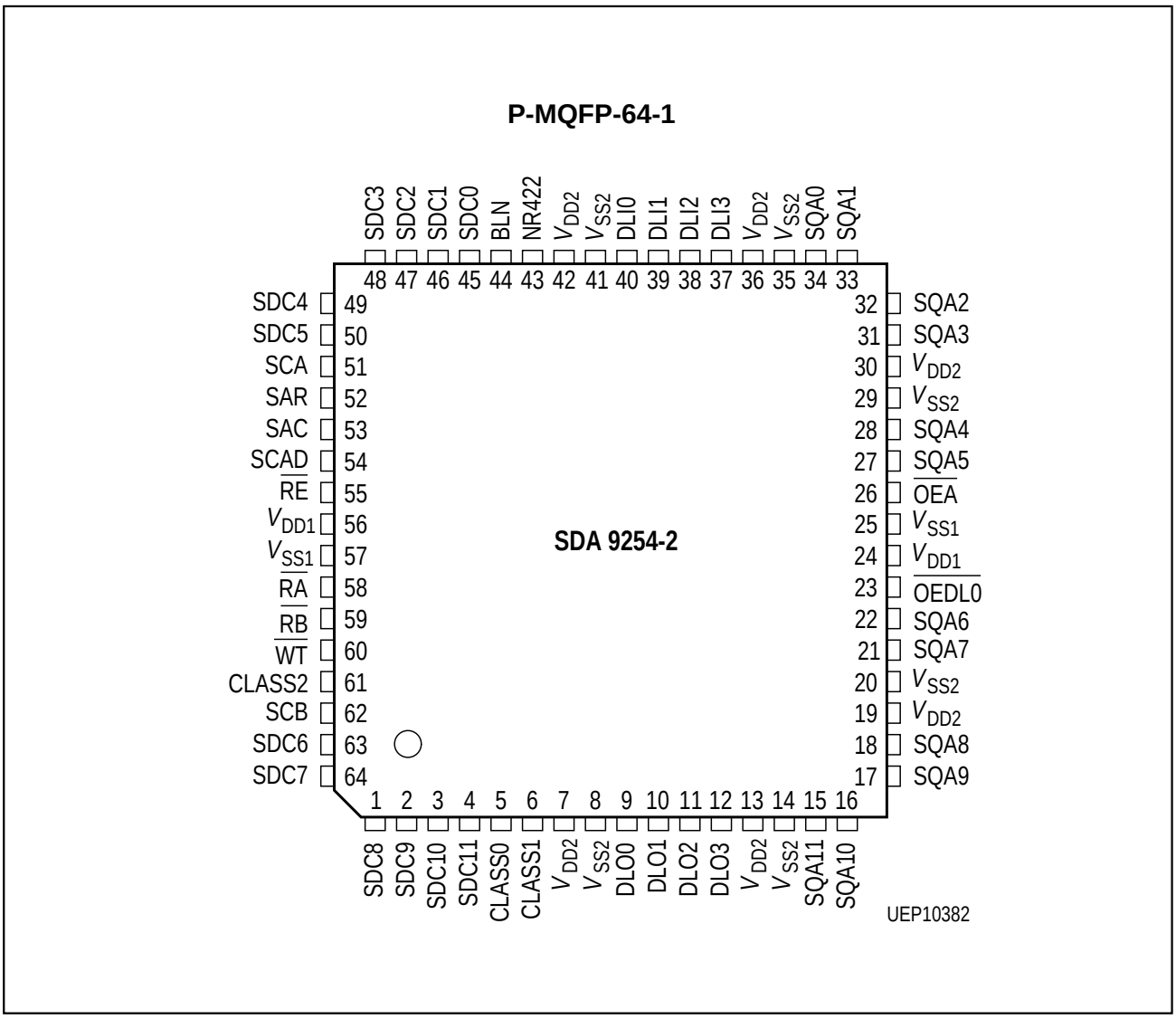


Figure 6

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
15 . . 18 21 22 27 28	SQA11 . . SQA8 SQA7 SQA6 SQA5 SQA4	O . . . . . . O	Serial data output port A (luminance signal)
31 32 33 34	SQA3 . . SQA0	O . . O	Serial data output port A (chrominance signal)
51	SCA	I	Serial clock input for port A
58	$\overline{RA}$	I	Read transfer control input (latch A to shift register A)
26	$\overline{OEA}$	I	Output enable input for port A
62	SCB	I	Serial clock input for port B and C
59	$\overline{RB}$	I	Read transfer control input (latch B to shift register B)
23	$\overline{OEDLO}$	I	Output enable input for delay line output
4 . . 1 64 63 50 49	SDC11 . . SDC8 SDC7 SDC6 SDC5 SDC4	I I	Serial data input port C (luminance signal)
48 47 46 45	SDC3 SDC2 SDC1 SDC0	I I I I	Serial data input port C (chrominance signal)
60	$\overline{WT}$	I	Write transfer control input (shift register C to latch C)
52	SAR	I	Serial row address input
53	SAC	I	Serial column address and mode control input
54	SCAD	I	Serial address clock input
55	$\overline{RE}$	I	RAM-enable input (also latches the addresses)
5 6	CLASS0 CLASS1	I I	Characteristic of the noise reduction filter

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
61	CLASS2	I	(medium or strong)
12 11 10 9	DLO3 DLO2 DLO1 DLO0	O O O O	Delay line output (for 4:2:2-mode)
37 38 39 40	DLI3 DLI2 DLI1 DLI0	I I I I	Delay line input (for 4:2:2-mode)
43	NR422	I	Noise reduction 4:2:2
44	BLN	I	Horizontal blanking input
7, 13, 19, 30, 36, 42	V_{DD2}		Data output power supply (+ 5 V)
8, 14, 20, 29, 35, 41	V_{SS2}		Data output power supply (GND)
24, 56	V_{DD1}		Memory power supply (+ 5 V), must be connected to V_{DD2}
25, 57	V_{SS1}		Memory power supply (GND), must be connected to V_{SS2}

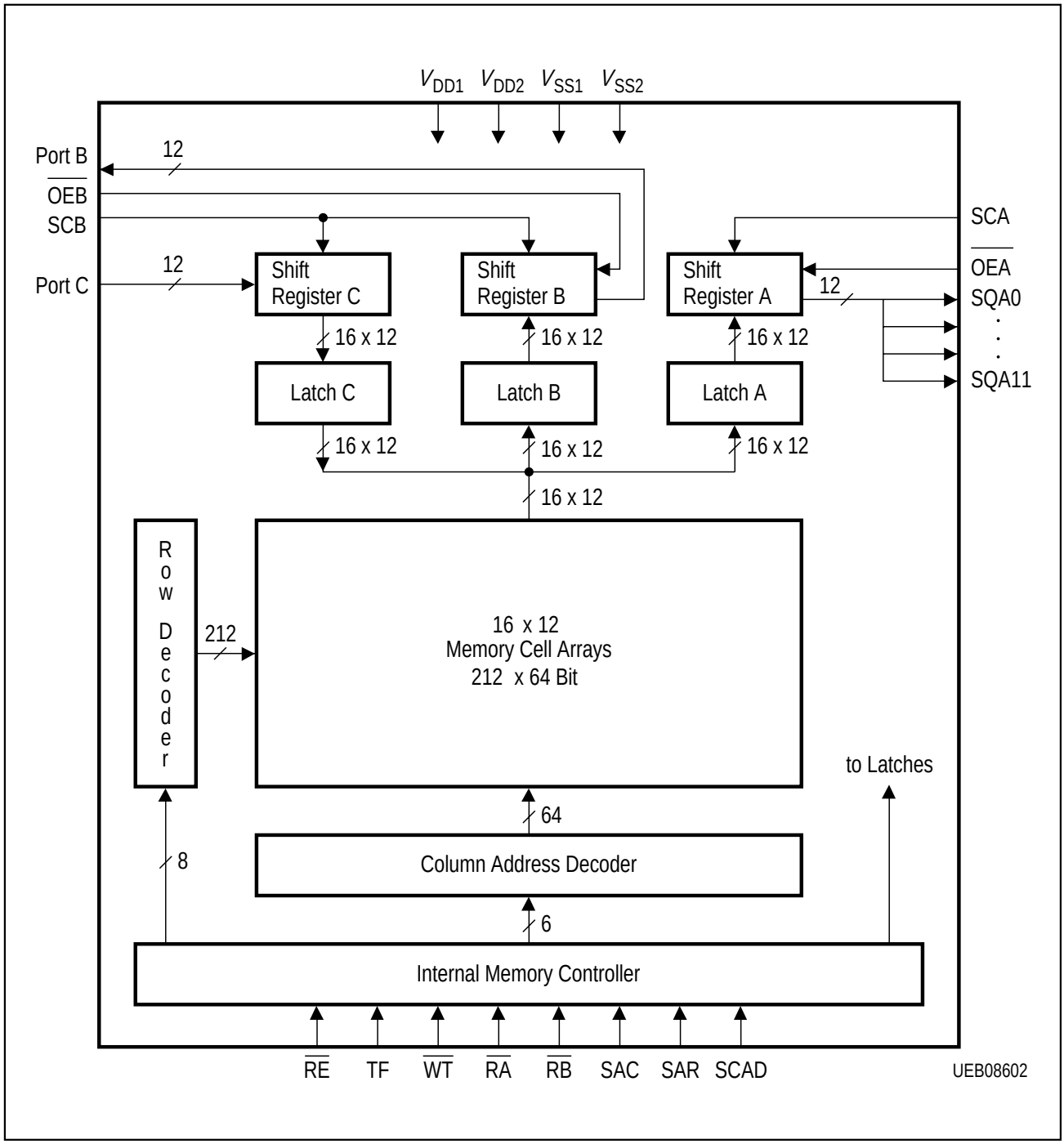


Figure 7
Block Diagram of the Memory

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Storage temperature	T_{stg}	– 55	125	°C	
Soldering temperature	T_{sold}		260	°C	
Soldering time	t_{sold}		10	s	
Input/output voltage	$V_{I/Q}$	– 1	7	V	
Power supply voltage	V_{DD}	– 1	7	V	
Data out current (short circuit)	I_Q		10	mA	
Total power dissipation	P_{tot}		1.2	W	
Power dissipation per output	P_Q		60	mW	

Operating Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD1}	4.5	5.0	5.5	V
Supply voltage	V_{DD2}	4.5	5.0	5.5	V
Supply voltage	V_{SS1}		0		V
Supply voltage	V_{SS2}		0		V
H-input voltage (except CLASS2)	V_{IH}	2.0		6.5	V
L-input voltage (except CLASS2)	V_{IL}	– 1.0		0.8	V
H-input voltage (CLASS2)	V_{IHC}	V_{DD} – 0.5		5.5	V
L-input voltage (CLASS2)	V_{ILC}	– 1.0		V_{SS} + 0.5	V
Ambient temperature	T_A	0	25	70	°C

DC Characteristics

V_{DD} = 5 V ± 10 %; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
H-output voltage	V_{QH}	2.4			V	I_{OUT} = – 2.5 mA
L-output voltage	V_{QL}			0.4	V	I_{OUT} = 2.1 mA
Input leakage current	$I_{I\,(L)}$	– 10		10	µA	0 V ≤ V_I ≤ 6.5 V
Output leakage current	$I_{Q\,(L)}$	– 10		10	µA	$\overline{OEA}$ = $\overline{OEDLO}$ = V_{IH}
Average supply current	I_{CCa}			200	mA	(t_{SC} port A = t_{SC} min) (t_{SC} port B = 2 t_{SC} min) (t_{SC} port C = 2 t_{SC} min) (t_{RC} = t_{RC} min) I_{CCa} depends on cycle rate and on output loading. Specified values are measured with open output.
Standby supply current	I_{CCb}			5	mA	($\overline{RE}$ = $\overline{OEA}$ = $\overline{OEDLO}$ = V_{DD1}) t_{SC} (SCA, SCB, SCAD) = max. (t_{SC})

AC Characteristics

V_{DD} = 5 V ± 10 %; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Memory read or write cycle time	t_{RC}	240		100000	ns	Operation with $t_{RC} \geq t_{RCmin}$ ensures that 8-bit serial data are shifted out within one $\overline{RE}$ cycle taking $t_{SC} = t_{SCmin}$. **See diagram 2, 3, 4, 6**
$\overline{RE}$ low time	t_{RE}	100		100000	ns	**See diagram 2, 3, 4, 6**
Serial port cycle time	t_{SC}	30		100000	ns	**See diagram 2 – 6**
$\overline{RE}$ precharge time	t_{RP}	100			ns	**See diagram 2, 3, 4, 6**
Address setup time	t_{AS}	5			ns	**See diagram 2, 3, 4, 6**
Address hold time	t_{AH}	6			ns	**See diagram 2, 3, 4, 6**
SCAD to $\overline{RE}$ set-up time	t_{ROS}	3			ns	**See diagram 2, 3, 4, 6**
$\overline{RE}$ to SCAD hold time	t_{ROH}	10			ns	**See diagram 2, 3, 4, 6**
$\overline{RE}$ to $\overline{RA}$ or $\overline{RB}$ delay time	t_{RRD}	90			ns	t_{RRD} and t_{RRL} are restrictive operating parameters only in memory read transfer cycles. **See diagram 2, 3**
$\overline{RA}$ or $\overline{RB}$ to $\overline{RE}$ lead time	t_{RRL}	– 30			ns	See $\overline{RE}$ to $\overline{RA}$ or $\overline{RB}$ delay time. **See diagram 2, 3**
$\overline{RA}$ to SCA $\overline{RB}$ to SCB set-up time	t_{RSS}	0			ns	**See diagram 2, 3**
$\overline{RA}$ or $\overline{RB}$ pulse width	t_{RPW}	10			ns	**See diagram 2, 3**
$\overline{RA}$ to SCA $\overline{RB}$ to SCB hold time	t_{RSH}	15			ns	**See diagram 2, 3**

AC Characteristics (cont'd)

V_{DD} = 5 V ± 10 %; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
$\overline{WT}$ to $\overline{RE}$ lead time	t_{WRL}	30			ns	t_{WRL} and t_{RWL} are restrictive operating parameters only in memory write transfer cycles. In that case t_{WRL} applies if the write transfer from shifter C to latch C occurs before the rising edge of $\overline{RE}$. Otherwise t_{RWL} has to be satisfied. **See diagram 4**
$\overline{RE}$ to $\overline{WT}$ lead time	t_{RWL}	50			ns	See $\overline{WT}$ to $\overline{RE}$ lead time
Output buffer turn-off delay	t_{OFF}	0		20	ns	t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltages levels.
$\overline{WT}$ to SCB delay time	t_{WTD}	0			ns	**See diagram 4**
$\overline{WT}$ to SCB lead time	t_{WTL}	15			ns	**See diagram 4**
$\overline{WT}$ pulse width	t_{WTP}	10			ns	**See diagram 4**
$\overline{OEA}$ to output A access time	t_{OAA}			25	ns	**See diagram 2, 5**
Access time from SCA	t_{CAA}			25	ns	**See diagram 2**
Access time from SCB	t_{CBA}			25	ns	**See diagram 3, 7**
Data input set-up time to SCB	t_{DS}	5			ns	**See diagram 5, 7**
Data input hold time to SCB	t_{DH}	6			ns	**See diagram 5, 7**
$\overline{OEDLO}$ to output DLO access time	t_{ODA}			25	ns	**See diagram 7**

AC Characteristics (cont'd)

V_{DD} = 5 V ± 10 %; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Refresh period	t_{REF}			16	ms	Either 256 refresh cycles or read/write cycles on 212 consecutive row addresses have to be performed within the 16 ms interval to maintain data
Transition time (rise/fall)	t_T	2		10	ns	Transition times are measured between V_{IH} and V_{IL}. **See diagram 1**
L-serial clock time	t_{SCL}	10			ns	**See diagram 2**
H-serial clock time	t_{SCH}	10			ns	**See diagram 2**
Hold time from SCA	t_{CAH}	6			ns	**See diagram 2**
Hold time from SCB	t_{CBH}	6			ns	**See diagram 3, 7**
Input capacitance (SCA, SCB)	C_{I1}			7	pF	f = 1 MHz
Input capacitance (all other pins)	C_{I2}			5	pF	f = 1 MHz
Output capacitance (SQA 0-11, DLO 0 ... 3)	C_Q			7	pF	f = 1 MHz

Operation Truth Table

$\overline{RE}$ Cycle N					$\overline{RE}$ Cycle N + n, n = 1, 2, 3 ...							
SCAD	SAR	SAC	Mode		$\overline{OEA}$	$\overline{OEDLO}$	SCA	SCB	$\overline{RA}$	$\overline{RB}$	$\overline{WT}$	Operation
			M0	M1								
⎍	RA0...RA7	CA0...CA5	L	L	X	X	X	X	⎎	X	X	Read transfer from memory to shifter A
⎍	RA0...RA7	CA0...CA5	H	L	X	X	X	X	X	⎎	X	Read transfer from memory to shifter B
⎍	RA0...RA7	CA0...CA5	L	H	X	X	X	X	X	X	⎎	Write transfer from shifter C to memory
⎍	X	X	H	H	X	X	X	X	X	X	X	Refresh with internal row address
X	X	X	X	X	L	X	⎍	X	X	X	X	Serial read port A
X	X	X	X	X	X	L	X	⎍	X	X	X	Data output DLO
X	X	X	X	X	X	X	X	⎍	X	X	X	Serial read port C

Note: X = Don't care

Row address, column address and mode bits have to be defined in $\overline{RE}$ cycle N in order to become effective in $\overline{RE}$ cycle N + 1

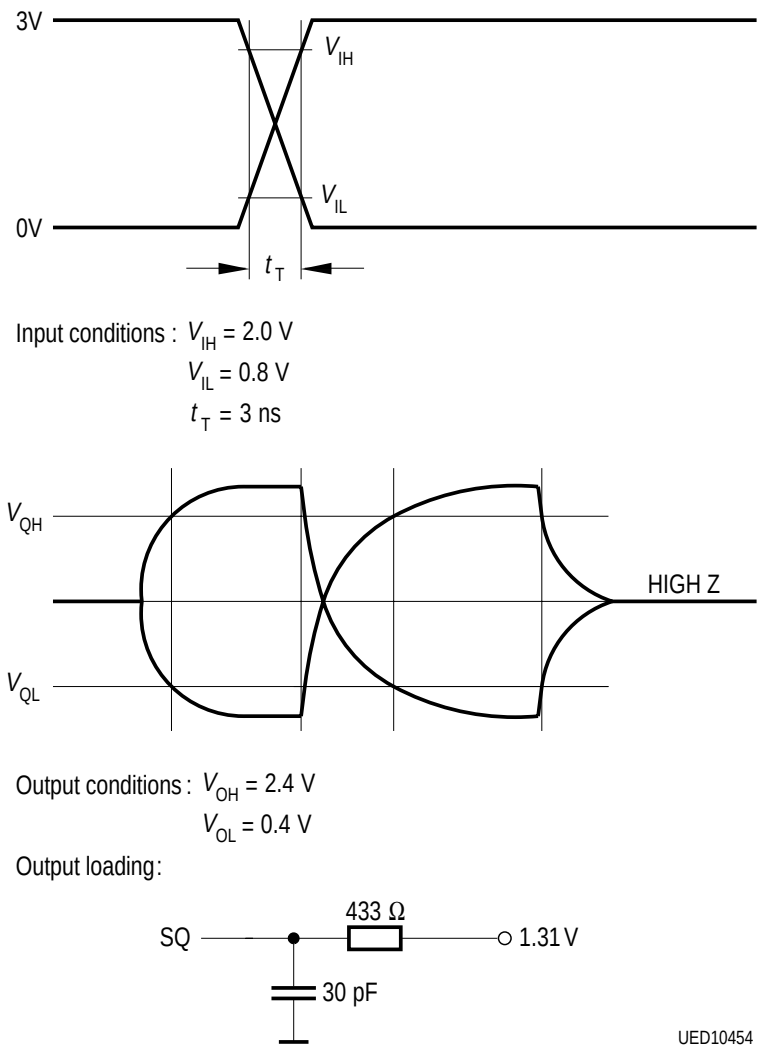


Diagram 1
AC-Timing Measuring Conditions

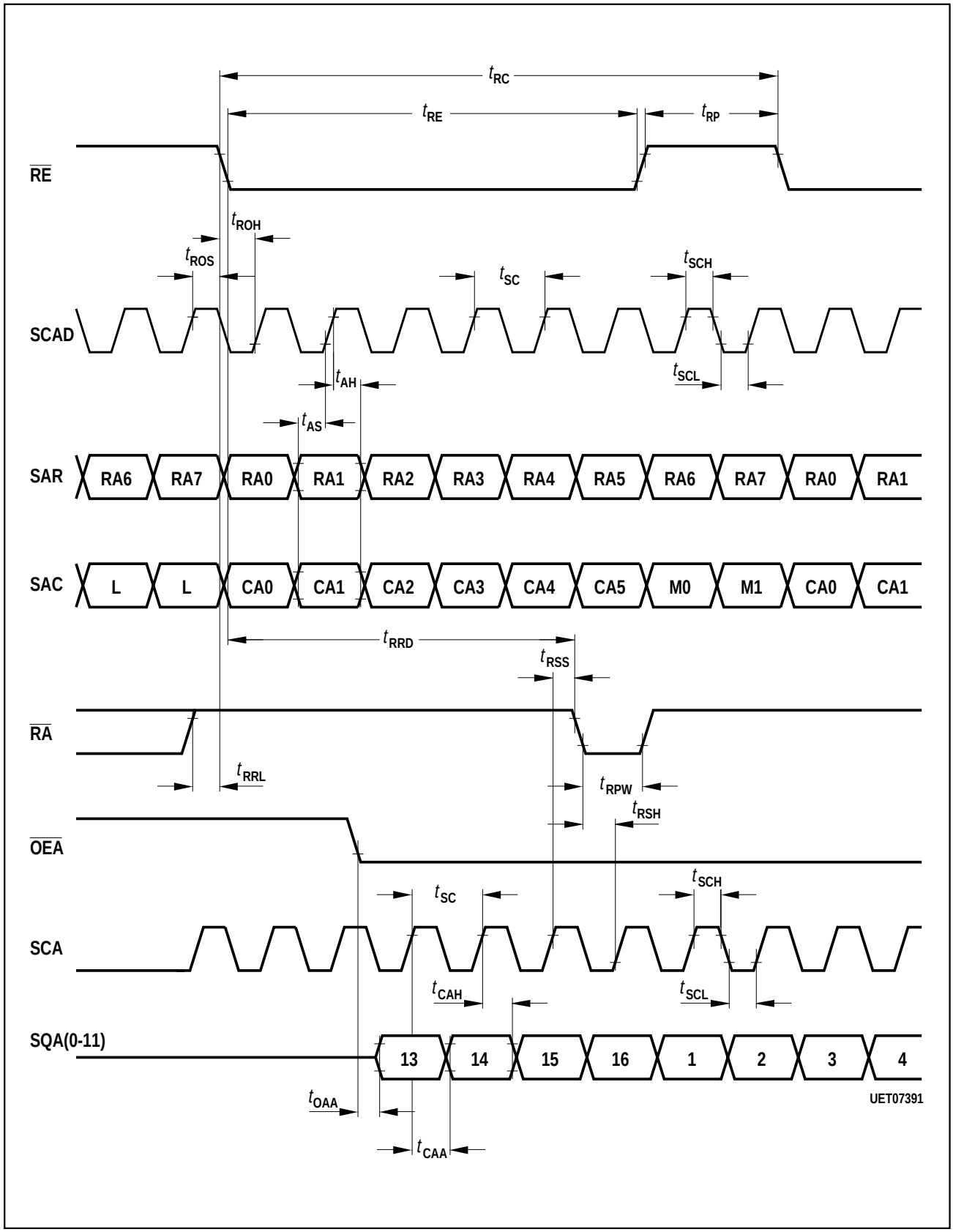


Diagram 2
Read Transfer Memory to Port A

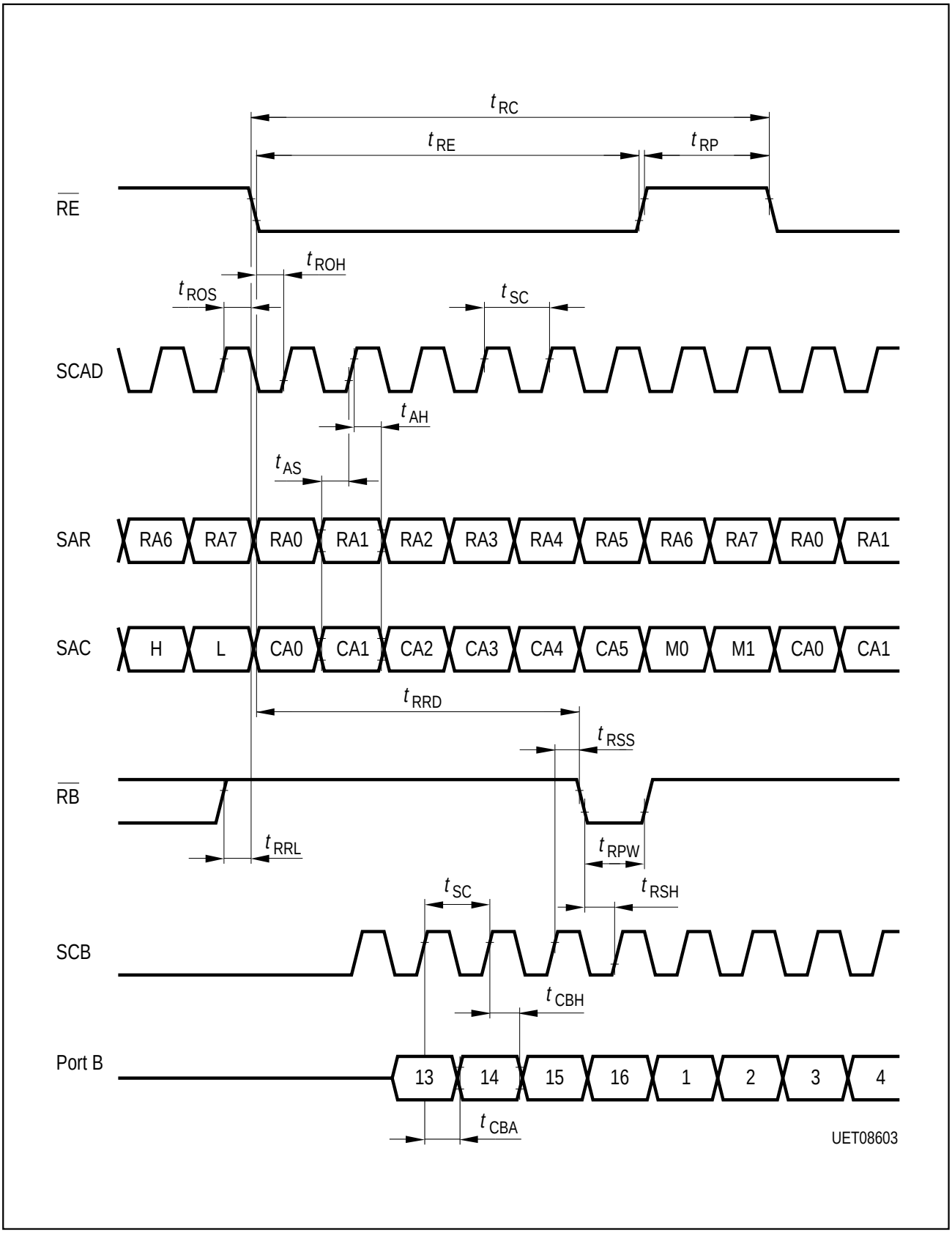


Diagram 3
Read Transfer Memory to Port B

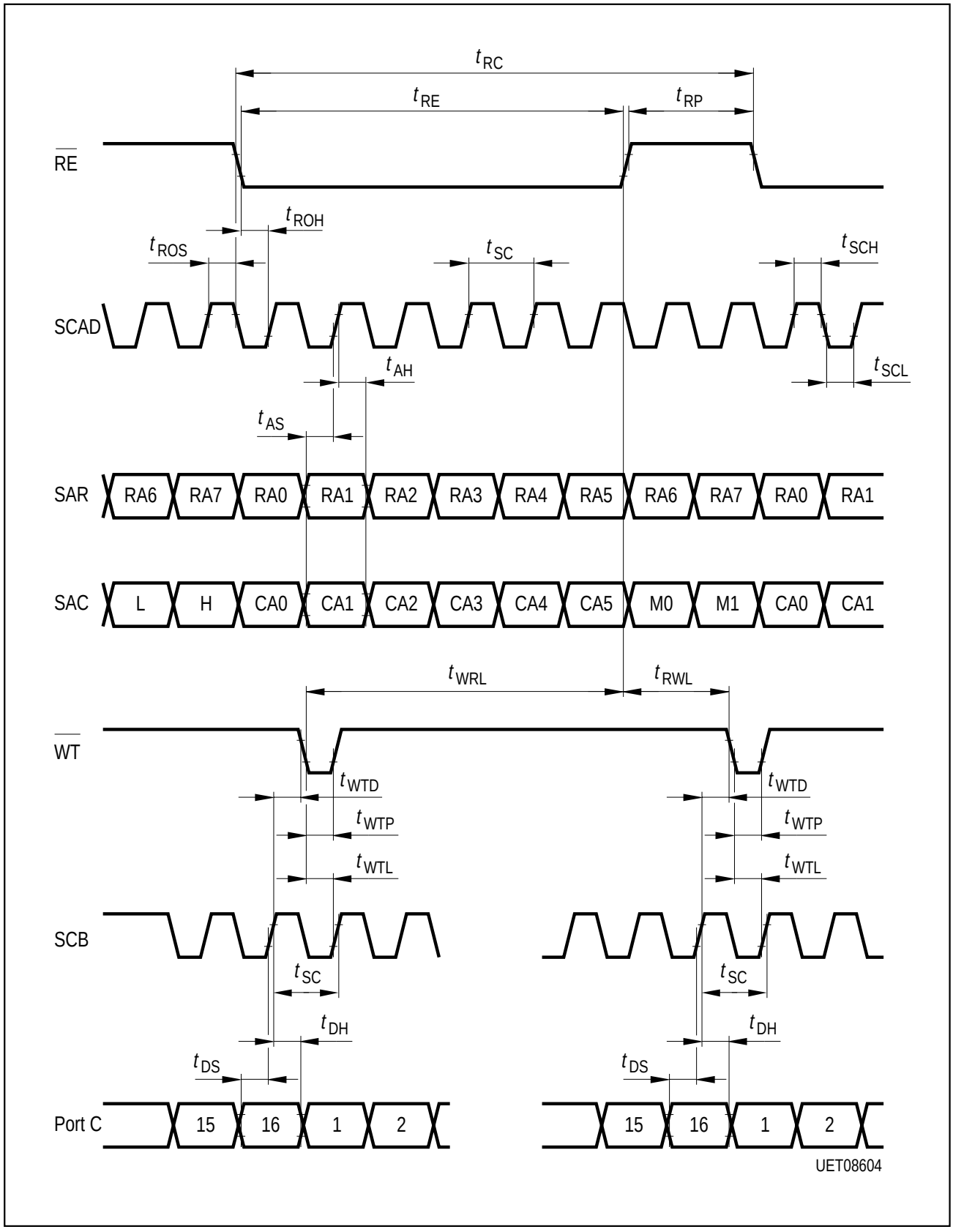


Diagram 4
Write Transfer from Port C to Memory

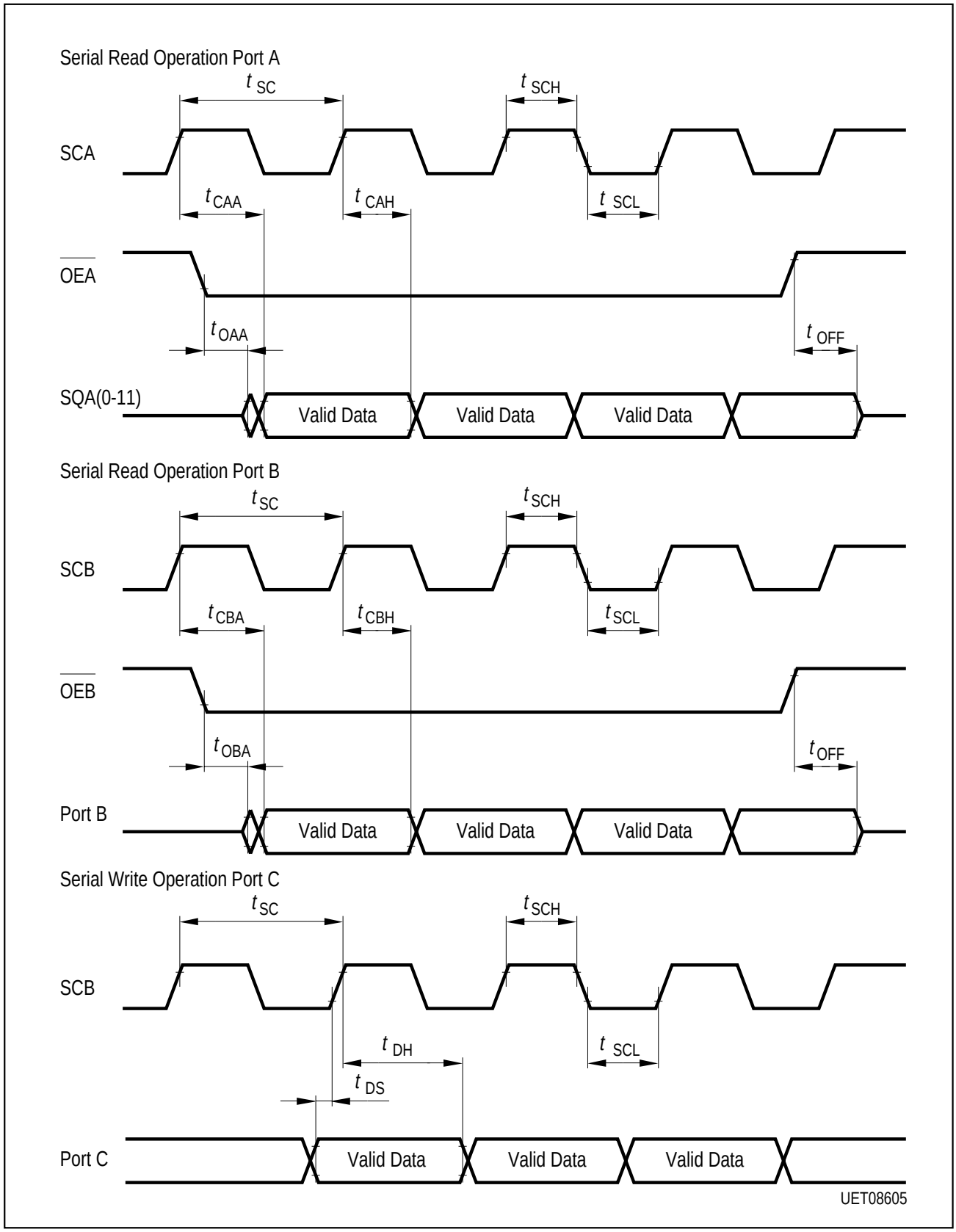


Diagram 5
Serial Read and Write Operations

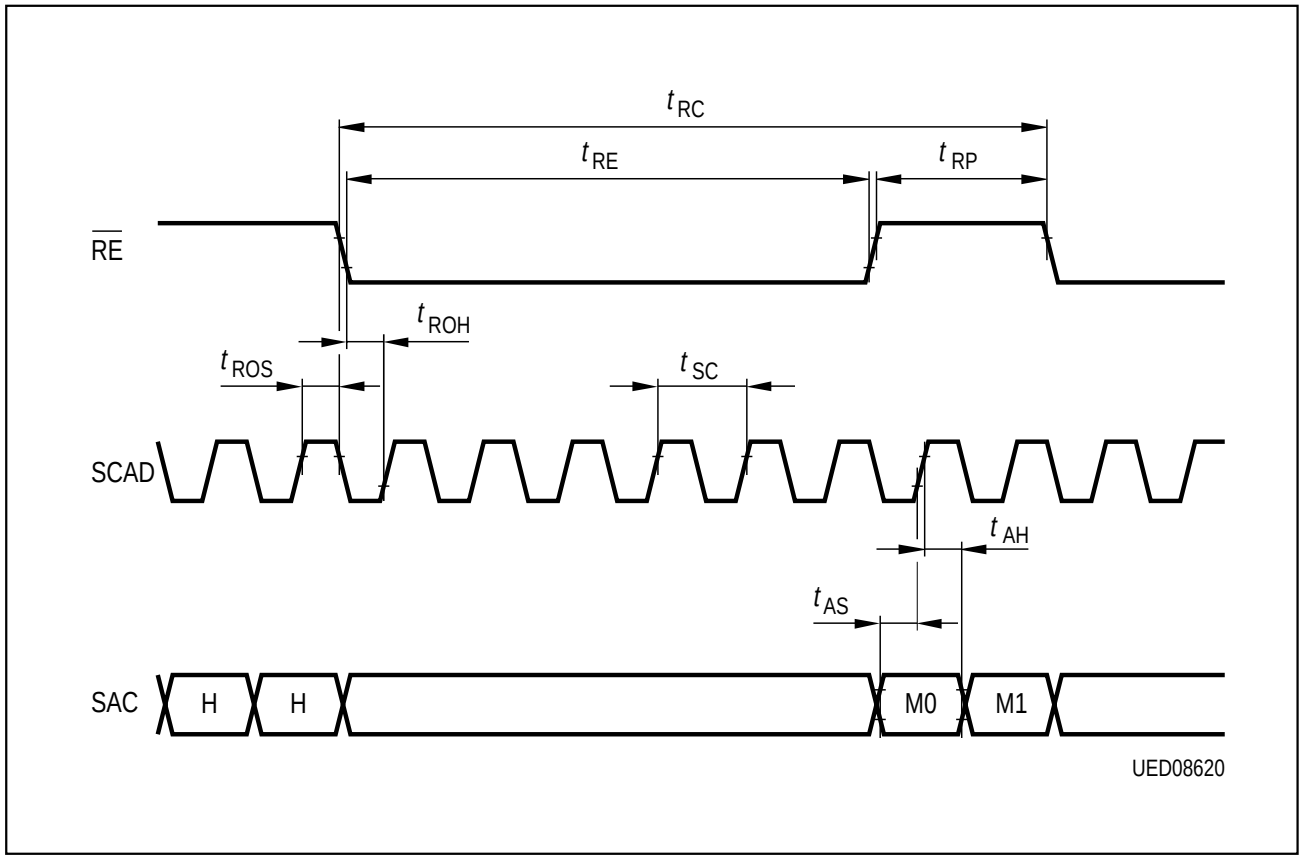
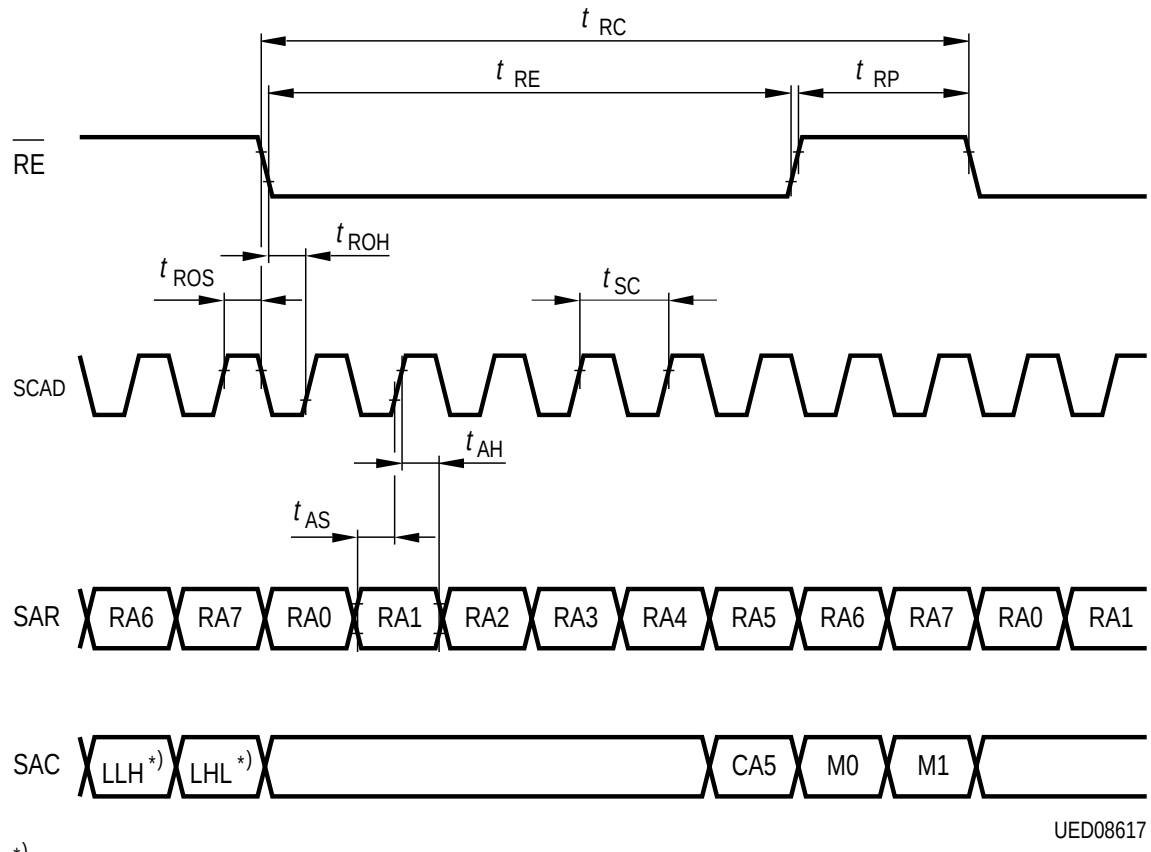


Diagram 6a
Refresh with Internal Row Address



*) Mode bits arbitrary, except combination M0 = "H" and M1 = "H"

*) Mode bits should toggle in successive cycles

Diagram 6b
Refresh with External Row Address

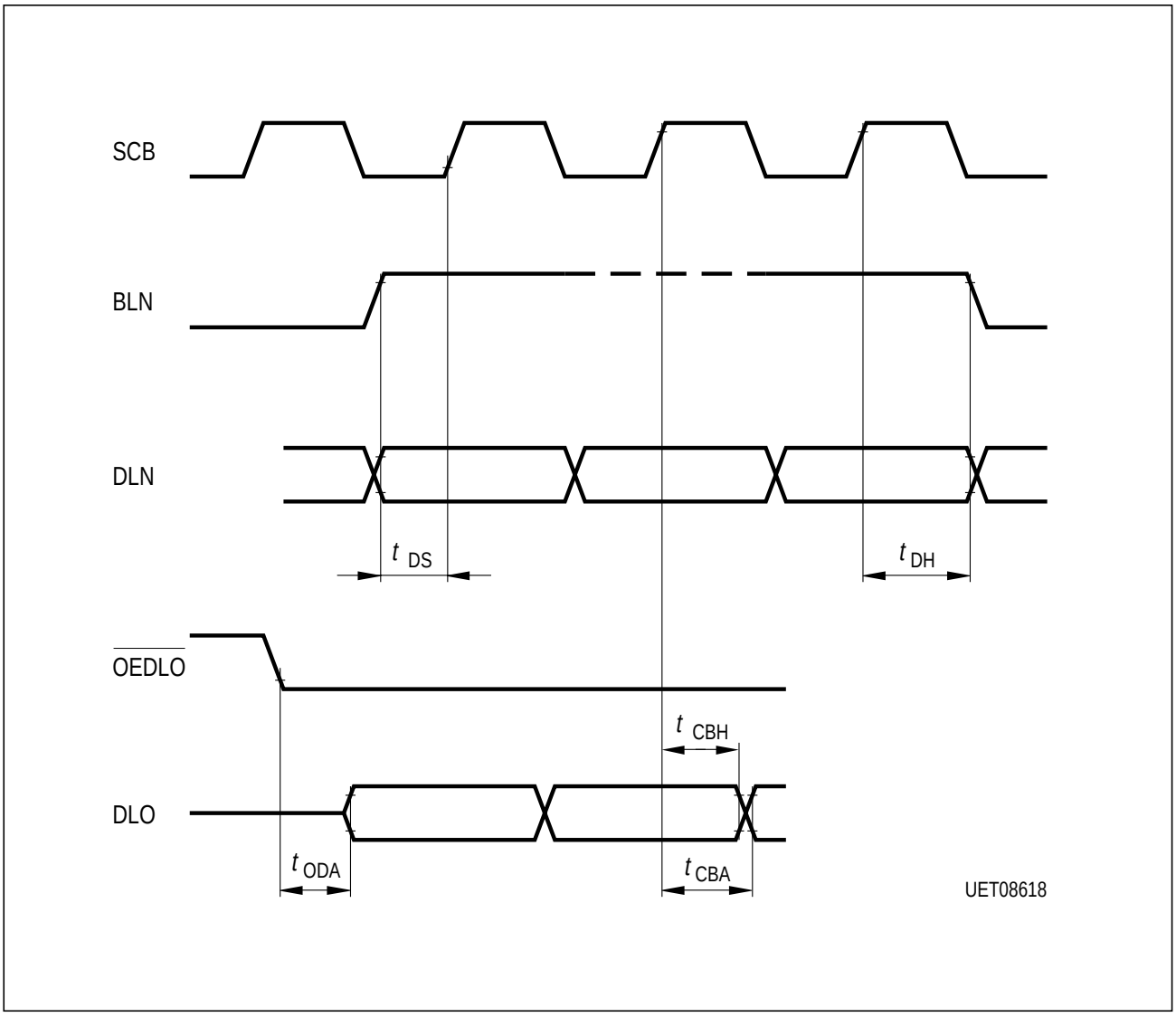


Diagram 7
Timing of BLN, DLI and DLO

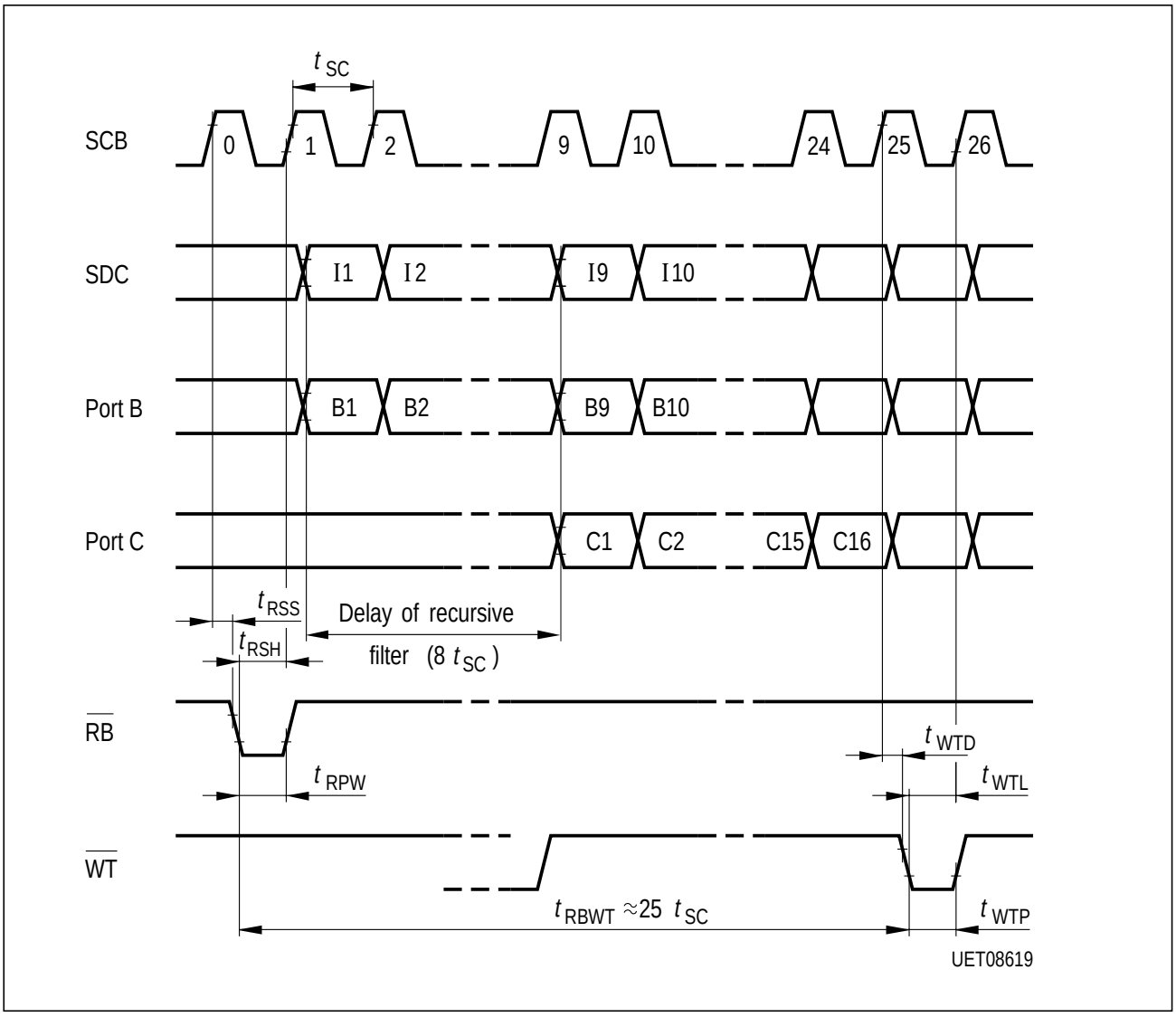


Diagram 8
$\overline{RB}$, $\overline{WT}$ Timing Restrictions

Application Circuit

For best performance and operation within the specified AC parameter limits it is mandatory to use separate decoupling capacitors for V_{SS1}/V_{DD1} and V_{SS2}/V_{DD2} with V_{SS1} shorted to V_{SS2} and V_{DD1} shorted to V_{DD2} on the board as shown in figure below.

Decoupling capacitors C_1 and C_2 of low inductance multilayer type (at least 0.1 µF) should be used. To avoid malfunction or even permanent damage of the device it is strongly recommended not to use any other supply configuration.

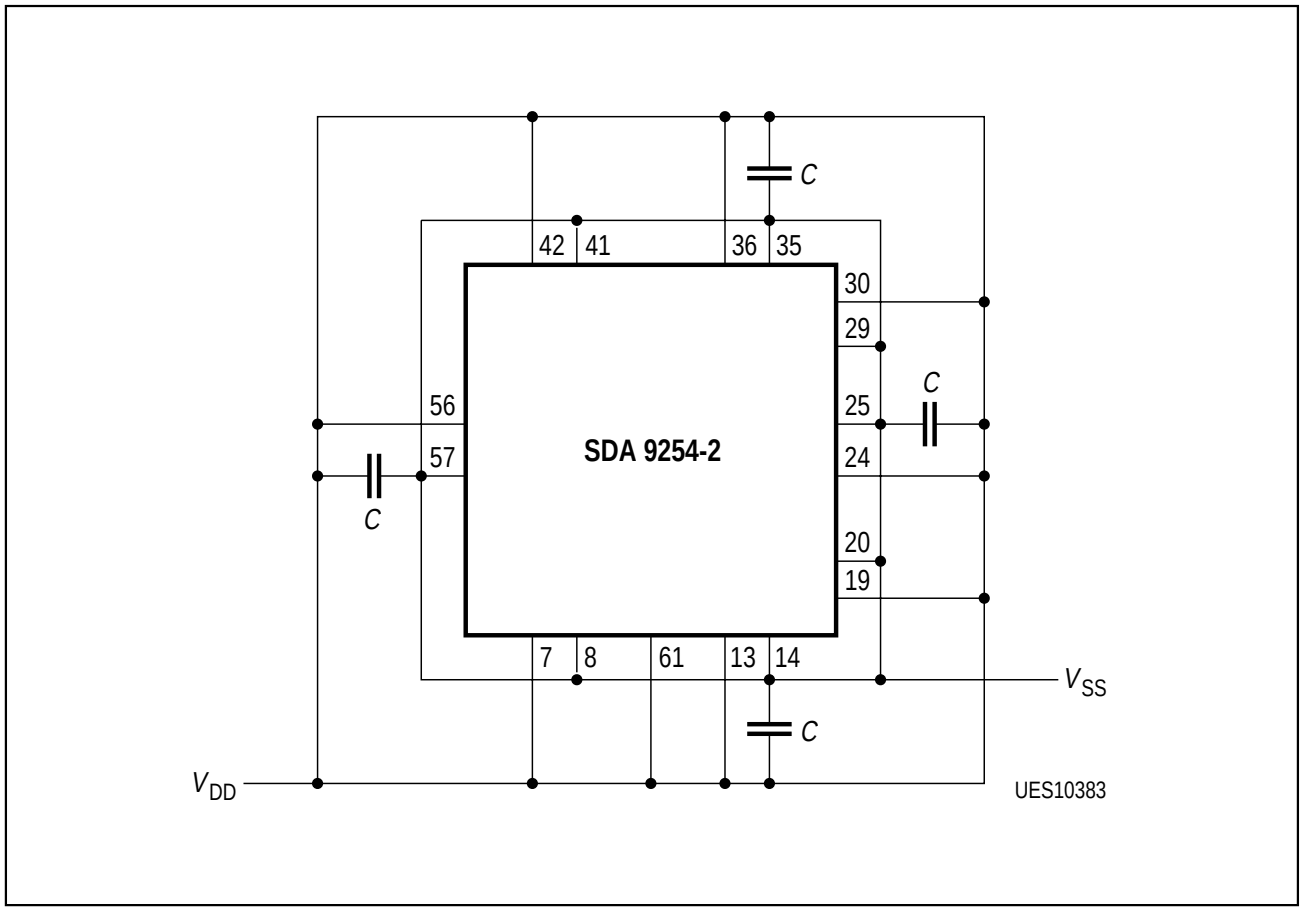


Figure 8

Application Information

Digital Storage of a TV Field

As standard for digital TV systems, CCIR recommendation 601 defines a field of 288 lines with 720 pixels per line. The sampling frequency is 13.5 MHz with a resolution of 8 bit per pixel.

Information is stored in 3 different channels: one channel for luminance (Y), two channels for chrominance (U and V).

The bandwidth ratio between the different channels is either Y:U:V = 4:1:1 or 4:2:2 depending on the coding method.

The bus width for the 4:1:1 format is 12 bit, the 4:2:2 format requires 16 bit and a SDA 9251-2X memory device additionally.

The SDA 9254-2 is designed for low cost large area flicker- and noise reduction systems. The following block diagram shows a typical application for 4:1:1 signals.

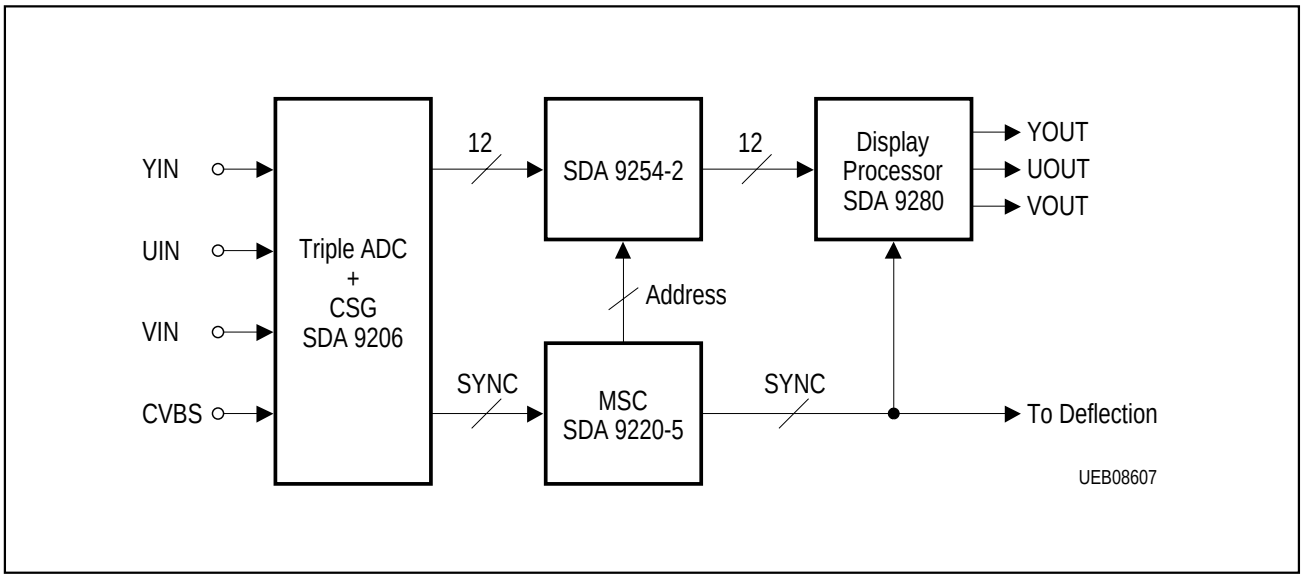
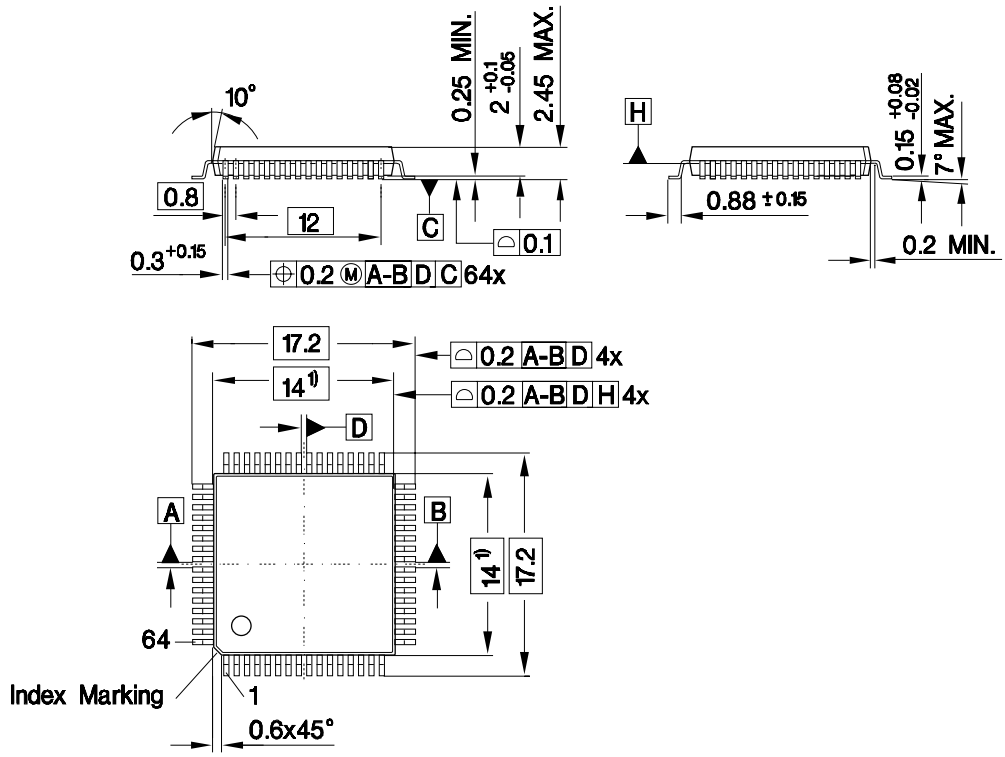


Figure 9
Low Cost Flicker- and Noise Reduction System with SDA 9254-2

Package Outlines

P-MQFP-64-1
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm