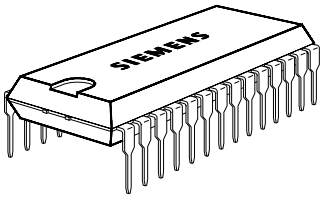
SIEMENS

Clock Sync Generator SDA 9257

Preliminary Data **MOS IC**

Features



P-DIP-28-1

- All settings made by I^2C Bus
- PLL lock-in behavior can be set to TV- or VCR mode
- Automatic clamping of CVBS input
- Provides all horizontal and vertical sync signals and clocks for operating PAMUX, analog color decoders, the A/D converters, PSND and Featurebox
- Free-running capability
- Frequency generator function possible with digitally adjustable frequency
- Lock-in function of the PLL on CVBS also possible with externally supplied 24-MHz or 27-MHz clock
- Multi-standard operation (50 Hz, 60 Hz; PAL, NTSC, SECAM)
- Vertical noise suppression and 50/60-Hz detection
- Serial digital output for actual frequency value and CVBS-black level

Applications

- Memory based image improvement with analog color decoder
- Memory based image improvement with digital multi-standard decoder
- Free-running sync generator
- Digital frequency synthesizer

Type	Ordering Code	Package
SDA 9257	Q67100-H5038	P-DIP-28-1

Functional Description

The clock sync generator consists essentially of the following function blocks (**refer to block diagram**):

- Analog clamping
- 7-bit, 27-MHz A/D converter
- Sync processor with digital horizontal PLL, vertical sync processor and pulse generator
- Clock generator with discrete timing oscillator, D/A converter, analog PLL and divider, as well as a crystal oscillator
- I^2C Bus interface
- Button flutter elimination

Circuit Description

1 Horizontal PLL (HPLL)

The CVBS is clamped before A/D conversion such that the H-sync pulse level is applied to the analog ground. Conversion takes place with 7 bits and a nominal frequency of 27 MHz. The digital HPLL filters the signal with a cutoff frequency of 1 MHz for a decimated clock frequency of 13.5 MHz, then measures the black level, calculates the sync threshold and determines the phase difference between the horizontal pulse and its own phase position. By means of digital PI filtering an increment is gained from this for the **D**iscrete **T**iming **O**scillator (DTO). The PI filter can be set by the bus so that the lock-in behavior of the PLL is optimal in relation to either the TV or VCR mode.

The DTO generates a saw-tooth with a frequency that is proportional to the increment, i.e. one quarter of the clock frequency on pin CLK1 (nominally 27 MHz). The saw-tooth is converted into a sinusoidal clock signal by means of sin ROMs and D/A converters and applied to an analog PLL which quadruples the frequency and minimizes residual jitter. In this manner a clock is provided that is line-locked with the CVBS-input signal. The ratio of this clock frequency to the horizontal frequency of CVBS can be set to the values 1728, 1716 or 1536 by the I^2C Bus.

The digital horizontal PLL supplies a further composite sync signal derived directly from the CVBS, a noise-suppressed horizontal pulse and a non-suppressed vertical pulse obtained by digital integration of the main equalizing pulses. An integration time of 26.6 µs or 11.3 µs can be set by the I^2C Bus. The HPLL is driven in the “external clock mode” by the 24-MHz clock supplied by pin CKE and locks onto CVBS by continually locking the relationship between the input clock and the horizontal frequency of CVBS (768 $\pm$ 32).

The HPLL can lock onto a composite sync signal using **application circuit 5.** The edges on pin CVBS should not be steeper than 100 ns.

2 Vertical Sync Processing

Vertical sync processing consists of:

- 625/525 line detection
- Vertical noise suppression

The 625/525 line detector measures the range of lines within a field into which the vertical pulses will fall that were obtained from the CVBS signal by integration. By taking the average of the individual measurements with two up/down counters, the status bits “FF” and “FFGF” (**refer to timing diagram 8** and I^2C Bus) are obtained.

When vertical noise suppression is switched on (V_{OFF} = 0), the vertical pulse obtained from the CVBS signal by integration is admitted only within a preset window (**refer to timing diagram 8**) and appears as a VS pulse. The width of the window can be set with the I^2C Bus bit VWW.

In the temporary absence of vertical pulses in CVBS, a continuous VS can be generated by switching on a “flywheel mode” (SCHW = 1) provided that the number of lines per field in CVBS is 312.5 or 262.5 respectively.

When interference to CVBS is heavy, missing vertical pulses can be supplemented by switching on the flywheel mode and vertical interference pulses can be eliminated by switching on the noise suppression circuitry. Noise suppression and the flywheel mode can be enabled independently of each other.

There is also the possibility of generating VS in the free-running mode. The VS pulses are then completely independent of the vertical sync pulse in CVBS. When FREE = 1, a VS pulse is generated every 262.5 or 312.5 lines (VF = 1 or 0 respectively). Free-running generation of VS occurs every 262 or 312 lines in the terminal mode (TERM = 1).

The two fields can be identified by means of status bit HB. It toggles for every field but is set to 0 whenever the vertical pulse occurs within the first half of a line and within the noise-reduction window (start of the first field).

3 Pulse Generation

The clock sync generator supplies the following pulses:

- HS
- VS
- BLN
- Two clamping pulses (H1 and H2)
- Either a sandcastle (SC) or a super sandcastle (SSC) pulse or a composite sync (CS)
- The HS pulse is 32 CLK1 clock periods long and can be shifted by the I^2C Bus in increments of 8 CLK1 clock periods each (**see timing diagram 1**).
- For the VS pulse refer to vertical noise suppression
- With the BLN pulse the start time (high-to-low edge) and the stop time (low-to-high edge) can be set within a certain range of lines in increments of two CLK1 clock periods by the I^2C Bus. The timing of BLN does not change during the field blanking interval.
- The start time (low-to-high edge) and stop time can similarly be set in increments of two CLK1 clock periods for pulses H1 and H2.
- The composite sync signal is derived from the CVBS, after it has passed through a low-pass filter, by means of the sync threshold in the HPLL and is also provided with circuitry to suppress noise which might occur due to very noisy CVBS (**refer to timing diagrams 4 and 5, and diagram 1**).
- An external transistor stage is required to generate sandcastle or super sandcastle pulses and inserts the missing burst key in the pulse on the SC pin, which has only a zero, vertical- and horizontal-blanking level. For this purpose the inverse burst-key signal is available at pin SINC for triggering the transistor base (**refer to application circuit 6**).
  The start time of the horizontal blanking level may be defined in increments of two CLK1 clock periods over a wide range of lines by the I^2C Bus.

4 Miscellaneous Circuit Sections

- To suppress bottom flutter in VCR mode, the frequency of the clock can be “hold” by “freezing” the increment of the HPLL. The vertical-frequency “freezing-time” starts a number of lines (programmable by the I²C Bus) before the vertical pulse and then lasts for a number (programmable) of lines (**refer to timing diagram 2**). The settings do not depend on I²C-bit VCRTV.
- The increment of the HPLL, the black level and the status bits are output serially on the SINC pin (optionally to the sandcastle pulse) and are therefore available for a digital color decoder, for instance. Because the frame of these line-frequency output begins with a start bit (low) it can be detected independently of the phase of HPLL (**refer also to timing diagram 3**).
- An active low reset is available for other chips at pin RES. It is reset when the chip supply V_{DD} is switched on or when voltage glitches occur in it. It is not cancelled until the crystal oscillator resonates and the two device supplies V_{DD} and V_{DDA} are applied. The minimum length of time is 1 ms.

5 External Clock Mode of the HPPL

The HPPL locks onto the CVBS signal for the following operating ranges when the chip is operated with a clock frequency supplied on pin CKE (SCLE bit at 1):

Control Bit		Clock Frequency Range on CKE
HPPL 1	HPPL 0	
0	X	26.1 … 27.9 MHz
1	0	26.1 … 27.9 MHz
1	1	23.1 … 24.9 MHz

The jitter on output pulses HS, VS, BLN, H1 and H2 and output clocks CLK1 and CLK2 is several CLK1-clock periods long.

Detailed Circuit Description

Description of I²C Interface

Slave Address:

1	0	1	1	0	B	C

B: Equal to the value set on pin ADR1
C: Equal to the value set on pin ADR0

Receiver Format:

S	Slave Address	0	A	Sub Address	A	Data Byte	A	P

S: Start condition
A: Acknowledge
P: Stop condition

Synoptical Table of Data Byte Formats

Receiver Register	SUB-ADDR.	Data Bits (MSB)							(LSB)
Pin Control	00	OEFB	SCL2	SCLE	CLKDI	SSC1	SSC0	I1	SCHW
HPLL Control	01	HPLL1	HPLL0	RSTH	VTHRE	CLOF	VCRT	FRZIN	EXINC
V Process. - and	02	FREE	VOFF	VF	VWW	TERM	VCO2	VCO1	VCO0
VCO Control	03	INC07	INC06	INC05	INC04	INC03	INC02	INC01	INC00
External Clock-Frequency Control	04	INC15	INC14	INC13	INC12	INC11	INC10	INC09	INC08
BLN Start Time	05	BON8	BON7	BON6	BON5	BON4	BON3	BON2	BON1
BLN Stop Time	06	BOF8	BOF7	BOF6	BOF5	BOF4	BOF3	BOF2	BOF1
H1 Start Time	07	H10N8	H10N7	H10N6	H10N5	H10N4	H10N3	H10N2	H10N1
H1 Stop Time	08	H10F8	H10F7	H10F6	H10F5	H10F4	H10F3	H10F2	H10F1
H2 Start Time	09	H20N8	H20N7	H20N6	H20N5	H20N4	H20N3	H20N2	H20N1
H2 Stop Time	10	H20F8	H20F7	H20F6	H20F5	H20F4	H20F3	H20F2	H20F1
HS Start Time	11	HS0N8	HS0N7	HS0N6	HS0N5	HS0N4	HS0N3	HS0N2	HS0N1
SC Start Time	12	SC0N8	SC0N7	SC0N6	SC0N5	SC0N4	SC0N3	SC0N2	SC0N1
FRZINC TIME	13	FI0N4	FI0N3	FI0N2	FI0N1	FILE4	FILE3	FILE2	FILE1

(Automatic incrementing of the subaddress)
When operating voltage is applied (POR), all registers are set to 0.

Pin Control (subaddress 00)

Output Enable by Featurebox Signals	Control Bit OEFB
BLN, HS, VS outputs tristate	0
BLN, HS, VS outputs enabled	1

Selection of Clock Frequency on CLK2	Control Bit SCL2
13.5 MHz (nominal)	0
27 MHz (nominal)	1

Selection of Clock for Chip Operation	Control Bit SCLE
A line locked clock is generated by the internal PLL	0
Clock source is CLE. The radio between the horizontal frequency in CVBS and CLK1 depends on control bits HPLL0 and HPLL1*	

Clock Out Disable	Control Bit CLKDI
CKL1 and CKL2 tristate	1
CKL1 and CKL2 enabled	0

Selection of Function on SC and SINC			Control Bits	
SC-Pin Function		SINC-Pin Function	SSC1	SSC0
Tristate		Tristate	0	0
Super sandcastle	without burst key	Burst key inverted	0	1
Sandcastle			1	1
Composite sync		Serial increment and status bits	1	0

Level on I1	Control Bit I1
Low	0
High	1

Mode of Vertical Pulse Generation	Control Bit SCHW
No flywheel mode	0
Flywheel mode	1

* Pin CLE should most definitely be connected to ground in this instance in order to minimize output signal jitter

HPLL Control (subaddress 01)

Relationship between Horizontal Frequency in CVBS and Frequency on CKL1	Control Bits	
	HPLL1	HPLL0
1728	0	*)
1716	1	0
1536	1	1

Initiation of a Reset for HPLL	Control Bit RSTH
No function	0
HPLL is reset once, new lock-in process starts	1

Minimum Sync Pulse Length from which a Vertical Pulse is Detected	Control Bit VTHRE
26.6 µs	0
11.3 µs	1

CVBS Clamping ON/OFF	Control Bit CLOF
Clamping ON	0
Clamping OFF	1

Selection of HPLL Lock-In Behavior	Control Bit VCRTV
Optimum for VCR	0
Optimum for CVBS from network	1

Freezing of the Actual Value of Clock Frequency	Control Bit FRZINC
No function	0
Instantaneous increment is freezing so that the instantaneous frequency value is frozen and there is no lock-in function of HPLL	1

Selection of Increment for Determining Clock Frequency	Control Bit EXINC
Increment from HPLL	0
Increment corresponding to I^2C Bus bits INC00 … INC15 (frequency generator mode)	1

*) don't care

Vertical Processor and VCO Control (subaddress 02)

Generation of V Pulse	Control Bit FREE
V derived from CVBS	0
Free-running generation; vertical frequency is determined by VF bit, VOFF bit is enabled, SCHW bit should be set to 1	1

Vertical Noise Suppression	Control Bit VOFF
Noise suppression enabled	0
No noise suppression	1

Number of Lines per Field	Control Bit VF
312.5 or 312	0
262.5 or 262	1

Note: VF must be set to the number of lines present in CVBS for flywheel and noise suppression modes.

VF is determined by the number of lines per field for the free-running or terminal mode.

Width of Window in Vertical Processing	Control Bit VWW
Wide window in vertical noise suppression mode and for detection of status bits FF and FFGF	0
Narrow window **(refer also to timing diagrams 8 and 9)**	1

Number of Lines per Field Generated in Free-Running Mode	Control Bits				
	FREE	TERM	SCHW	VF	VOFF
312	×	1	×	0	×
262	×	1	×	1	×
312.5	1	0	1	0	×
262.5	1	0	1	1	×
344	1	0	0	0	×
288	1	0	0	1	×

x: don’t care

Center Frequency (of VCO)	Control Bits		
	VCO2	VCO1	VCO0
Approx. 22.4 MHz	0	1	1
Approx. 24.0 MHz	0	1	0
Approx. 25.6 MHz	0	0	1
Approx. 27.0 MHz	0	0	0
Approx. 29.0 MHz	1	1	1
Approx. 31.0 MHz	1	1	0
Approx. 33.0 MHz	1	0	1
Approx. 35.0 MHz	1	0	0

Note: The pull-in range of the VCO is ± 8 %, irrespective of the center frequency

External Clock Frequency Setting (subaddresses 03 and 04)

Clock Frequency on CLK1 (FQ = XTAL Frequency, [INC] = Digital Value of INC15 … INC00) EXINC bit must be set)	Control Bits (MSB) (binary offset) (LSB)			
	INC15	INC14	…	INC00
F = FQ × 4 • 65536/262144 = FQ	0	0	…	0
F = FQ × 4 • (65536 + [INC])/262144		⋮		
F = FQ × 4 • (65536 + 65535)/262144 = 2 x FQ	1	1	…	1

Note: When clock frequencies below 24 MHz or above 29 MHz are selected, the VCO should be set with control bits VCO2 … VCO0 as well. Clock jitter may rise when crystal clock FQ is changed.

All times quoted below refer to a nominal frequency of 27 MHz on CLK1

BLN Start Time (subaddress 05)

BLN Start Time in Relation to Reference Time (refer also to timing diagram 1)			**Control Bits ± (Two's Complement) (LSB)**					
Time	**Number in 13.5-MHz Clock Periods**		**BON8**	**BON7**	**BON6**	**…**	**BON2**	**BON1**
9.62 µs	+ 130	– (– 128) + 2*	1	0	0	…	0	0
⋮		⋮				⋮		
0.22 µs	+ 3	– (– 1) + 2*	1	1	1	…	1	1
0.15 µs	+ 2	– (0) + 2*	0	0	0	…	0	0
⋮		⋮				⋮		
– 9.25 µs	– 125	– (+ 127) + 2*	0	1	1	…	1	1

BLN Stop Time (subaddress 06)

BLN Stop Time in Relation to Reference Time			**Control Bits (One's Complement)**					
Time	**Number in 13.5-MHz Clock Periods**		**BOF8**	**BOF7**	**BOF6**	**…**	**BOF2**	**BOF1**
+ 0.22 µs	+ 3	0 + 3*	0	0	0	…	0	0
⋮	⋮					⋮		
+ 9.63 µs	+ 130	127 + 3*	0	1	1	…	1	1
+ 9.0 µs	+ 131	128 + 3*	1	0	0	…	0	0
	⋮					⋮		
+ 19.11 µs	+ 258	255 + 3*	1	1	1	…	1	1

* Due to internal delays

H1 Start Time (subaddress 07) and
H1 Stop Time (subaddress 08) (identical coding)

H1 Start and Stop Times in Relation to Reference Time			**Control Bits**					
Time	**Number in 13.5-MHz Clock Periods**		**H10N8 H10F8**	**H10N7 H10F7**	**H10N6 H10F6**	**… …**	**H10N2 H10F2**	**H10N1 H10F1**
+ 4.88 µs	+ 66	– (– 64) + 2*	1	1	0	…	0	0
⋮	⋮				⋮			
+ 0.222 µs	+ 3	– (– 1) + 2*	1	1	1	…	1	1
+ 0.148 µs	+ 2	– (+ 0) + 2*	0	0	0	…	0	0
⋮	⋮				⋮			
– 4.51 µs	– 61	– (+ 63) + 2	0	0	1	…	1	1
– 4.58 µs	– 62	– (+ 64) + 2*	0	1	0	…	0	0
⋮	⋮				⋮			
– 9.26 µs	– 125	– (+ 127) + 2*	0	1	1	…	1	1
– 9.33 µs	– 126	– (+ 128) + 2*	1	0	0	…	0	0
	⋮				⋮			
– 13.95 µs	– 189	– (+ 191) + 2*	1	0	1	…	1	1

* Due to internal delays

H2 Start Time (subaddress 09) and
H2 Stop Time (subaddress 10) (identical coding)

H2 Start and Stop Times in Relation to Reference Time			**Control Bits**					
Time	**Number in 13.5-MHz Clock Periods**		**H20N8 H20F8**	**H20N7 H20F7**	**H20N6 H20F6**	**… …**	**H20N2 H20F2**	**H20N1 H20F1**
+ 14.32 µs	+ 194	– (– 192) + 2*	0	1	0	…	0	0
⋮	⋮				⋮			
+ 9.70 µs	+ 131	– (– 129) + 2*	0	1	1	…	1	1
+ 9.63 µs	+ 130	– (– 128) + 2*	1	0	0	…	0	0
+ 9.56 µs	+ 129	– (– 127) + 2*	1	0	0	…	0	1
⋮	⋮				⋮			
+ 0.222 µs	+ 3	– (– 1) + 2*	1	1	1	…	1	1
+ 0.148 µs	+ 2	– (0) + 2*	0	0	0	…	0	0
+ 0.074 µs	+ 1	– (+ 1) + 2*	0	0	0	…	0	1
⋮	⋮				⋮			
– 4.51 µs	– 61	– (+ 63) + 2*	0	0	1	…	1	1

HS Start Time (subaddress 11)

HS Start Time in Relation to Reference Time			**Control Bits**				
Time	**Number in 13.5-MHz Clock Periods**		**HS0N8**	**HS0N7**	**HS0N6**	**....**	**HS0N1**
– 28.52 µs	+	– (– 96) + 2*	1	0	1	0 0 0 0	0
⋮	⋮			⋮			
+ 0.37 µs	+ 5	– (– 1) · 4 + 1*	1	1	1	1 1 1 1	1
+ 74 ns	+ 1	– (0) · 4 + 1*	0	0	0	0 0 0 0	0
– 222 ns	–	– (+ 1) · 4 + 1*	0	0	0	0 0 0 0	1
⋮	⋮			⋮			
– 34.89 µs	– 471	– (118) · 4 + 1*	0	0	1	1 0 1 1	0
– 35.18 µs	– 475	– (119) · 4 + 1*	0	0	1	1 0 1 1	1

* Due to internal delays

SC Start Time (subaddress 12)

Start Time of H Insertion in the SC or SSC Pulse			Control Bits (+) (Two's Complement) (LSB)					
Time	**Number in 13.5-MHz Clock Periods**		**SC0N8**	**SC0N7**	**SC0N6**	**…**	**SC0N2**	**SC0N1**
+ 9.55 µs	+ 129	(+ 128) + 1*	1	0	0	…	0	0
	⋮				⋮			
74 ns	+ 1		0	0	0	…	0	0
		– (0) + 1*						
	⋮				⋮			
– 9.33 µs	– 126	– (+ 127) + 1*	0	1	1	…	1	1

Freezing of Actual Clock Frequency in Number of Lines Near the Vertical Pulse (subaddress 13)

Start of Clock Frequency in Number of Lines before the Vertical Pulse	Control Bits			
	FION4	**FION3**	**FION2**	**FION1**
0 (no freezing)	0	0	0	0
1	0	0	0	1
.				
.		⋮		
.				
15	1	1	1	1

Duration of Clock Frequency Freezing in Number of Lines	Control Bits			
	FILE4	**FILE3**	**FILE2**	**FILE1**
0 (no freezing)	0	0	0	0
.				
.		⋮		
.				
15	1	1	1	1

* Due to the internal delays

Transmitter Format:

S	Slave Address	1	A	Status Byte	A	P

N: no acknowledge

Status Byte	Status Bits							
	KOI	THREUM	FFGF	FF	HB	POR	POR	POR

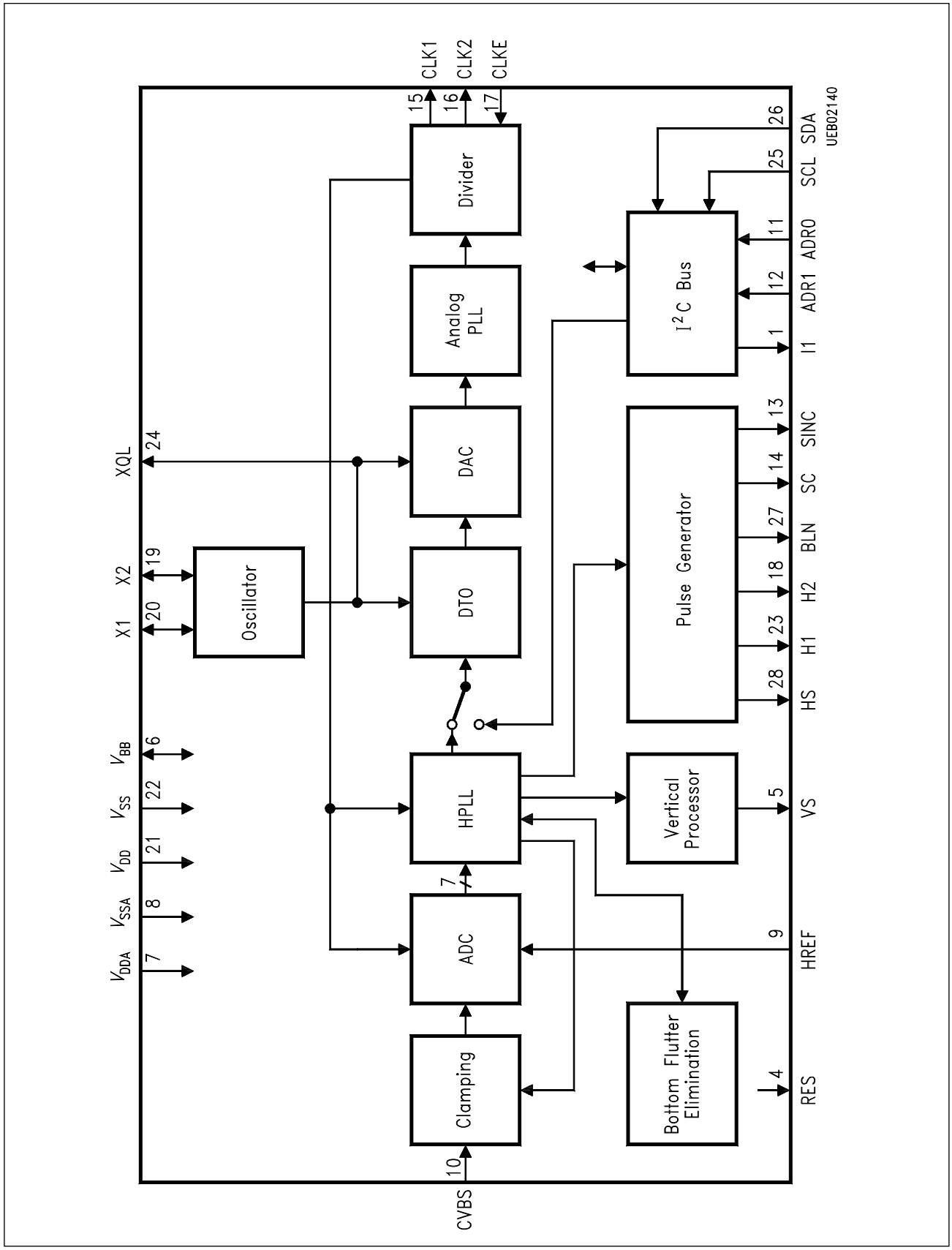
Absolute Difference in Time between the Horizontal Sync Pulse in CVBS and the HPLL	Status Bit KOI
Greater than or equal to 2.4 µs	0
Less than 2.4 µs	1

Absolute Difference in Time between the Horizontal Sync Pulse in CVBS and the HPLL	Status Bit THRELIM
Greater than 0.6 µs	0
Less than 0.6 µs for 8 or more successive lines (i.e. HPLL well locked in)	1

Identified Number of Lines per Field (refer also to timing diagram 9)	Status Bits		Control Bit VWW
	FFGF	FF	
Less than 287	0	1	×
Greater than or equal 287	0	0	×
Between 262 and 264	1	1	1
Between 312 and 314	1	0	1
Between 250 and 275	1	1	0
Between 300 and 325	1	0	0

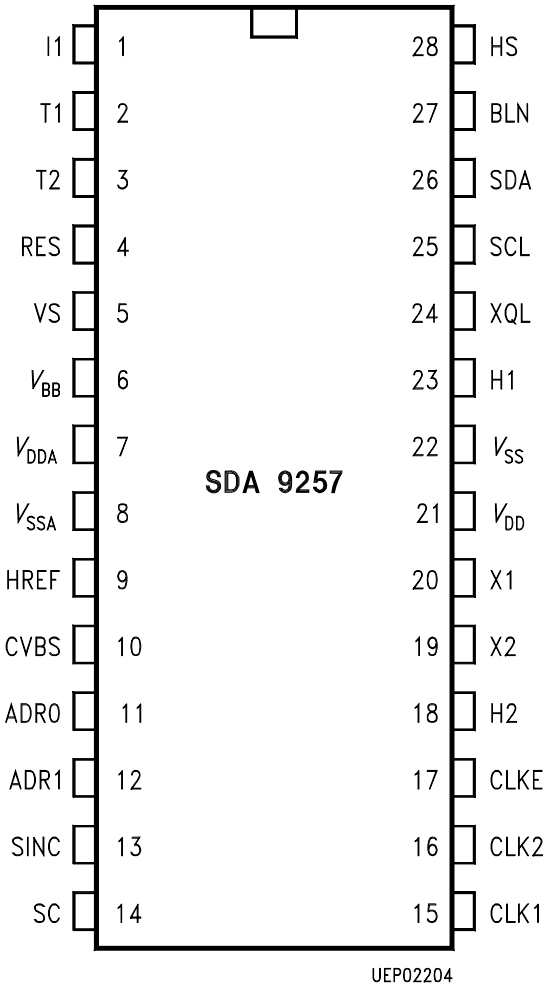
Field Detection (Applicable to Interlace Only)	Status Bit HB
First field	0
Second field	1

Status bit POR: POR is set by power on reset or by setting the bit RSTH.
POR is reset after reading the status byte.



Block Diagram

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function	Description
1	I1	I^2C Bus bit I1	Pin (e. g. for source selection) set by I^2C Bus
2	T1	Test pin	Test pin, connect to V_{SS}
3	T2	Smoothing and test pin	Internal smoothing, test pin
4	RES	Reset	Reset output, active low
5	VS	Vertical sync pulse	Tristate vertical pulse output
6	V_{BB}	V_{BB}	Substrate bias
7	V_{DDA}	+ 5 V	Analog supply
8	V_{SSA}	Ground	Analog ground
9	HREF	+ 3 V	High reference voltage
10	CVBS	CVBS	CVBS input, 2 V_{SS} nom.
11	ADR0	Address 0	I^2C-chip select
12	ADR1	Address 1	
13	SINC	Serial increment	Output for serial increment or inverse burst-key output
14	SC	Sandcastle	SC, SSC or CS output
15	CLK1	Clock 1	Tristate clock output, 24-32 MHz
16	CLK2	Clock 2	Tristate clock output, 12-16 MHz or 24-32 MHz
17	CLKE	External clock	External clock input, 24-32 MHz
18	H2	Clamping pulse	Clamping pulse input
19	X2	Xtal 2	Crystal connection
20	X1	Xtal 1	Crystal connection (clock input)
21	V_{DD}	+ 5 V	Digital supply
22	V_{SS}	Ground	Digital ground
23	HI	Clamping pulse	Clamping pulse output
24	XQL	Xtal clock	Crystal clock output
25	SCL	Clock I^2C Bus	Clock input, I^2C Bus
26	SDA	Serial data I^2C Bus	Bi-directional data, I^2C Bus
27	BLN	Blanking out	Tristate output for Featurebox
28	HS	Horizontal sync pulse	Tristate H-pulse output

Absolute Maximum Ratings

(all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{DD} V_{DDA}	– 0.3 – 0.3	6 6	V V	
Voltages on SCL, SDA, ADR1, ADR0, TEST, XQL, CKE and HREF	V_I	– 0.3		V	
CVBS for AC coupling for DC coupling	V_I V_I	– 0.3 – 0.3		V V	
Ambient temperature	T_A	– 20	70	°C	
Storage temperature	T_{stg}	– 20	125	°C	
Total power dissipation	P_{tot}		1	W	
Thermal resistance	R_{th}		39	K/W	
Supply voltage difference	$V_{DD} - V_{DDA}$		0.25	V	

Operating Range

Supply voltage	V_{DD} V_{DDA}	4.5 4.5	5.5 5.5	V V	
Ambient temperature	T_A	– 10	70	°C	

Characteristics

T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply current	I_{DD} I_{DDA}			100 50	mA mA	No load

CVBS Input

Input signal	V_{IPP}	0.25	2	4	V	
H-sync pulse level of CVBS	V_{SY}	0		1	V	When internal clamping is not used
Input leakage current	I_I			10	µA	V_I = 0 V
Input capacitance	C_I			12	pF	
Input frequency	f	0		12	MHz	to avoid aliasing
Internal resistance of CVBS source	R_I			100	Ω	With clamping and 10 nF clamping capacitor

Input HREF

Input voltage	V_I	2.7		3	V	
Input current	I_I			15	µA	V_I = 3 V

Inputs ADR1, ADR0

L-input voltage	V_{IL}	0		0.8	V	
H-input voltage	V_{IH}	2		V_{DD}	V	
Input leakage current	I_I			10	µA	V_I = 5.5 V
Input capacitance	C_I			7	pF	

SCL Input – SDA Input/Output

L-input voltage	V_{IL}	0		1.5	V	
H-input voltage	V_{IH}	3		V_{DD}	V	
Input capacitance	C_I			10	pF	
Input leakage current	I_I			7	µA	V_I = 5.5 V
Input frequency	f_{SCL}			100	kHz	
Max. capacitance on bus	C_{max}			400	pF	

Characteristics (cont'd)

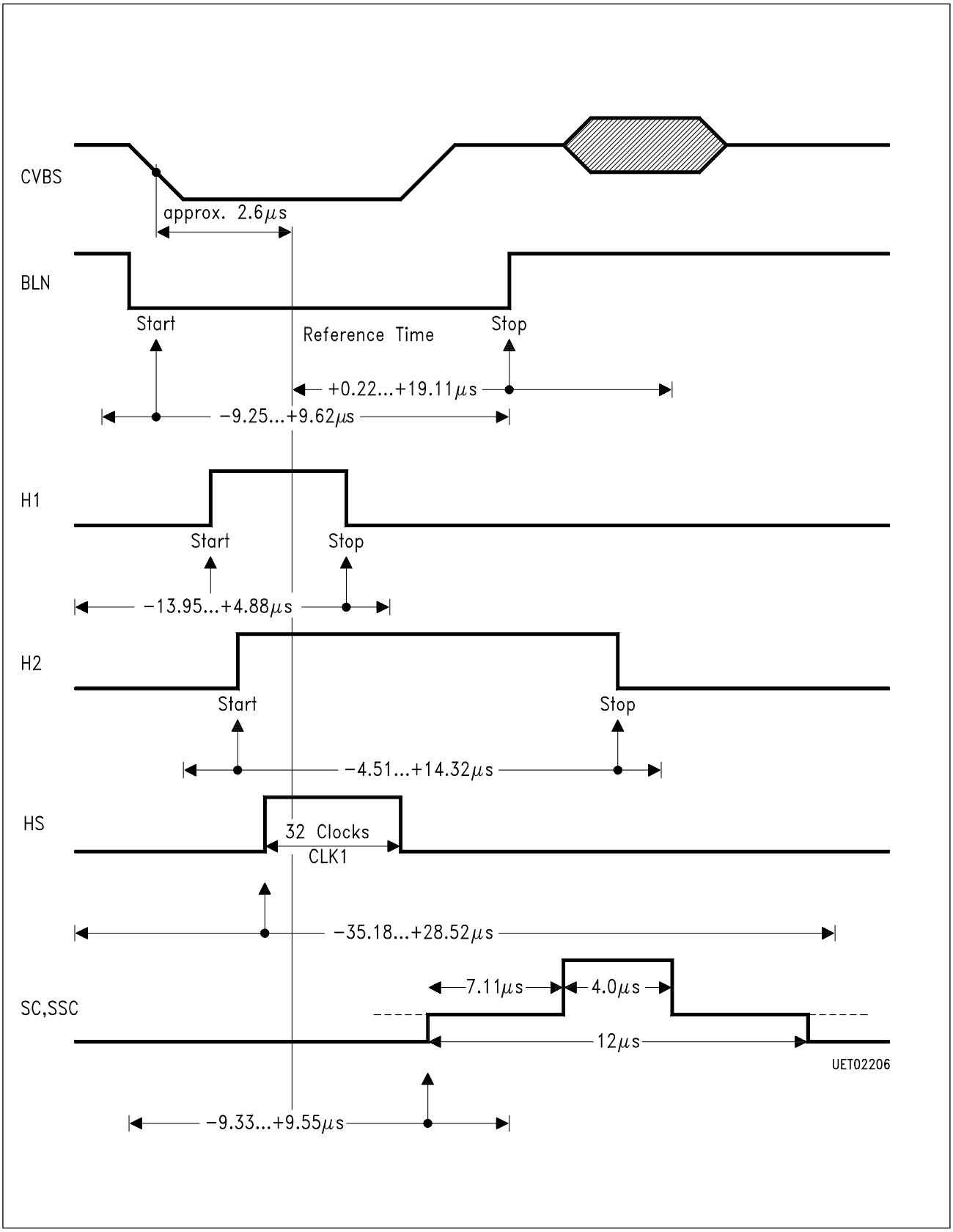
T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Fall time (acknowledge)	t_F			0.3	µs	from 3 to 1 V
SDA upon acknowledge	V_{AL}	0		0.4	V	I_{AL} = 3 mA
CKE Input						
L-input voltage	V_{IL}	0		0.8	V	
H-input voltage	V_{IH}	2		V_{DD}	V	
Input capacitance	C_I			10	pF	
Input leakage current	I_I			7	µA	V_I = 5.5 V
Input frequency	f_{CKE}			35	MHZ	
Transition times	t_R, t_F			5	ns	
Crystal Connections X1, X2						
Crystal frequency	f_c	20.44	20.50	20.56	MHZ	Overall tolerance incl. temperature drift
Crystal type		Fundamental crystal				
Equivalent parallel C	C_O			7	pF	
Crystal resonant impedance	Z_R			25	Ω	
Pin capacitance	C_I			7	pF	
External capacitance	C_{ext}			30	pF	
VS, HS, H1, H2, BLN, I1 and RES Outputs						
L-output voltage	V_{QL}	0		0.4	V	I = 1.6 mA
H-output voltage	V_{QH}	2.4		V_{DD}	V	I = – 0.5 mA
Load capacitance	C_L			50	pF	
Transition times	t_R, t_F			5	ns	C_L = 30 pF
Output delay time	t_{QD}			25	ns	
Output hold time	t_{QH}	6			ns	

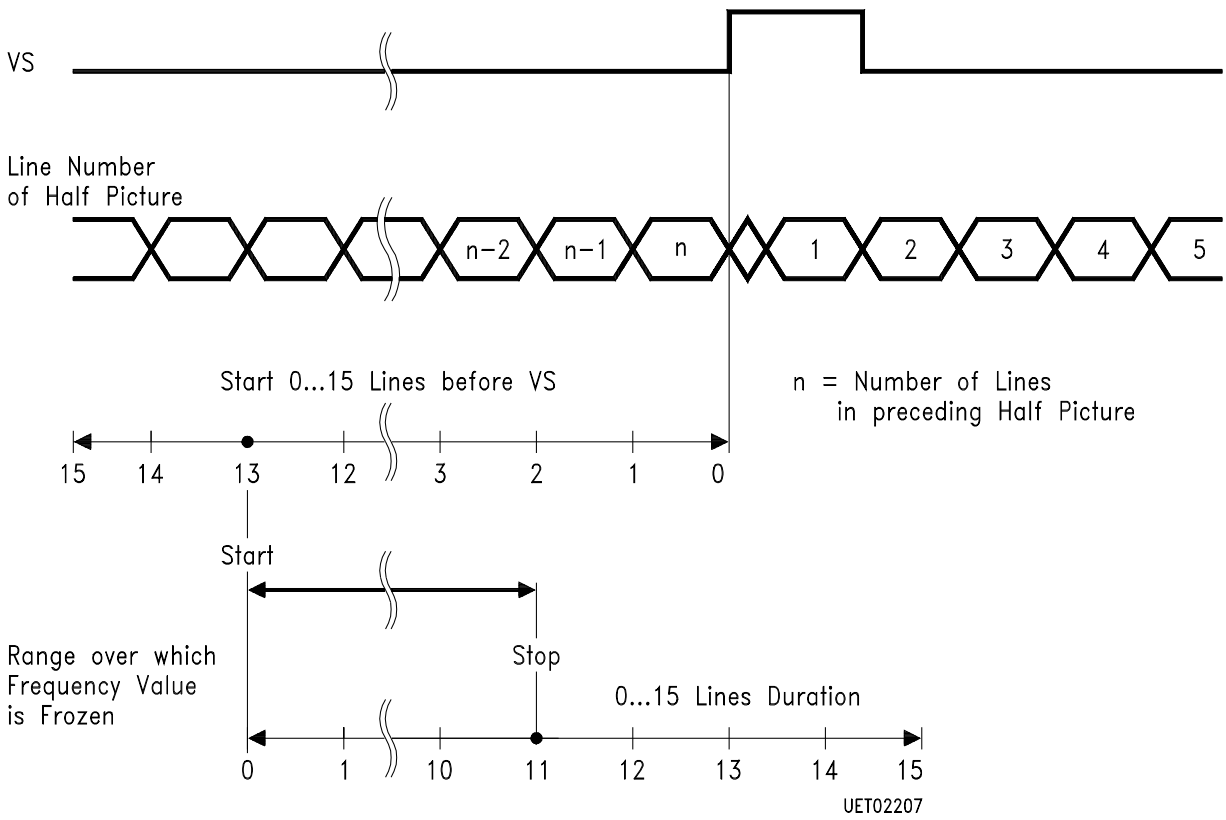
Characteristics (cont'd)

T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CLK1, CLK2 Outputs						
L-output voltage	V_{QL}	0		0.4	V	I = 1.6 mA
H-output voltage	V_{QH}	2.4		V_{DD}	V	I = – 0.5 mA
Load capacitance	C_L			50	pF	
Transition times	t_R, t_F			5	ns	C_L = 30 pF
Low time	t_{WL13}	26			ns	13.5 MHz ± 8 %
High time	t_{WH13}	26			ns	13.5 MHz ± 8 %
Low time	t_{WL27}	10			ns	27 MHz ± 8 %
High time	t_{WH27}	10			ns	27 MHz ± 8 %
Skew	t_{SK}	0		4	ns	
Jitter (rms)	t_j			3	ns	TV-time constant, 0.6 V nominal sync amplitude
Frequency range when PLL is locked at CVBS	f	25.72	27.00	28.26	MHz	
SINC Output						
L-output voltage	V_{QL}	0		0.4	V	I = 1.6 mA
H-output voltage	V_{QH}	2.4		V_{DD}	V	I = – 0.5 mA
Load capacitance	C_L			50	pF	
Transition times	t_R, t_F			5	ns	C_L = 30 pF
SC Output						
H-output voltage	V_{QH}	4.4		4.9	V	I = – 0.5 mA
Vertical level output voltage	V_{QV}	2.1	2.5	2.6	V	for SSC I = – 0.3 mA
L-output voltage	V_{QL}		0.4	0.8	V	I = 1.6 mA
Load capacitance	C_L			30	pF	
Transition times	t_R, t_F			5	ns	for composite sync
Transition times	t_R, t_F			100	ns	for SC or SSC
Output delay time	t_{QD}			25	ns	for composite sync
Output hold time	t_{QH}	6			ns	for composite sync

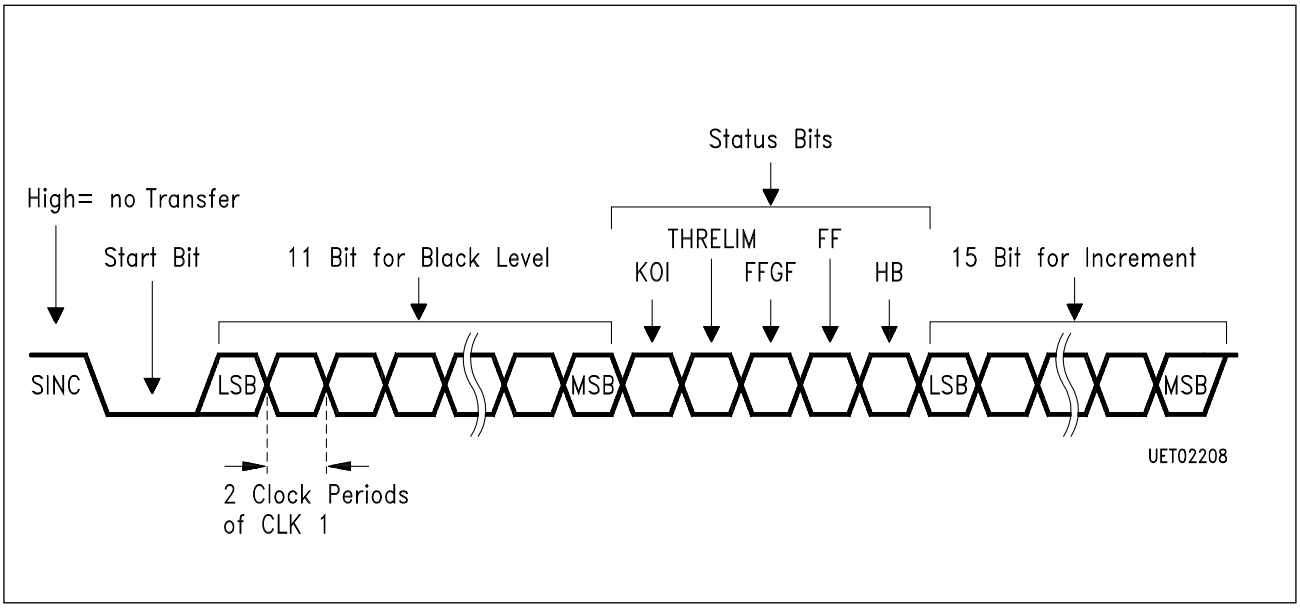


Timing Diagram 1
I²C Bus Programming Areas of Horizontal-Frequency Pulses

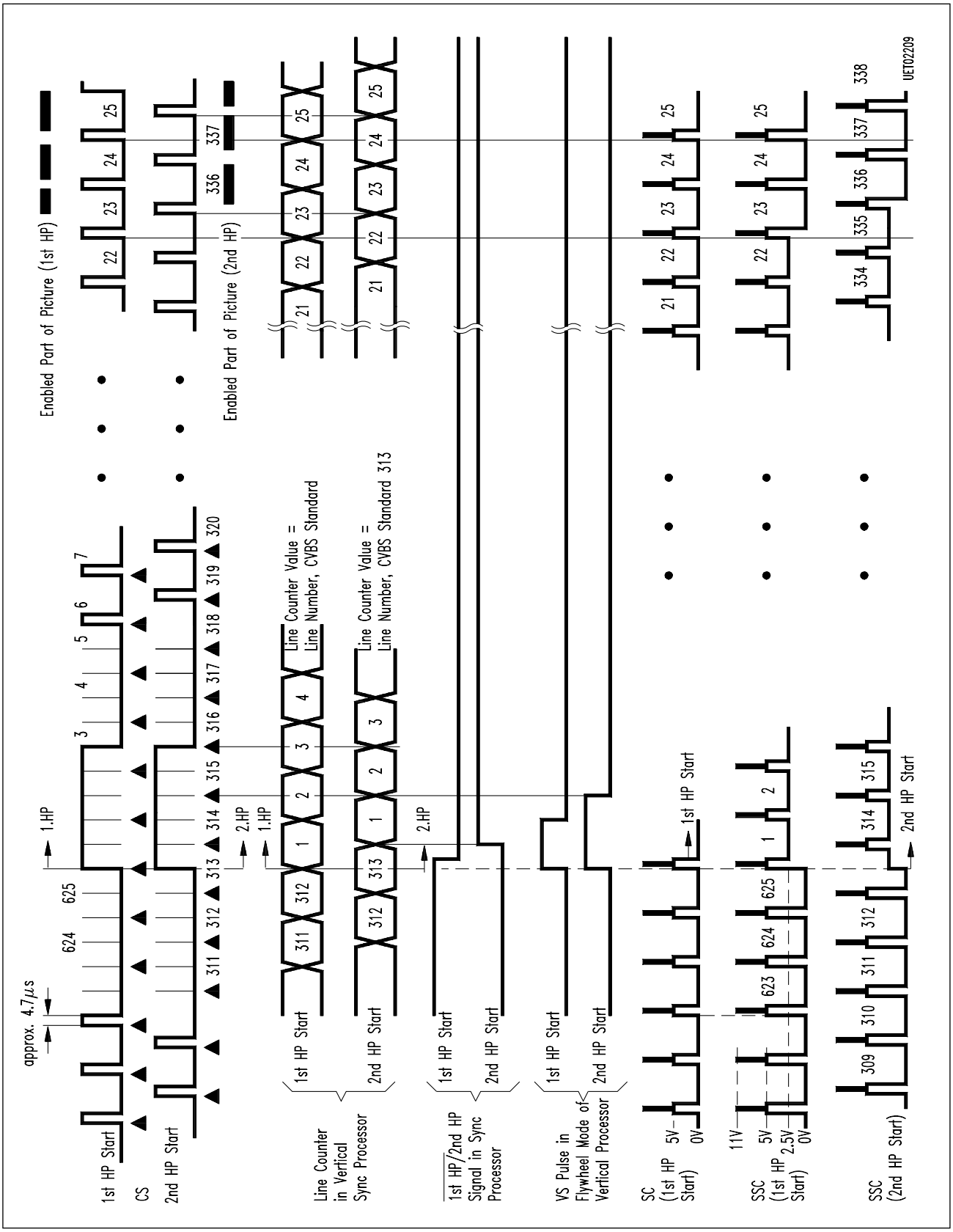


(In this example the frequency value was frozen 13 lines before the VS pulse and for a duration of 11 lines).

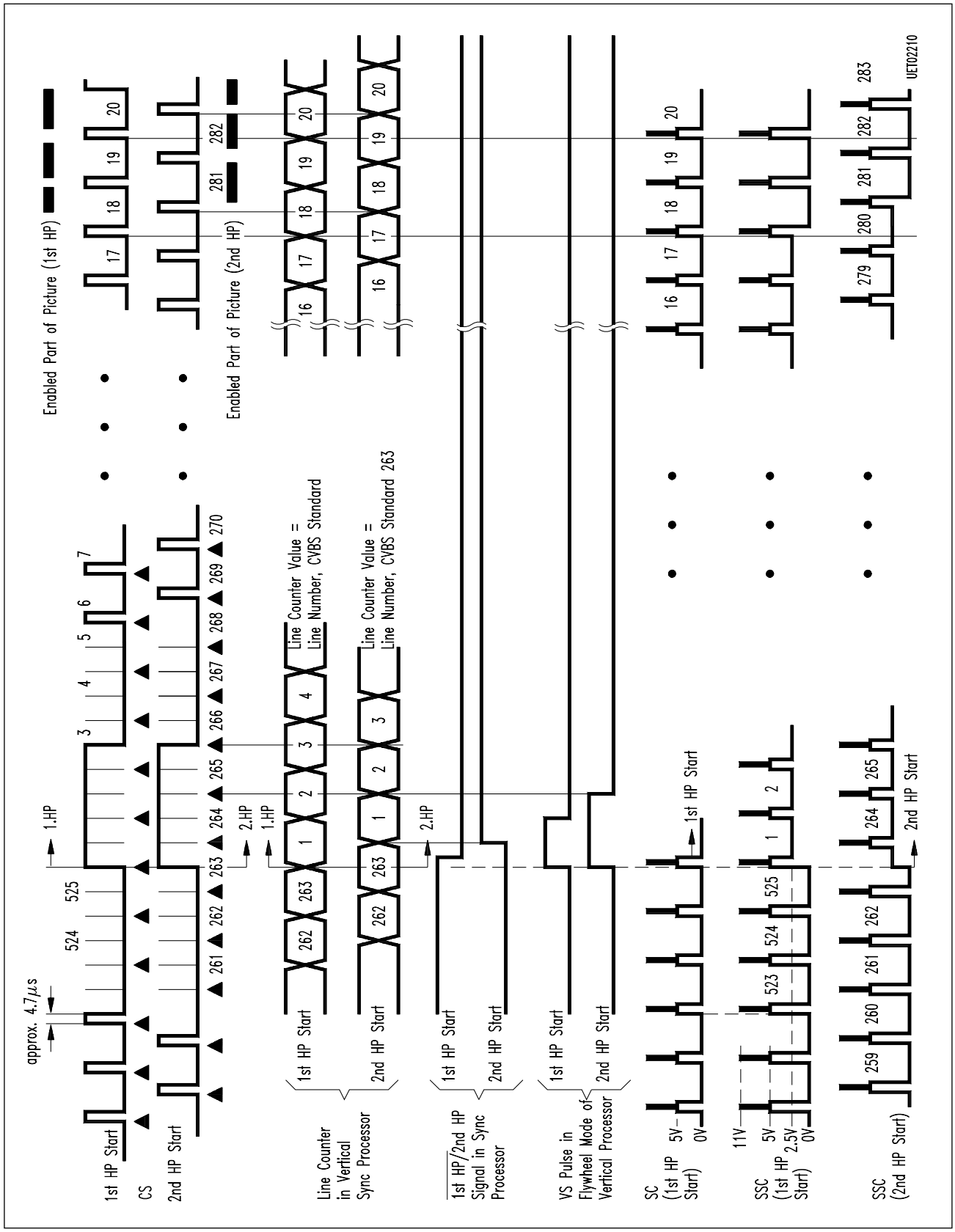
Timing Diagram 2
I²C Bus Programming Area in which Clock Frequency Value Generated by HPLL can be Frozen



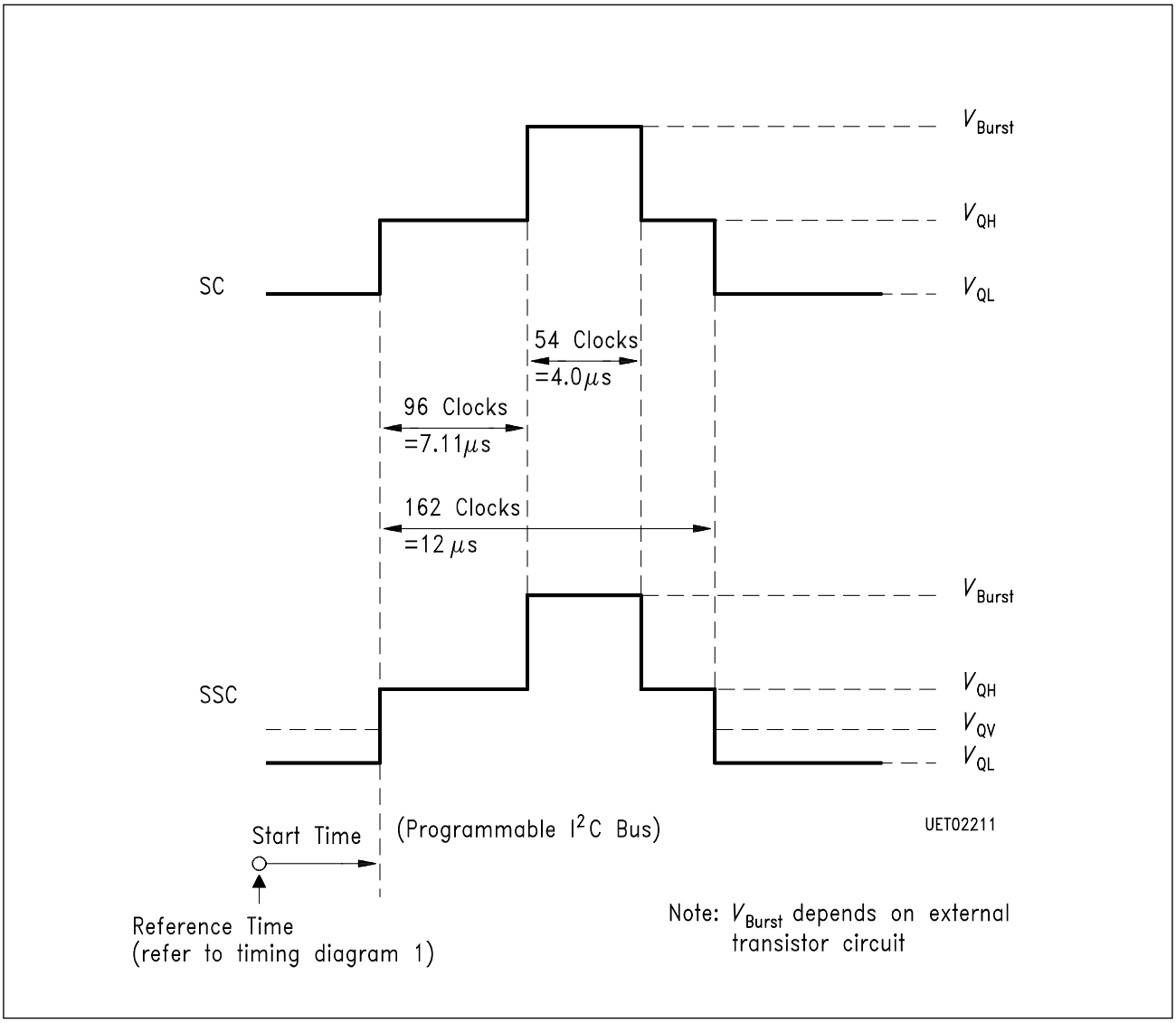
Timing Diagram 3
Serial Transfer of Increment, Black Level and Status Bits on Pin SINC (once for each TV line)



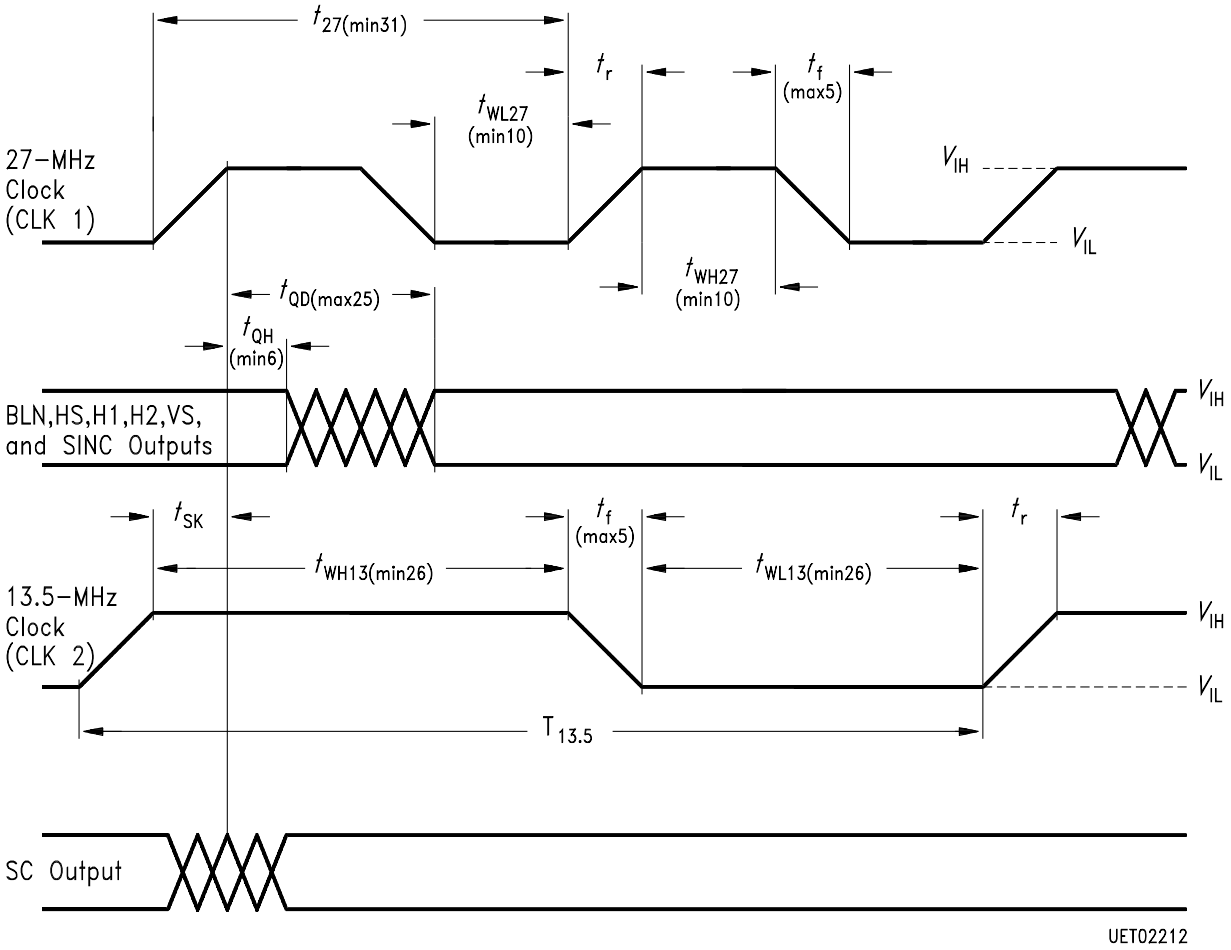
Timing Diagram 4
Sandcastle, Super Sandcastle, VS and Composite Sync CS at 50 Hz



Timing Diagram 5
Sandcastle, Super Sandcastle, VS and Composite Sync CS at 60 Hz

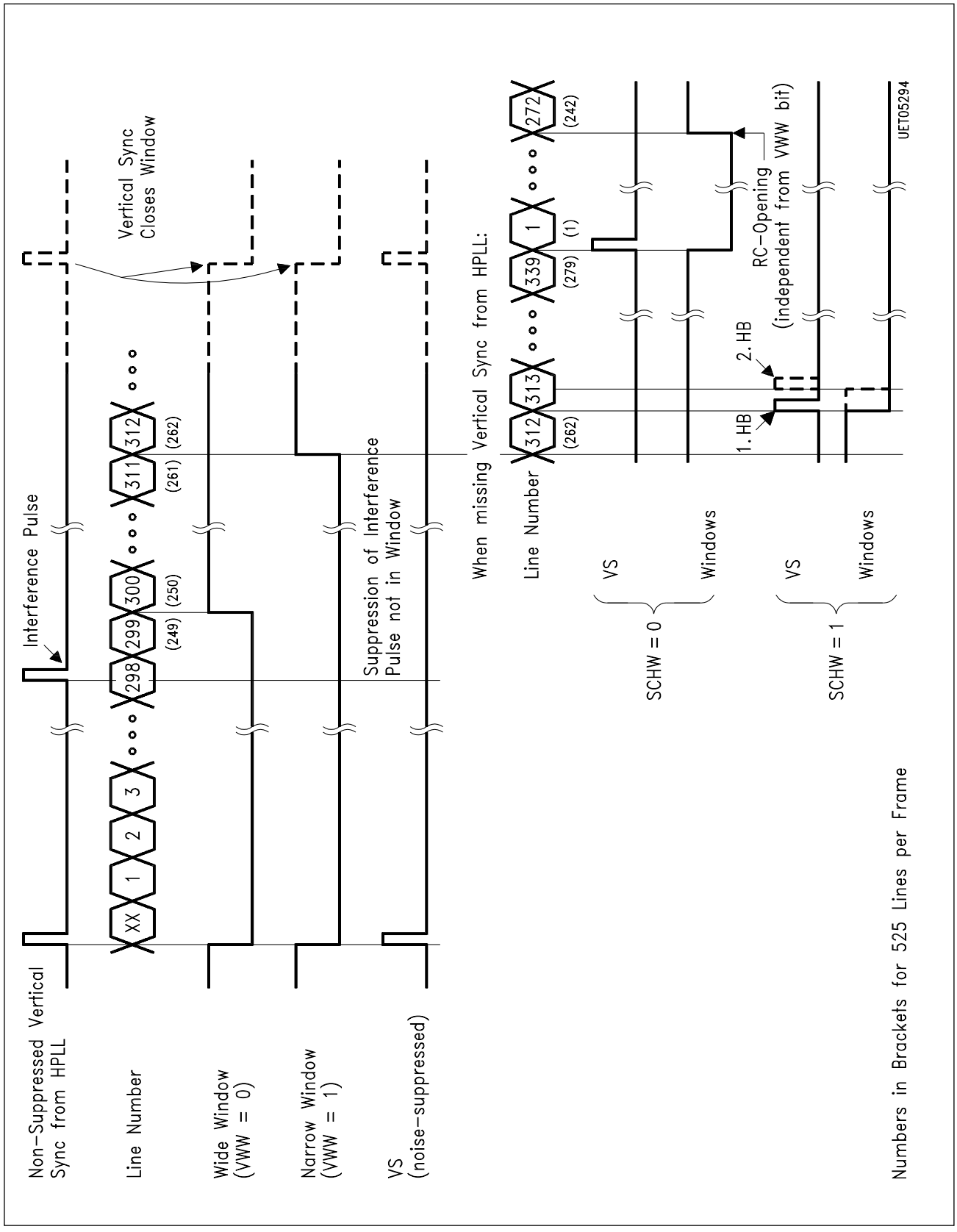


Timing Diagram 6
Sandcastle and Super Sandcastle Pulse

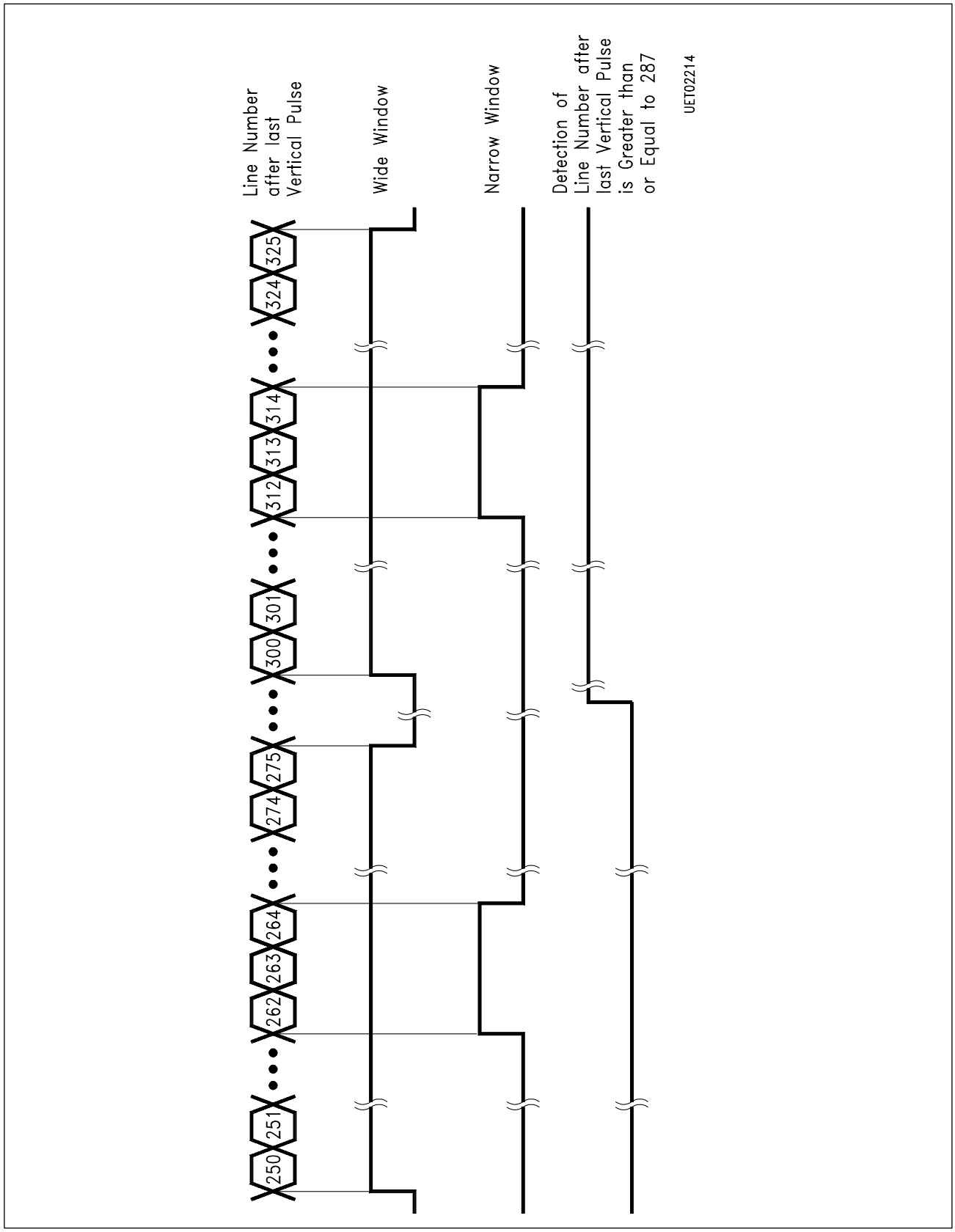


Timing of output clock satisfies PIP and Featurebox specifications and also the general specification for 27-MHz interfaces

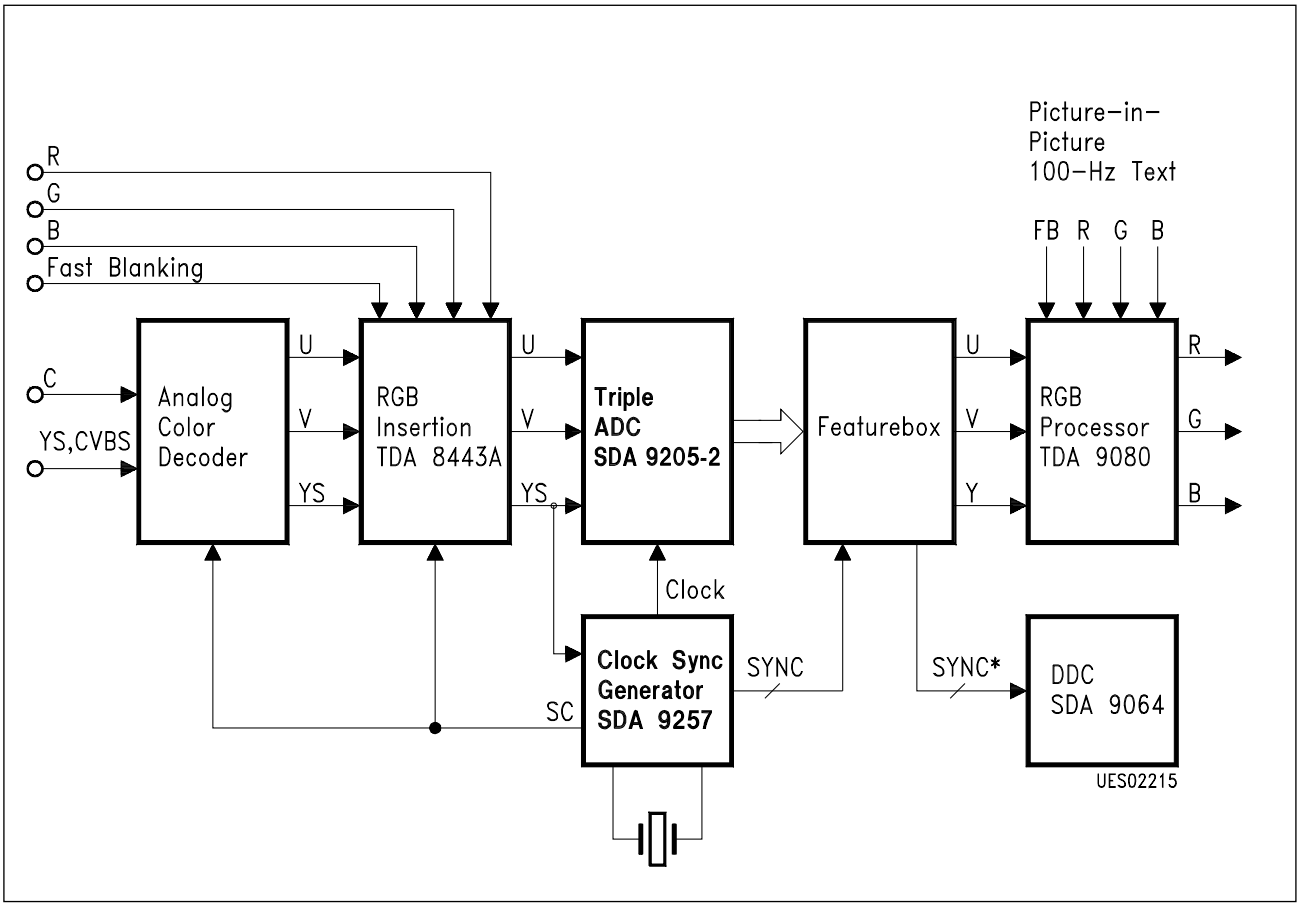
Timing Diagram 7
Output Clocks and Data



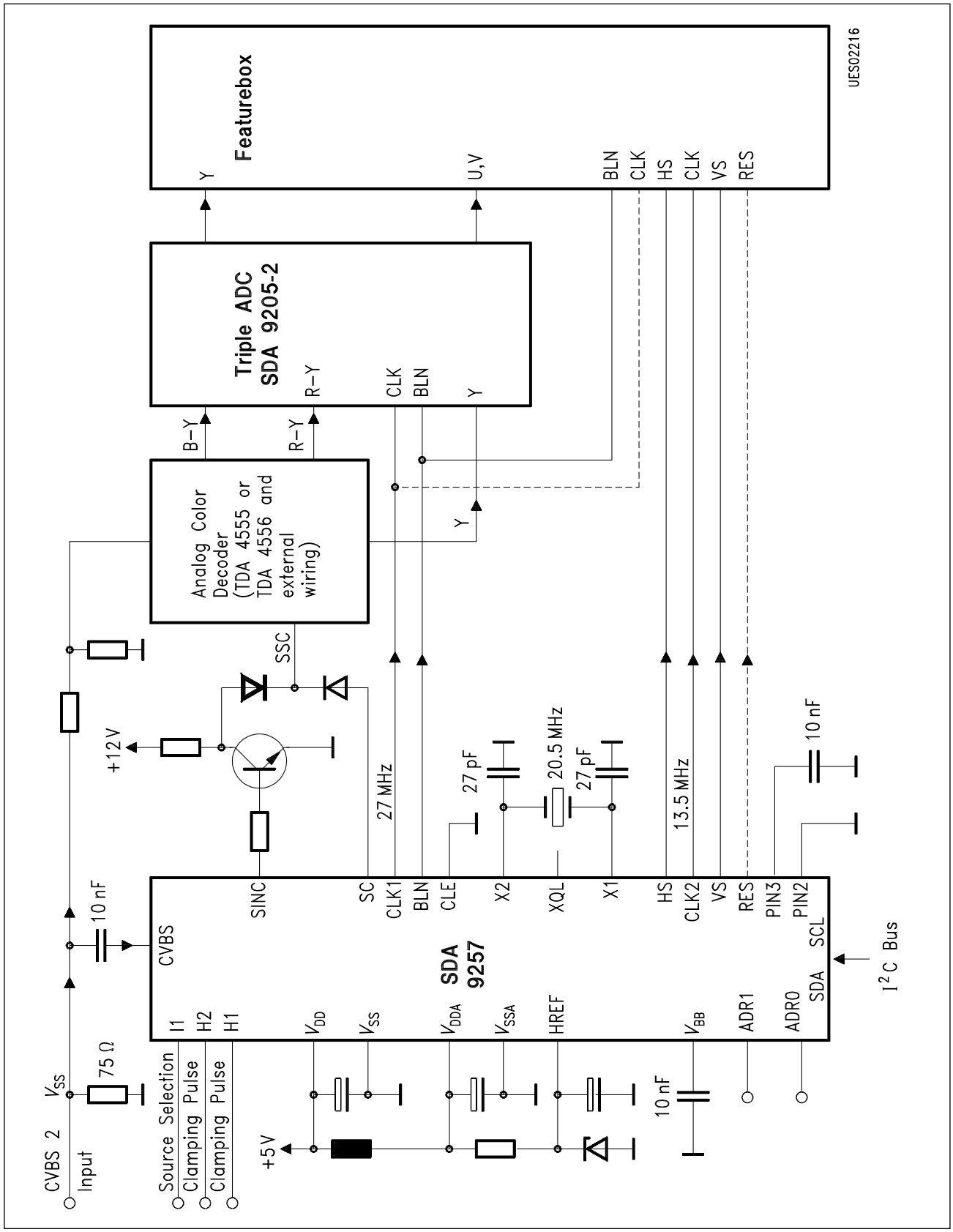
Timing Diagram 8
Window for Vertical Pulse Noise Suppression



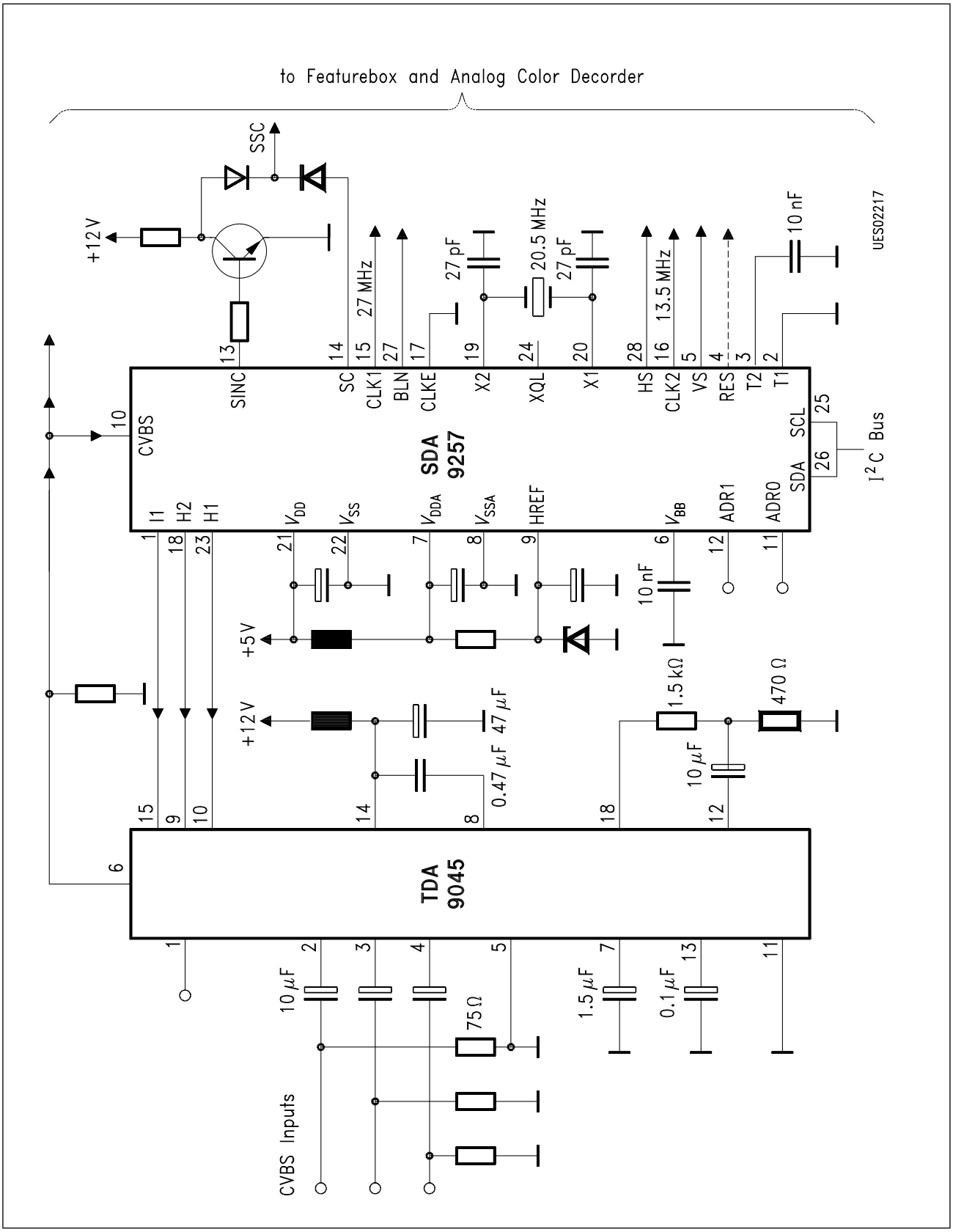
Timing Diagram 9
Window for Detection of Number of Lines per Field



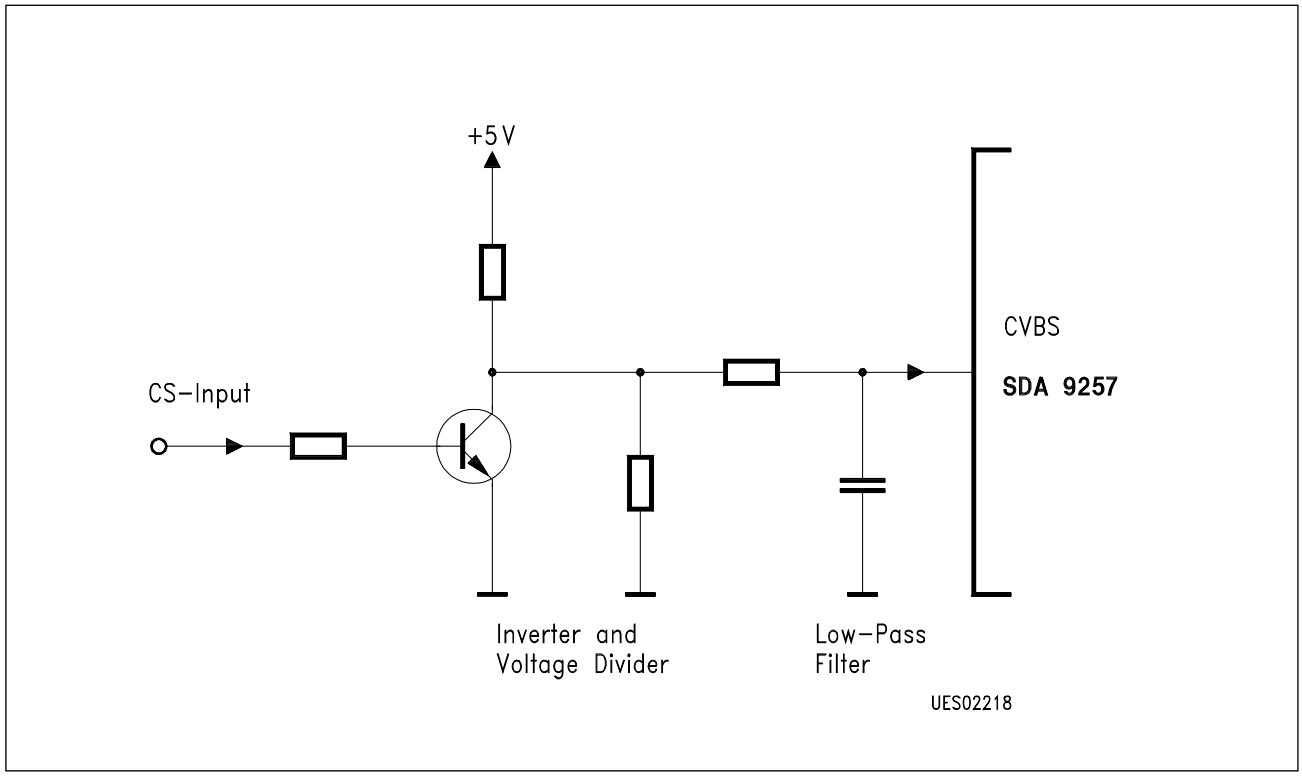
Application Circuit 1
Featurebox Environment with Analog Color Decoder



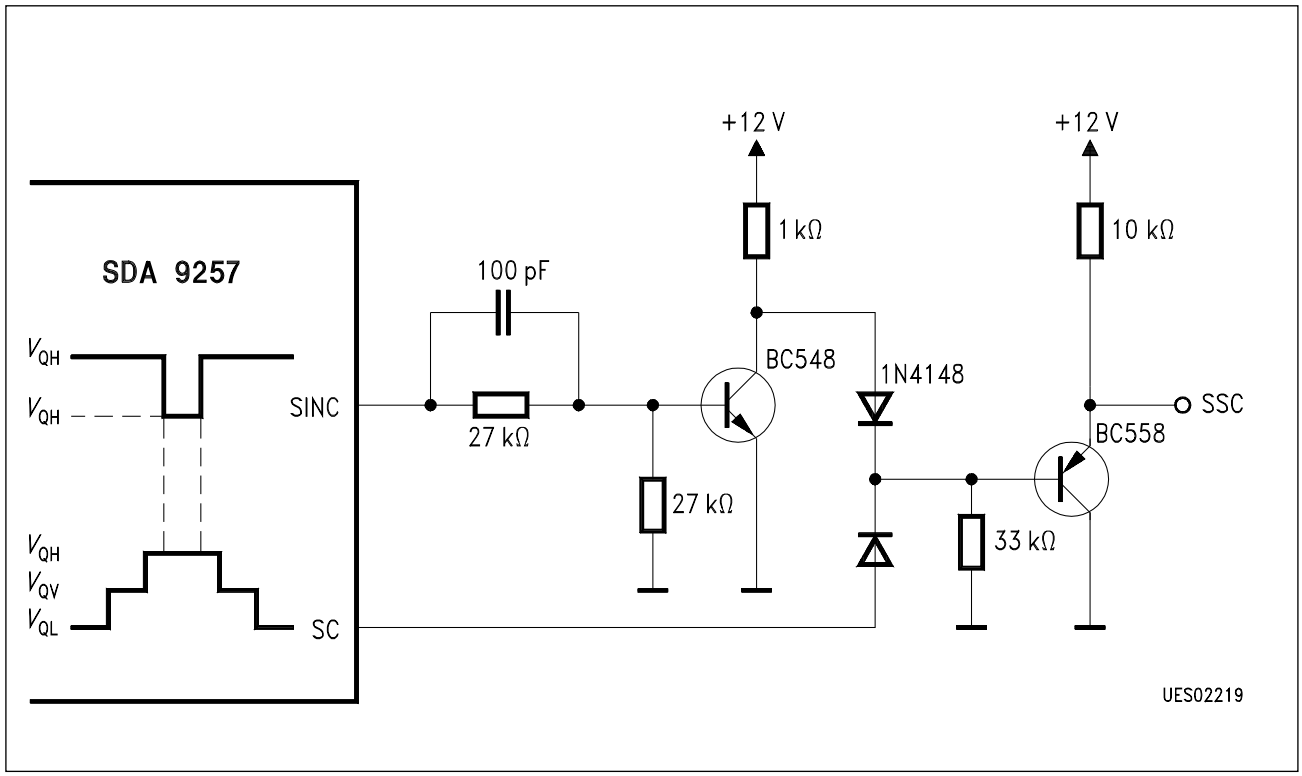
Application Circuit 2
Featurebox Environment with Analog Color Decoder



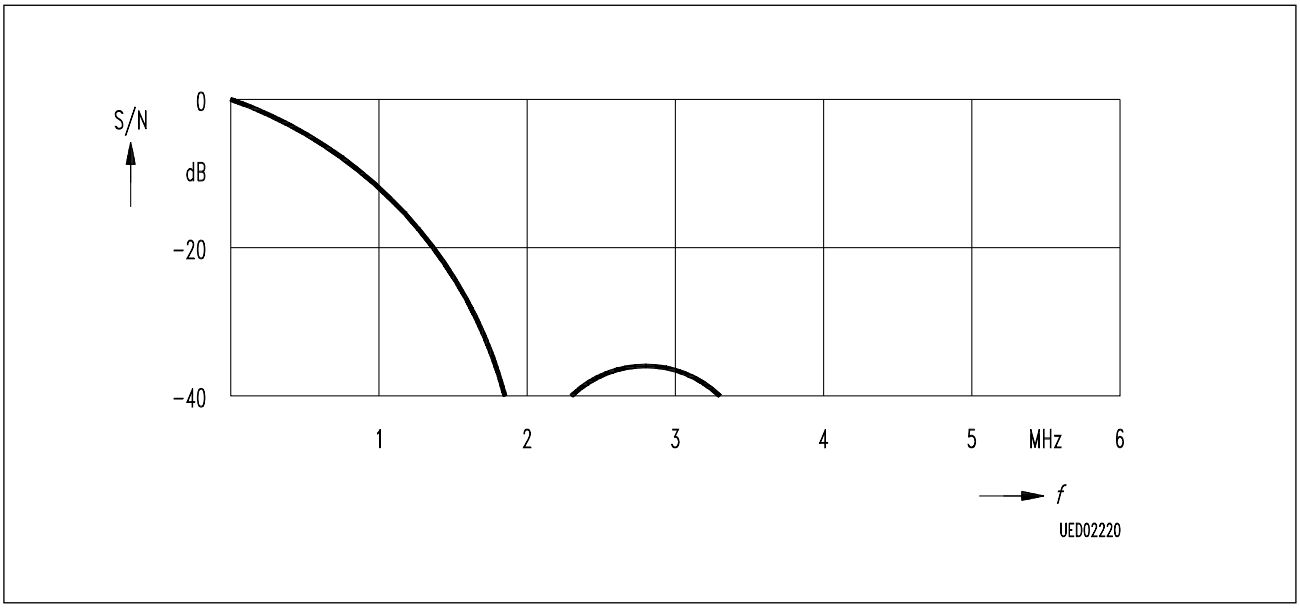
Application Circuit 3
CSG and PAMUX TDA 9045



Application Circuit 4
Input Circuit with Composite Sync as Source



Application Circuit 5
Possible Output Circuit for Generating Super Sandcastle



Frequency Response of Noise Suppression S of the Composite Sync Output Signal in Relation to CVBS Input