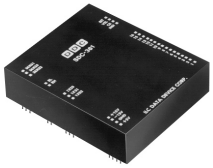


16-BIT, TWO SPEED SYNCHRO-TO-DIGITAL AND RESOLVER-TO-DIGITAL CONVERTER

DESCRIPTION

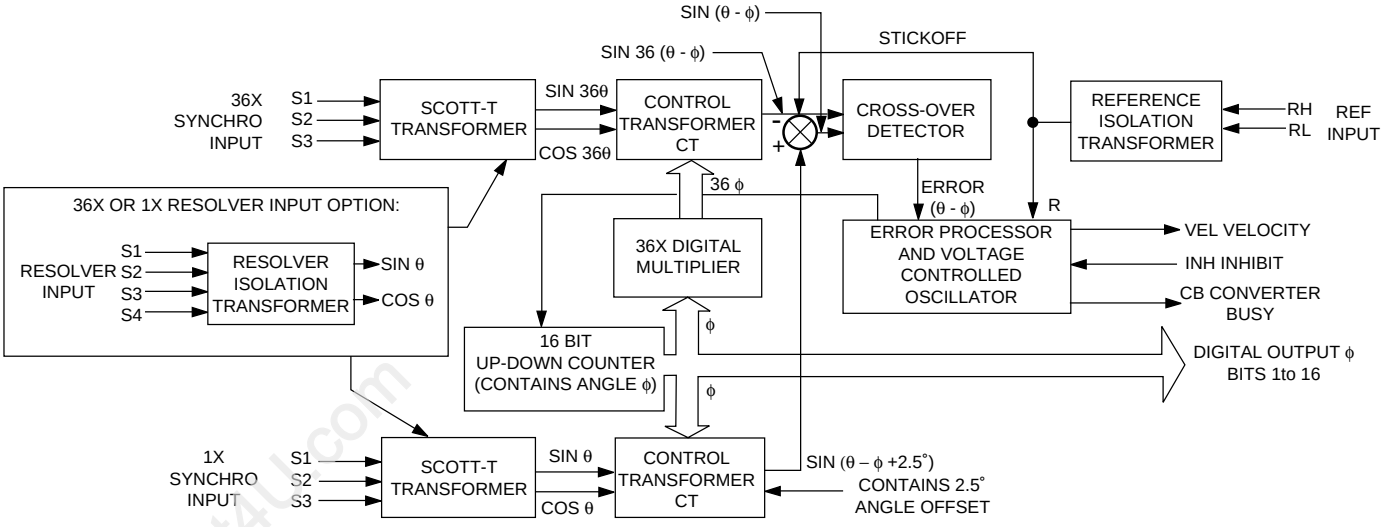
The SDC-361 is a low-cost, single module synchro-to-digital (S/D) and resolver-to-digital (R/D) tracking converter. A unique control transformer algorithm is used that provides inherently higher accuracy and jitter-free output. Other features include a BIT logic signal to indicate proper tracking and an analog velocity output. Utilizing a type II servo loop, these converters have no velocity lag up to the specified tracking rate, and output data is always fresh and continuously available. Each unit is fully trimmed and requires no adjustment.

APPLICATIONS

The SDC-361 may be used wherever analog angle data from synchros or resolvers must be converted rapidly and accurately to digital form for transmission, storage and analysis. Because these units are extremely rugged and stable, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial, commercial and military applications. Military ground support and avionics uses include ordnance control, radar tracking systems, navigation and collision avoidance systems.

FEATURES

- ***Accuracy: ±1 LSB = ±20 Seconds***
- ***SIGNAL AND REF INPUTS:***
  - ***Internal Transformer Isolation***
  - ***Broadband Input: 350-3000 Hz or 47-3000 Hz***
  - ***All common L-L voltage levels***
- ***LOGIC:***
  - ***TTL Compatible***
  - ***16-Bit Parallel Binary Angle Output, and Converter Busy, Inhibit and BIT***
- ***POWER REQUIREMENTS:***
  - ***±15 VDC and +5 VDC***



NOTE: Block Diagram Illustrates SDC-361. All References to "36X" are "18X" for SDC-362.

FIGURE 1. BLOCK DIAGRAM

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TABLE 1. SDC-361/362 SPECIFICATIONS		
PARAMETER	**VALUE**	
RESOLUTION	16 bits	
ACCURACY		
SDC-361	±1 LSB (20 sec)	
SDC-362	±1 LSB (40 sec)	
SIGNAL AND REFERENCE INPUT		
(All inputs transformer isolated. Other freq. and volt. available.on special order.)	Signal Frequency Range	Signal Input Impedance (L-L Balanced, Resistive)
Synchro Input		
90V L-L, 400 Hz (Option H)	350-3000 Hz	148 Kohm min
90V L-L, 60 Hz (Option I)	47-3000 Hz	148 Kohm min
11.8V L-L, 400 Hz (Option L)	350-3000 Hz	19 Kohm min
Resolver Input		
90V L-L, 400 Hz (Option H)	350-3000 Hz	148 Kohm min
26V L-L, 400 Hz (Option I)	350-3000 Hz	42 Kohm min
11.8V L-L, 400 Hz (Option L)	350-3000 Hz	19 Kohm min
	Reference Frequency Range	Reference Input Impedance (L-L Balanced, Resistive)
Reference Input		
(Option H, I)	40-150 V rms	300 Kohm min
(Option M, L)	10- 50 V rms	80 Kohm min
DIGITAL INPUT/OUTPUT		
Logic Type	TTL	
Inhibit Input (INH) Loading	Logic “0” inhibits, 0.2 Std TTL loads plus 18 Kohm min pull-up resistor to +5 V supply.	
Outputs		
16 Parallel data Bits	Natural binary angle; pos. logic	
Converter Busy (CB)	1-2.5 µsec positive pulse, data changes on leading edge	
Drive Capabilitity	2 Std TTL loads (Consult factory for 5 Std load capability)	
BIT (Bilt In Test)	Logic 0 = normal tracking Logic 1 = not tracking within fine speed range	
ANGULAR VELOCITY OUTPUT		
Scale Factor	±1.0 VDC ±30% for 100°/sec at 400 Hz ±1.0 VDC ±30% for 25°/sec at 60 Hz	
Range	±10 VDC min	
Loading	±10 Kohm max	
DYNAMIC CHARACTERISTICS		
Input Rate for Full Velocity		
Options H, M, L (400 Hz)	0-1000°/sec minimum	
Option I (60 Hz)	0-250°/sec minimum	
Acceleration for 1 LSB Lag		
Options H, M, L(400 Hz)	384°/sec² typ	
Option I (60 Hz)	23°/sec² typ	
Settling Time		
For Normal Tracking (Up to specified Input Rate)	No Lag Error	
For 179° Step Change (Typical Values)		
Options H, M, L (400 Hz)		
Settling to 1 LSB	400 msec	
Settling to Final Value	480 msec	
Options I (60 Hz)		
Settling to 1 LSB	1400 msec	
Settling to Final Value	1800 msec	

TABLE 1. SDC-361/362 SPECIFICATIONS (CONTD)			
PARAMETER	**VALUE**		
DYNAMIC CHARACTERISTICS (Continued)			
Velocity Constant (Type II Servo Loop)	Kv = ∞		
Acceleration Constant			
Options H, M, L (400 Hz)	K_A = 70,000 Nominal		
Option I (60 Hz)	K_A = 4,300 Nominal		
POWER SUPPLIES			
Nominal Value	+15 V	-15 V	+5 V
Voltage Range	+11.5 to +16.5 V	-11 to -16.5 V	+ 4.5 to + 5.5 V
Max Voltage without Damage	+18 V	-18 V	+7 V
Current			
Typical	10 mA	35 mA	110 mA
Maximum	15 mA	50 mA	150 mA
TEMPERATURE RANGES			
Operating			
-1 Option	-55°C to + 105°C		
-3 Option	0°C to + 70°C		
Storage	-55°C to + 125°C		
PHYSICAL CHARACTERISTICS			
Size	3.125 x 2.625 x 0.82 inches (79.4 x 66.7 x 20.8 mm)		
Weight	7 oz (200 g)		

INTRODUCTION

The operation of a two speed S/D is essentially the same as a single speed module, except there are two control transformers (CT) which generate two error voltages. These two CTs are fed by a common up-down counter. The counter data is multiplied by 36 for an SDC-361 and 18 for an SDC-362 to generate the fine speed CT. Assuming an off-null condition as when the system is initially energized, the crossover detector feeds the coarse (1X) CT error signal output to the demodulator and error processor. The converter seeks a null as it would for a single speed S/D. As null is approached (to within 2.5° nominally) the coarse CT output drops below a preset threshold and the crossover detector then switches the fine CT error signal (36X for SDC-361, 18X for SDC-362) into the demodulator and error processor.

Since the counter angle θ is multiplied by 36X for SDC-361, and 18X for SDC-362, the gradient of the fine speed CT is 36X the coarse output CT for the SDC-361, and 18X for the coarse output CT for the SDC-362. The servo loop then seeks a finer null, using the fine speed CT error signal. The converter continues to use the fine error signal for continuous tracking, and only switches back to the coarse signal when the coarse error exceeds the crossover threshold. To eliminate false stable nulls at 180°, an angle offset and stickoff voltage are introduced in the coarse channel. The ±15 V power supplies can vary over their specified ranges with no change in the converter specifications except for a proportional change in the maximum ± tracking rates. When testing or evaluating the converters, it is advisable to limit the current to each of the three power supplies. Set each current limit to 50% greater than the maximum current listed for that supply in TABLE 1.

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To prevent damage to the input transformers, the maximum voltage should not exceed the specified input voltage by more than 30%. The maximum common mode voltage (DC plus recurrent AC peak) should not exceed 500 V.

DIGITAL INPUTS

Logic inputs are low power Schottky and the can drive remote loads. The BIT logic output is a built-in-test derived from the crossover detector. It goes to logic 1 whenever the digital output is not tracking the input signal within the range of the fine speed synchro or resolver.

TABLE 2. BIT WEIGHT

BIT	DEG/BIT	MIN/BIT
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.406	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	.66
16	0.0055	.33

TIMING

Whenever an input signal change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy pulse (CB). The output data change is initiated at the leading edge of the CB pulse, and the output is stable within 0.2 µsec after the leading edge. Extra CB pulses will not occur if the input angle changes while the counter is locked by the INH. The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the inhibit is applied. The converter will ignore an inhibit applied during the "busy" interval until that interval is over. Timing is as follows: (a) apply the inhibit, (b) wait 0.2 µsec, (c) transfer the data and (d) release the inhibit.

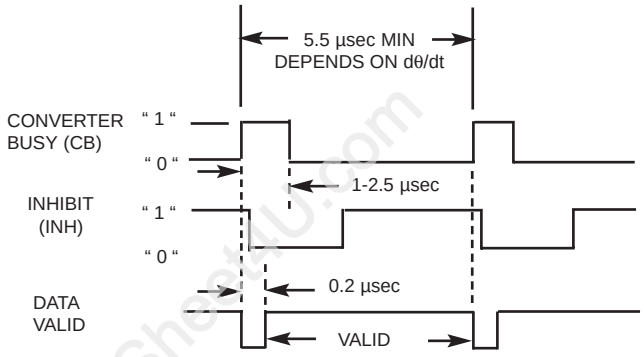

TABLE 2. TIMING DIAGRAM

ANALOG VELOCITY OUTPUT

VEL is a DC voltage proportional to the angular velocity $d\theta/dt = d\phi/dt$. The output is derived from an op-amp with low output impedance and is short-circuit protected. Other characteristics are listed in TABLE 1.

DYNAMIC PERFORMANCE

A Type II servo loop (Kv = ∞) and very large acceleration constants give these converters superior dynamic performance, as listed in TABLE 1. If the power supply voltages are not the ±15 VDC nominal values, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage. The +15 V supply voltage will determine the maximum positive velocity. The -15 V supply voltage will determine the maximum negative velocity.

As long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.

The loop dynamics of DDC's tracking S/D converters are described by the unity feedback configuration shown. The closed-loop transient response is nominally critically damped, and all loop dynamics can be determined from the diagram and formulas given.

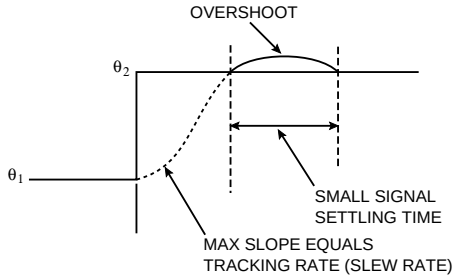

FIGURE 3. STEP RESPONSE INPUT

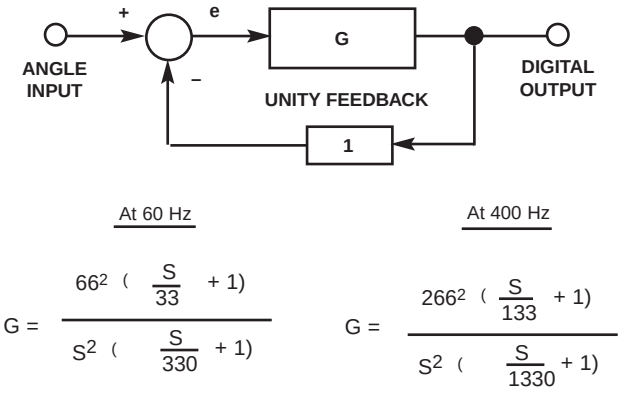

FIGURE 4. S/D CONVERTER LOOP DYNAMICS

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ACCURACY TESTS

Because of the accuracy of DDC's S/D converters, only laboratory grade synchro or resolver substitution boxes or standards should be used. If synchro standards are not available, arrangements may be made to witness the final source inspection at the DDC factory. The figure below shows how to setup equipment to measure S/D converter accuracy. A separate lamp driver or suitable readout is required for each output data line. The synchro standard is set to any desired test angle, and the lamps which are lit are added according to their bit weights and compared with the test angle.

PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from AC and power signal as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope probes, and to keep digital noise from coupling into the sensitive AC signals.

It is strongly recommended that circuit layouts be designed so plated through-holes are not required to mount hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a connection by ripping out the plated through-hole connection if the module must be replaced. It will also be easier to unsolder the module without the module being damaged.

TEST METHODS FOR DISCRETE MODULES

All of DDC's discrete S/D converter modules are high quality products whose semiconductor components are hermetically sealed. Discrete modules will meet specific test methods and conditions of MIL-STD-202E shown below unless alternate methods are specified by the customer in his procurement documentation.

TABLE 4. MIL-STD-202E TEST METHODS

METHOD	CONDITION	COMMENT
204C	C	10G, 2000 Hz vibration
213B	A	50G, 11 ms shock
106D *	--	Moisture
107D	A	Thermal shock
101D	B	Salt spray
105C	B	50,000 ft, altitude

* when conformally coated on P.C. board

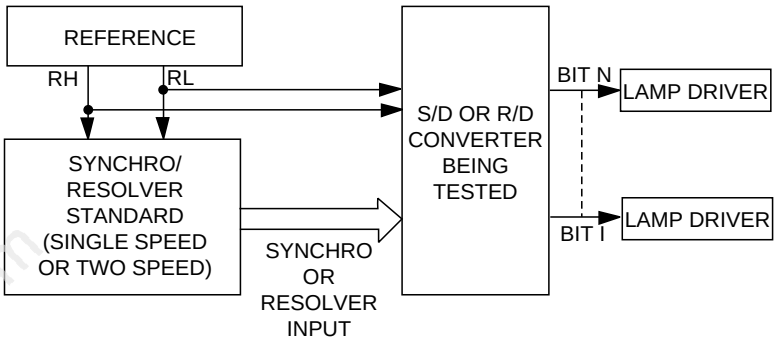

FIGURE 5. ACCURACY TEST CIRCUIT

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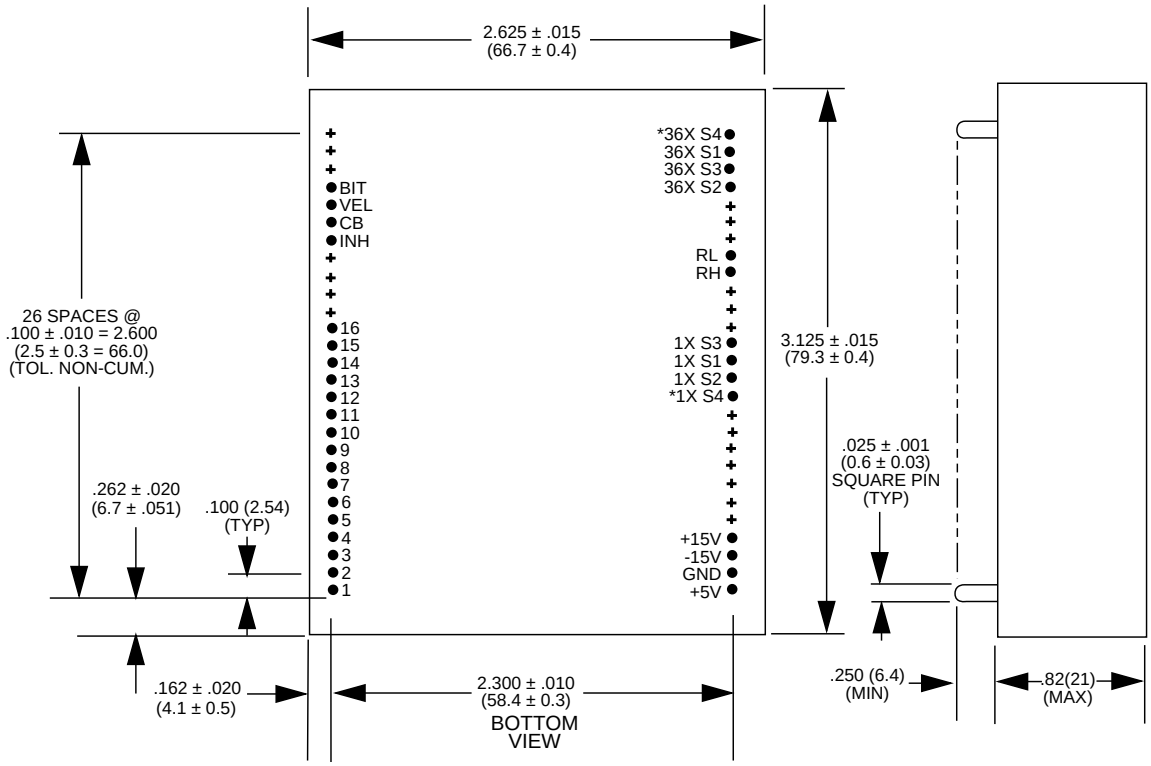

Notes:
1. All reference to 36X become 18X on SDC-362.
2. Pin labels for reference only.
3. All dimensions shown in inches (mm).
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.
6. S4 pins are present on resolver units only.

FIGURE 6. MECHANICAL OUTLINE

ORDERING INFORMATION

SDC-361-H-I

Temperature Range
- 1 = –55° to +105°C
- 3 = 0° to +70°C

Signal Input Voltage and Frequency
- H = 90 V L-L, 400 Hz (Synchro or Resolver)
- I = 90 V L-L, 60 Hz (Synchro only)
- M = 26 V L-L, 400 Hz (Resolver only)
- L = 11.8 V L-L, 400 Hz (Synchro or Resolver)

Speed
- 361 = 1 x 36 speed
- 362 = 1 x 18 speed

Input Type
- SDC = Synchro
- RDC = Resolver

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