General Description

SDC3110 combines a dedicated current mode PWM controller with a high voltage power MOSFET. It is optimized for high performance, low standby power, and cost effective off-line flyback converter applications in sub 27W range.

SDC3110 offers Complete protection coverage with automatic self-recovery feature including cycle-by-cycle current limiting (OCP), over load protection (OLP), V_{DD} over voltage clamp and under voltage lockout (UVLO). Excellent EMI performance is achieved with frequency shuffling technique, together with soft switching control at the totem pole gate drive output. The tone energy at below 22kHz is minimized in the design and audio noise is eliminated during operation

Features

- Power on soft start reducing MOSFET V_{DS} stress
- Frequency shuffling for EMI
- Extended burst mode control for improved efficiency and minimum standby power design
- Audio noise free operation
- Fixed 50kHz switching frequency
- Internal synchronized slope compensation
- Low V_{DD} startup current and low operating current
- Leading edge blanking on current sense input
- Good protection coverage with auto self-recovery:
  VDD over voltage clamp and under voltage lockout with hysteresis (UVLO)
  Line input compensated cycle-by-cycle over-current threshold setting for constant output power limiting over universal input voltage range
  Over load protection (OLP)
  Over voltage protection(OVP)

Applications

- Battery charger
- PDA power supplies
- Digital cameras and camcorder adaptor
- VCR, SVR, STB, DVD&DVCD player SMPS
- Set-top box power
- Auxiliary power supply for PC and server
- Open-frame SMPS

DIP-8

Figure 1. Package Type

Pin Configuration

Package: DIP-8

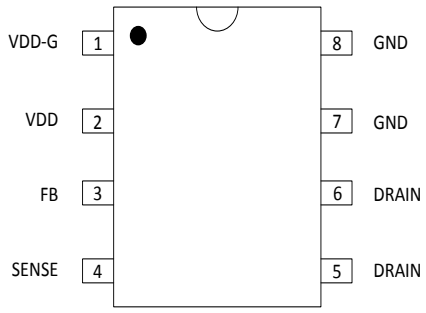


Figure 2. Pin Configuration

Pin Number	Pin Name	Function
1	VDD-G	Internal Gate Driver Power Supply
2	VDD	Chip DC power supply pin
3	FB	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at SENSE pin
4	SENSE	current sensing input
5,6	DRAIN	HV MOSFET DRAIN Pin. The DRAIN pin is connected to the primary lead of the transformer
7,8	GND	Ground

Table 1. Pin Description

Block Diagram

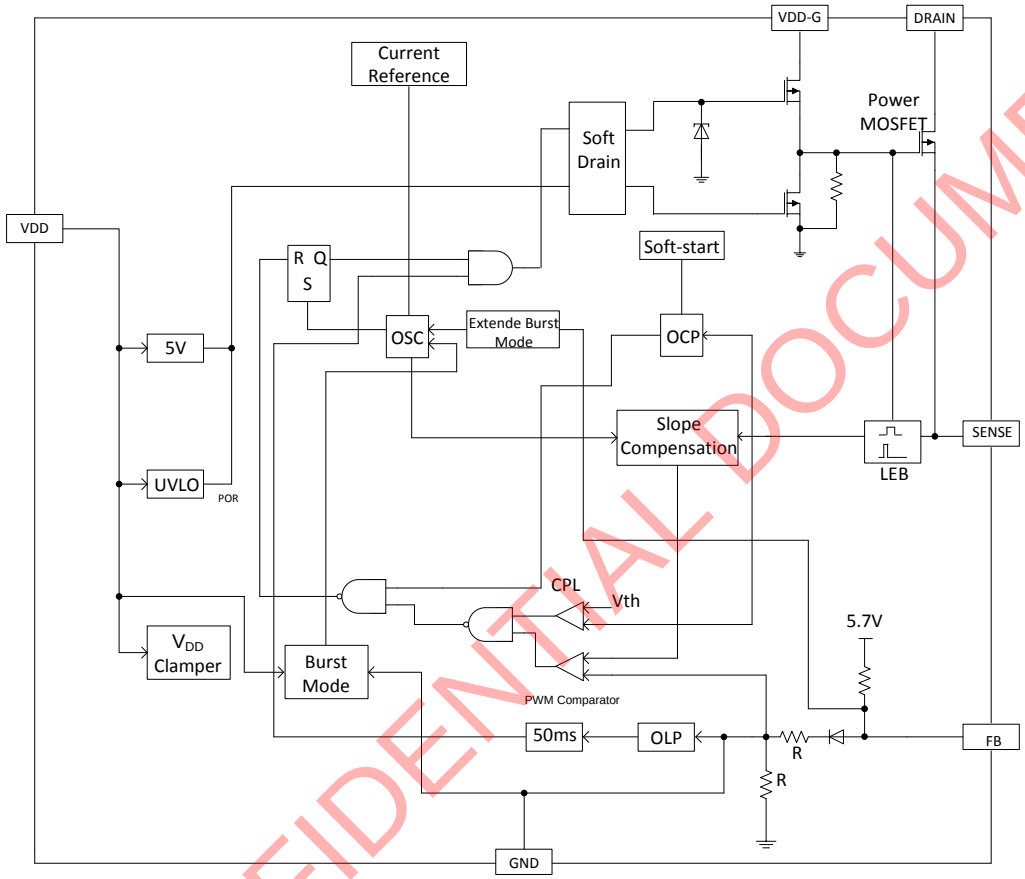
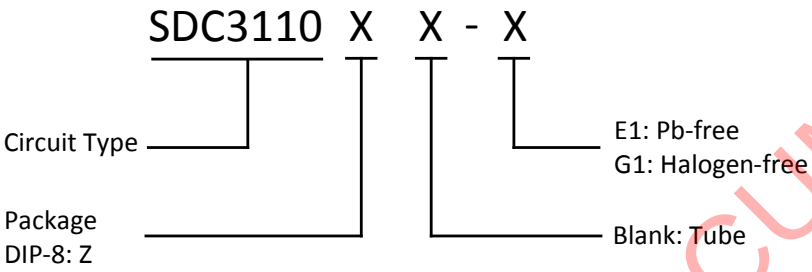


Figure 3. Functional Block Diagram

Ordering Information



Package	Temperature Range	Part Number		Marking ID		Packing Type
		Pb-free	Halogen-free	Pb-free	Halogen-free	
DIP-8	-40℃~85℃	SDC3110Z -E1	SDC3110Z -G1	SDC3110	SDC3110G	Tube

Output Power Table

Product	230VAC±15%		85-265VAC	
	Adopter	Open Frame	Adopter	Open Frame
SDC3110	20W	27W	12W	18W

Table 2. Output Power

Absolute Maximum Ratings (NOTE: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device.)

Parameter	Symbol	Value	Unit
DRAIN voltage (off state)	Bvdss	-0.3~600	V
VDD voltage	V_{dd}	-0.3~30	V
VDD-G input voltage	V_{dd-G}	-0.3~30	V
VDD clamp continuous current	$I_{VDD-Clamp}$	10	mA
FB input voltage	V_{FB}	-0.3~7	V
Sense input voltage	V_{SENSE}	-0.3~7	V
Operating junction temperature T_J	T_{JMAX}	150	°C
Storage temperature T_{STG}	T_{STG}	-55~150	°C
Lead temperature (soldering,10s)	T_{LEAD}	260	°C
Latch-up test per JEDEC 78	-	200	mA
ESD,HBM model per Mil-Std-883H,Method 3015	HBM	2000	V
ESD,MM model per JEDEC EIA/JESD22-A115	MM	200	V

Table 3. Absolute Maximum Ratings

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
DRAIN voltage (off state)	B_{Vdss}	-	600	V
VDD voltage	V_{DD}	10	25	V
Maximum Operating Frequency	f_{osc}		50	KHz
Operating Temperature Range	T_{OP}	-40	85	℃

Table 4. Recommended Operating Conditions

Electrical Characteristics (Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (V_{DD})						
VDD start up current	$I_{STARTUP}$	V_{DD}=14.5V, Measure Leakage current into V_{DD}	-	5	20	uA
Operation current	I_{VDD}	V_{FB}=3V	-	1.6	-	mA
VDD under voltage lockout enter	$V_{UVLO(ON)}$	-	8.7	9.7	10.7	V
VDD under voltage lockout exit (recovery)	$V_{UVLO(OFF)}$	-	14.6	15.8	17.0	V
Over voltage protection voltage	$V_{OVP(ON)}$	CS=0V, FB=3V Ramp up V_{DD} until gate clock is off	27.0	28.5	30.0	V
VDD zener clamp voltage	V_{DD_CLAMP}	I_{DD} = 10 mA		30.0		V
Feedback Input Section(FB Pin)						
VFB open loop voltage	V_{FB_OPEN}	-	5.4	5.7	6.0	V
FB pin short circuit current	I_{FB_SHORT}	Short FB pin to GND and measure current	-	1.45	-	mA
Zero duty cycle FB threshold voltage	V_{TH_0D}	-	-	0.8	-	V
Power limiting fb threshold voltage	V_{TH_PL}	-	-	3.7	-	V
Power limiting debounce time	t_{D_PL}	-	-	50	-	ms
Input impedance	Z_{FB_IN}	-	-	4	-	kΩ
Current Sense Input(Sense Pin)						
Soft start time	t_{SS}	-	-	4	-	ms
Leading edge blanking time	$t_{BLANKING}$	-	-	270	-	ns
Input impedance	Z_{SENSE_IN}	-	-	40	-	kΩ
Over current detection and control delay	t_{D_OC}	From Over Current Occurs till the Gate drive output start to turn off	-	120	-	ns
Internal current limiting threshold voltage	V_{TH_OC}	FB=3.3V	0.72	0.77	0.82	V
Oscillator						

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Normal oscillation frequency	f_{OSC}	-	45	50	55	kHz
Frequency temperature stability	Δf_{Temp}	-	-	5	-	%
Frequency voltage stability	Δf_{VDD}	-	-	5	-	%
Maximum duty cycle	D_{max}	FB=3.3V, CS =0V	70	80	90	%
Burst mode base frequency	f_{BM}	-	-	22	-	kHz
Mosfet Section						
MOSFET DRAIN-source breakdown voltage	B_{Vdss}	V_{GS}=0V, I_D=250uA	600	-	-	V
Static DRAIN to source on resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=1. 0A	-	-	3.3	Ω
Drain to source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V			1	uA
Frequency Shuffling						
Modulation range /Base frequency	Δf_{OSC}	-	-4	-	4	%

Table 5. Electrical Characteristics

Typical Performance Characteristics

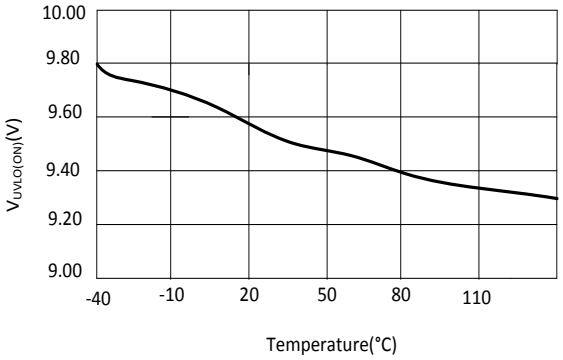


Figure 4. $V_{UVLO(ON)}$(V) vs. Temperature(°C)

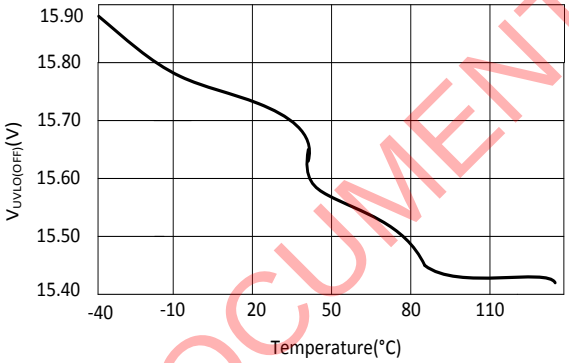


Figure 5. $V_{UVLO(OFF)}$ vs. Temperature(°C)

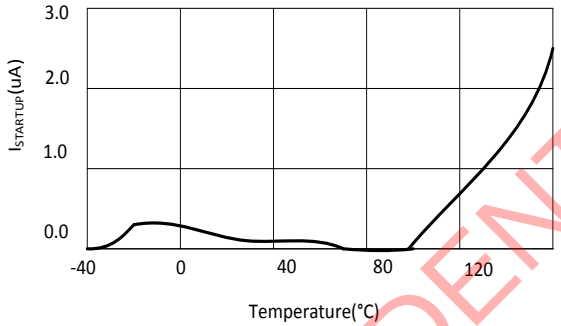


Figure 6. $I_{STARTUP}$(uA) vs. Temperature(°C)

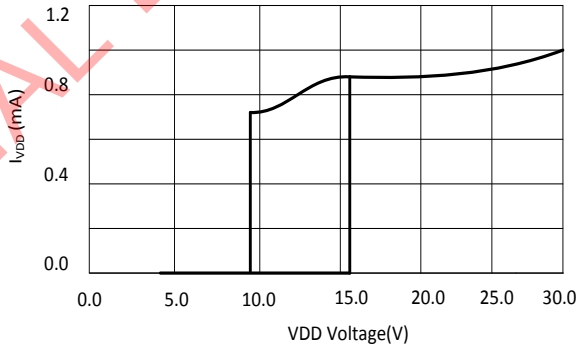


Figure 7. VDD Voltage(V) vs. I_{VDD}(mA)

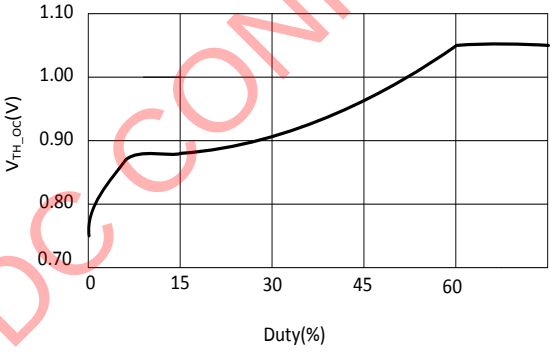


Figure 8. V_{TH_OC}(V) vs. Duty(%)

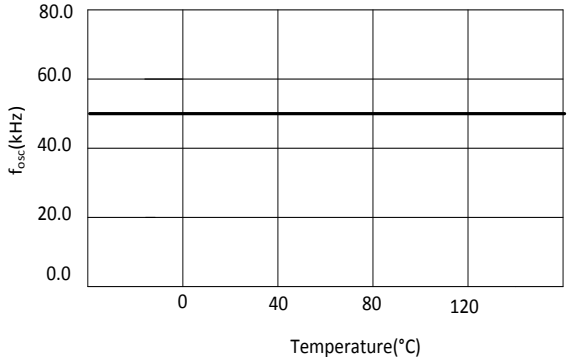


Figure 9. f_{osc}(kHz) vs. Temperature(°C)

Operation Description

The SDC3110 is a low power off-line SMPS switcher optimized for off-line flyback converter applications in sub 27W power range. The extended burst mode control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of SDC3110 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application. For AC/DC adaptor with universal input range design, a 2 MΩ, 1/ 8 W startup resistor could be used together with a VDD capacitor to provide a fast start-up and yet low power dissipation design solution.

Operating Current

The Operating current of SDC3110 is low at 2mA. Good efficiency is achieved with SDC3110 low operating current together with the extended burst mode control features.

Soft Start

SDC3110 features an internal 4ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the peak current is gradually increased from nearly zero to the maximum level of 0.77V. Every restart up is followed by a soft start.

Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in SDC3110. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold level and device enters burst mode control. The gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

The switching frequency of SDC3110 is internally fixed at 50kHz. No external frequency setting components are required for PCB design simplification.

Current Sensing and Leading Edge Blanking

Cycle-by-cycle current limiting is offered in SDC3110 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of internal power MOSFET so that the external RC filtering on sense input is no longer needed.

The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Gate Drive

The internal power MOSFET in SDC3110 is driven by a dedicated gate driver for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive results the compromise of EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. In addition to the gate drive control scheme mentioned, the gate drive strength can also be adjusted externally by a resistor connected between VDD and VDDG, the falling edge of the DRAIN output can be well controlled. It provides great flexibility for system EMI design.

Protection Controls

Good power supply system reliability is achieved with its rich protection features including cycle-by-cycle current limiting (OCP), over load protection (OLP) and over voltage clamp, under voltage lockout on VDD (UVLO). the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the switcher. Switcher restarts when VDD voltage drops below UVLO limit.

VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than 30V. The output of SDC3110 is shut down when VDD drops below UVLO_ON limit and switcher enters power on start-up sequence thereafter.

Typical Application

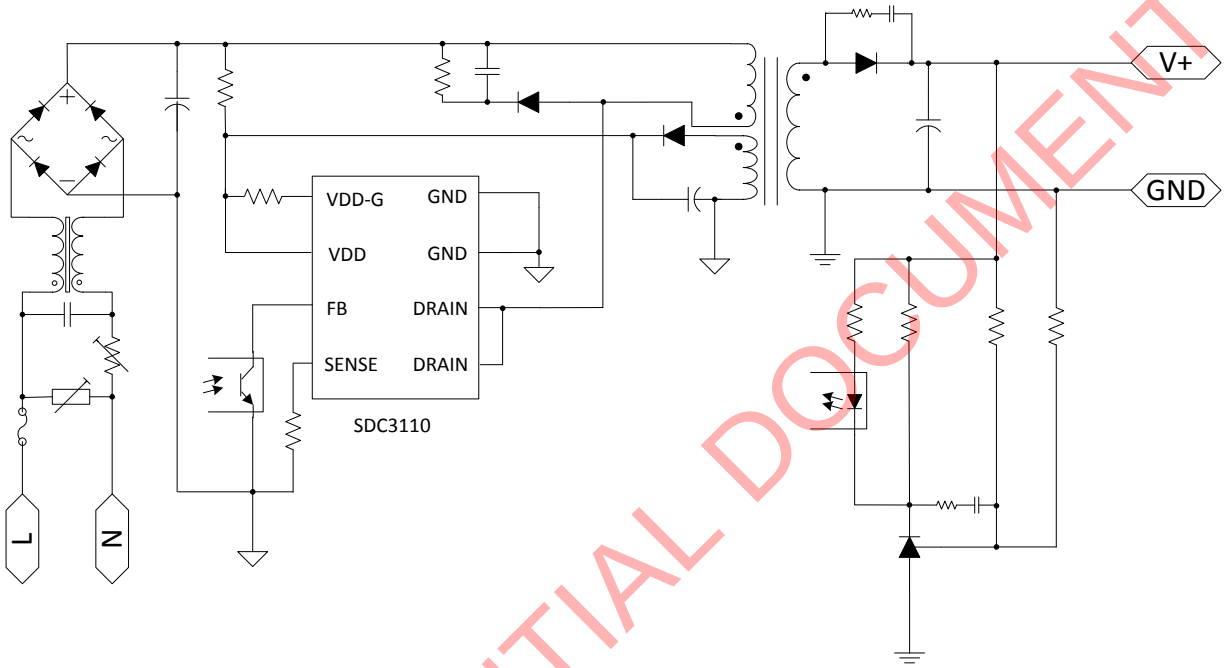
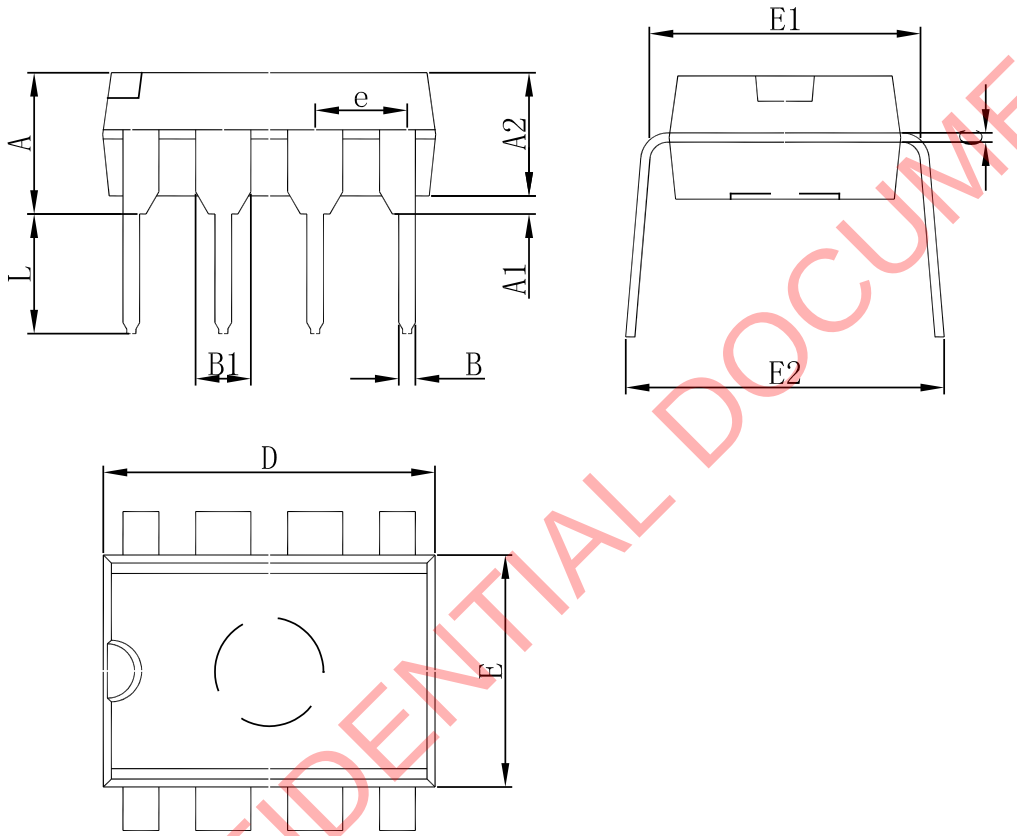


Figure 10. Typical Application

Package Information

DIP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

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