

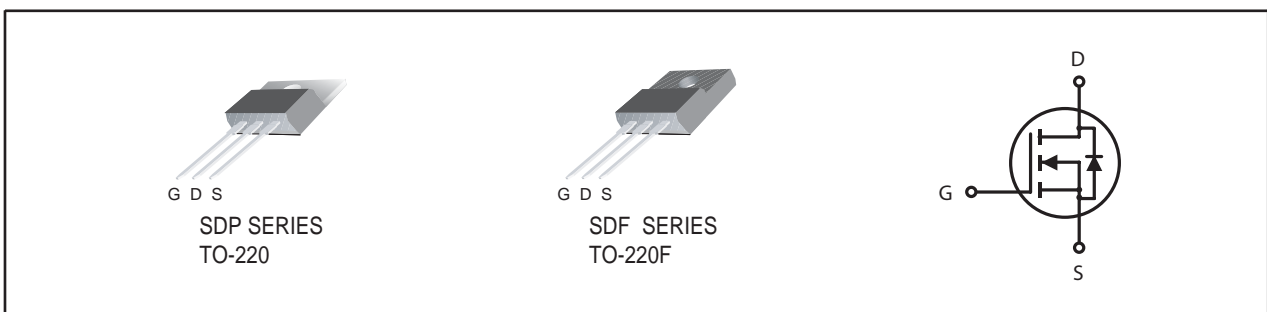


## N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (Ω) Max
650V	2A	5.6 @ V <sub>GS</sub> =10V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- TO-220 and TO-220F Package.



### ORDERING INFORMATION

Ordering Code	Package	Marking Code	Delivery Mode	RoHS Status
SDP02N65HZ	TO-220	SDP02N65	Tube	Halogen Free
SDP02N65PZ	TO-220	02N65	Tube	Pb Free
SDF02N65HZ	TO-220F	SDF02N65	Tube	Halogen Free
SDF02N65PZ	TO-220F	02N65	Tube	Pb Free

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	SDP02N65	SDF02N65	Units
V <sub>DS</sub>	Drain-Source Voltage	650		V
V <sub>GS</sub>	Gate-Source Voltage	±30	±30	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>C</sub> =25°C	2	A
		T <sub>C</sub> =100°C	1.4	A
I <sub>DM</sub>	-Pulsed <sup>a</sup>	5.9	5.9	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>c</sup>	56		mJ
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> =25°C	75	W
		T <sub>C</sub> =100°C	37.5	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 175		°C

### THERMAL CHARACTERISTICS

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	2	6	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

# SDP02N65

## SDF02N65

Ver 2.1

### ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	650			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =520V, V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±30V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2	3	4	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =1A		4.4	5.6	ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =20V, I <sub>D</sub> =1A		1.7		S
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		302		pF
C <sub>oss</sub>	Output Capacitance			37		pF
C <sub>rSS</sub>	Reverse Transfer Capacitance			10		pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =325V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> = 6 ohm		15.2		ns
t <sub>r</sub>	Rise Time			16.4		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			17		ns
t <sub>f</sub>	Fall Time			9.6		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =325V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V		5		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =325V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V		1.4		nC
Q <sub>gd</sub>	Gate-Drain Charge			2.2		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =1A		0.8	1.4	V

#### Notes

- a. Drain current limited by maximum junction temperature.  
 b. Guaranteed by design, not subject to production testing.  
 c. Starting T<sub>J</sub>=25°C, L=50mH, V<sub>DD</sub> = 50V. (See Figure 12)

Dec, 24, 2013

# SDP02N65

## SDF02N65

Ver 2.1

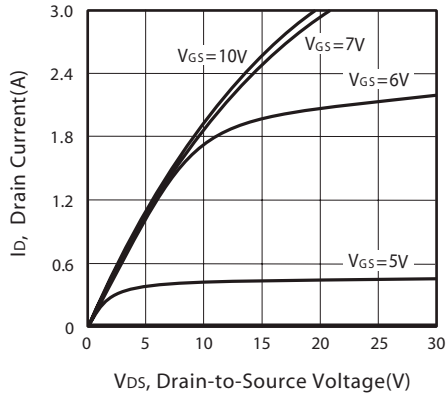


Figure 1. Output Characteristics

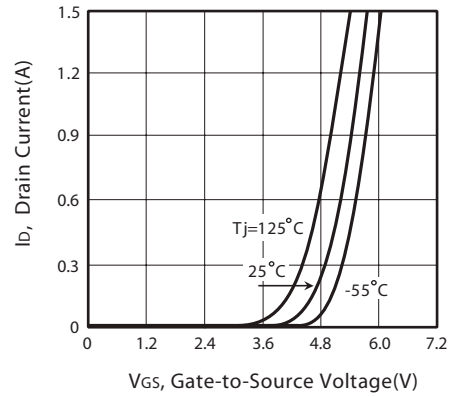


Figure 2. Transfer Characteristics

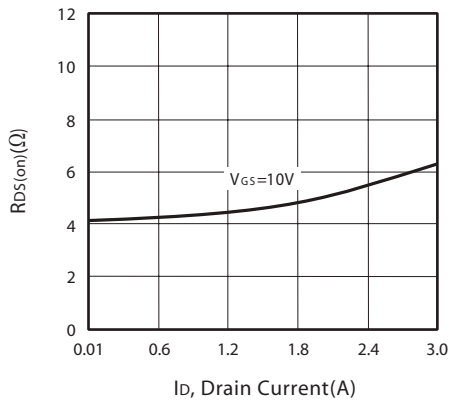


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

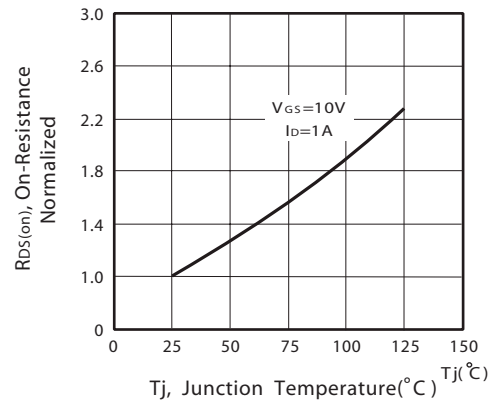


Figure 4. On-Resistance Variation with Drain Current and Temperature

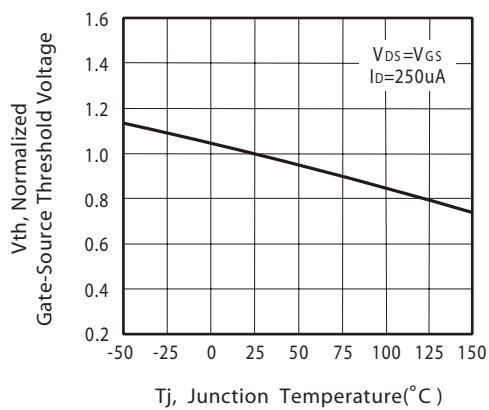


Figure 5. Gate Threshold Variation with Temperature

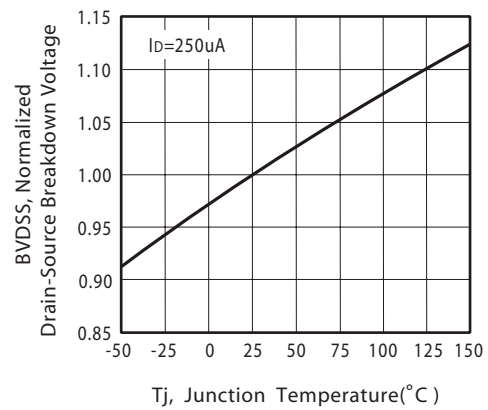


Figure 6. Breakdown Voltage Variation with Temperature

Dec,24,2013

# SDP02N65

## SDF02N65

Ver 2.1

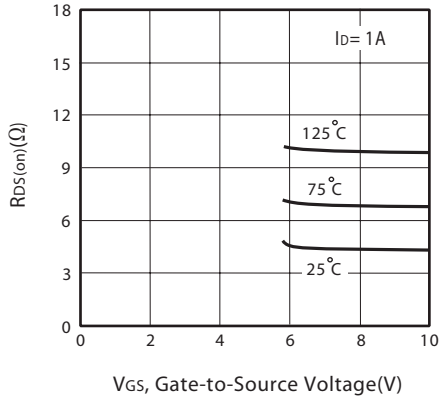


Figure 7. On-Resistance vs. Gate-Source Voltage

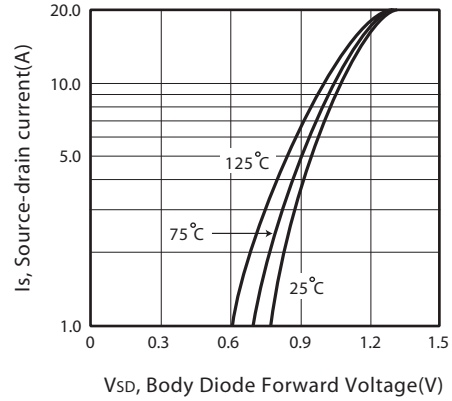


Figure 8. Body Diode Forward Voltage Variation with Source Current

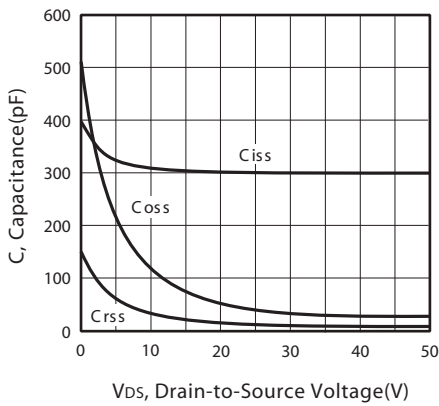


Figure 9. Capacitance

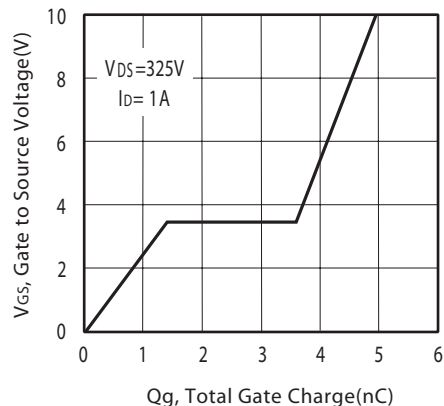


Figure 10. Gate Charge

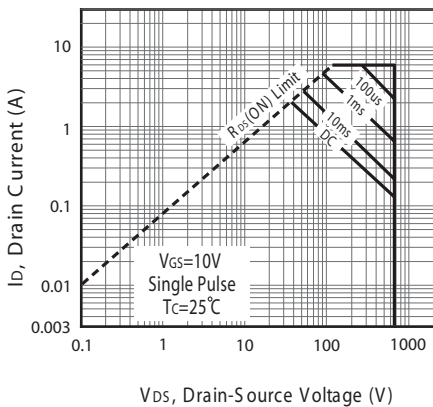


Figure 11a. Maximum Safe Operating Area for SDP02N65

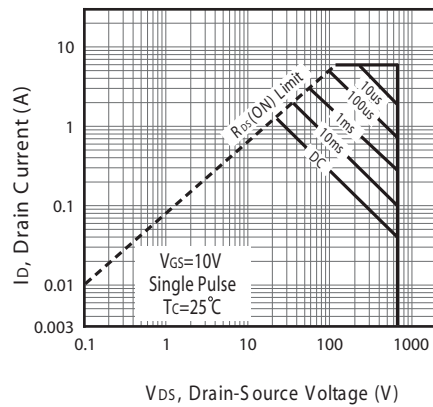


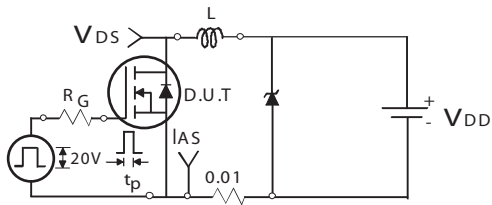
Figure 11b. Maximum Safe Operating Area for SDF02N65

Dec.24,2013

# SDP02N65

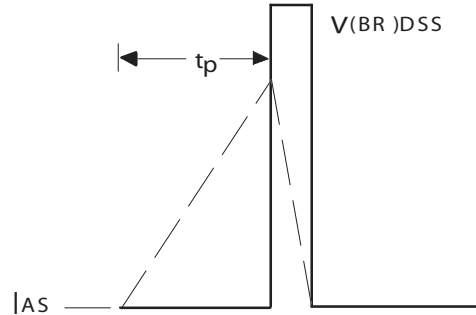
## SDF02N65

Ver 2.1



Unclamped Inductive Test Circuit

Figure 12a.



Unclamped Inductive Waveforms

Figure 12b.

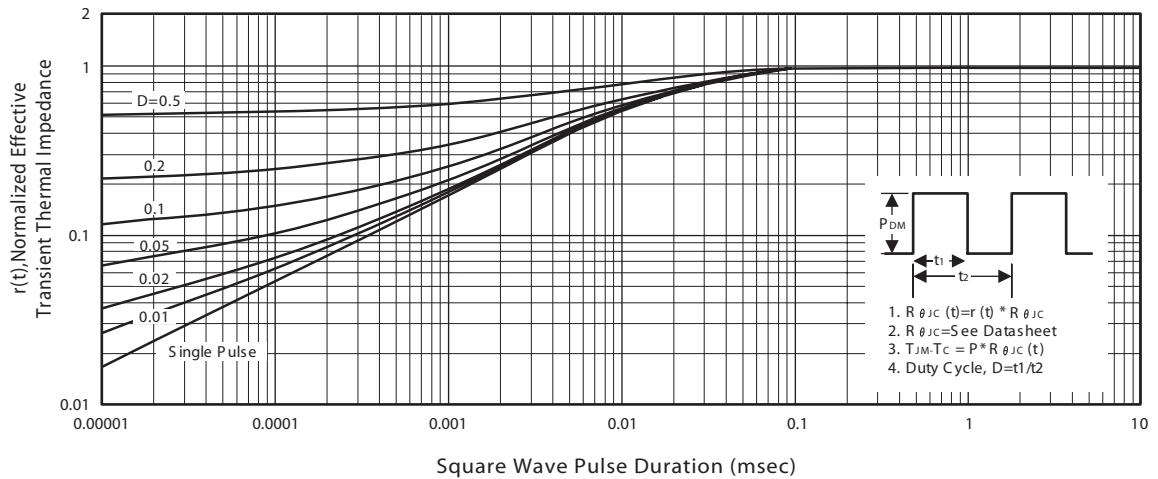


Figure 13a. Normalized Thermal Transient Impedance Curve for SDP02N65

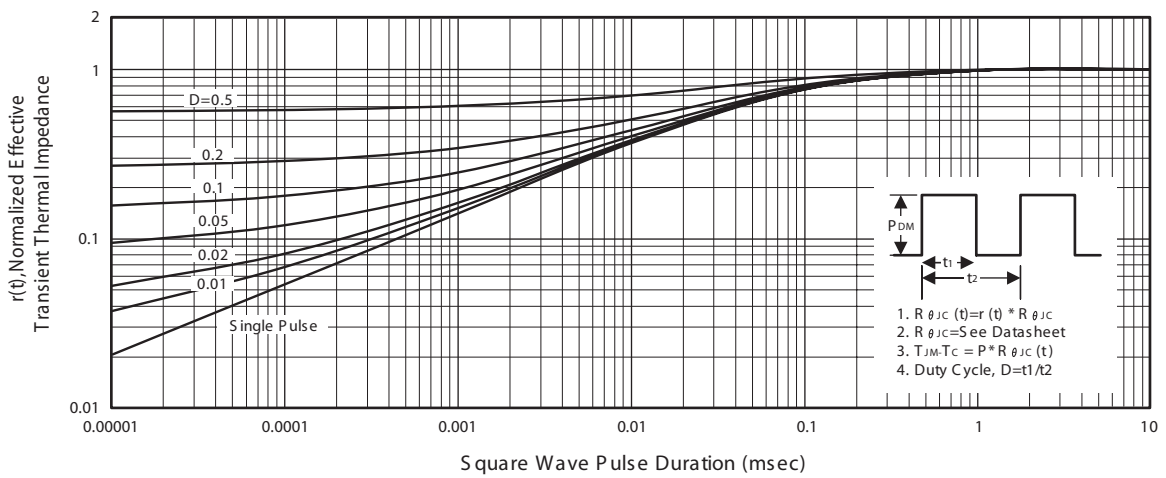


Figure 13b. Normalized Thermal Transient Impedance Curve for SDF02N65

Dec,24,2013

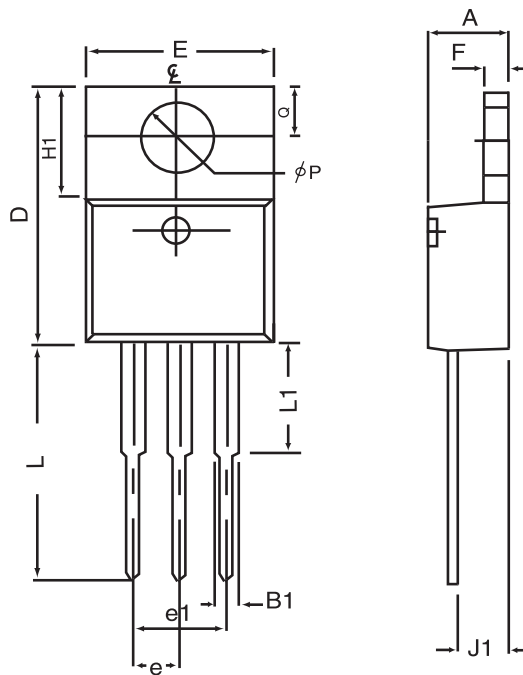
# SDP02N65

## SDF02N65

Ver 2.1

### PACKAGE OUTLINE DIMENSIONS

TO-220



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.80	0.170	0.189
B1	1.27	1.65	0.050	0.630
D	14.6	16.00	0.575	0.610
E	9.70	10.41	0.382	0.410
e	2.34	2.74	0.092	0.108
e1	4.68	5.48	0.184	0.216
F	1.14	1.40	0.045	0.055
H1	5.97	6.73	0.235	0.265
J1	2.20	2.79	0.087	0.110
L	12.88	14.22	0.507	0.560
L1	3.00	6.35	0.120	0.250
phi P	3.50	3.94	0.138	0.155
Q	2.54	3.05	0.100	0.120

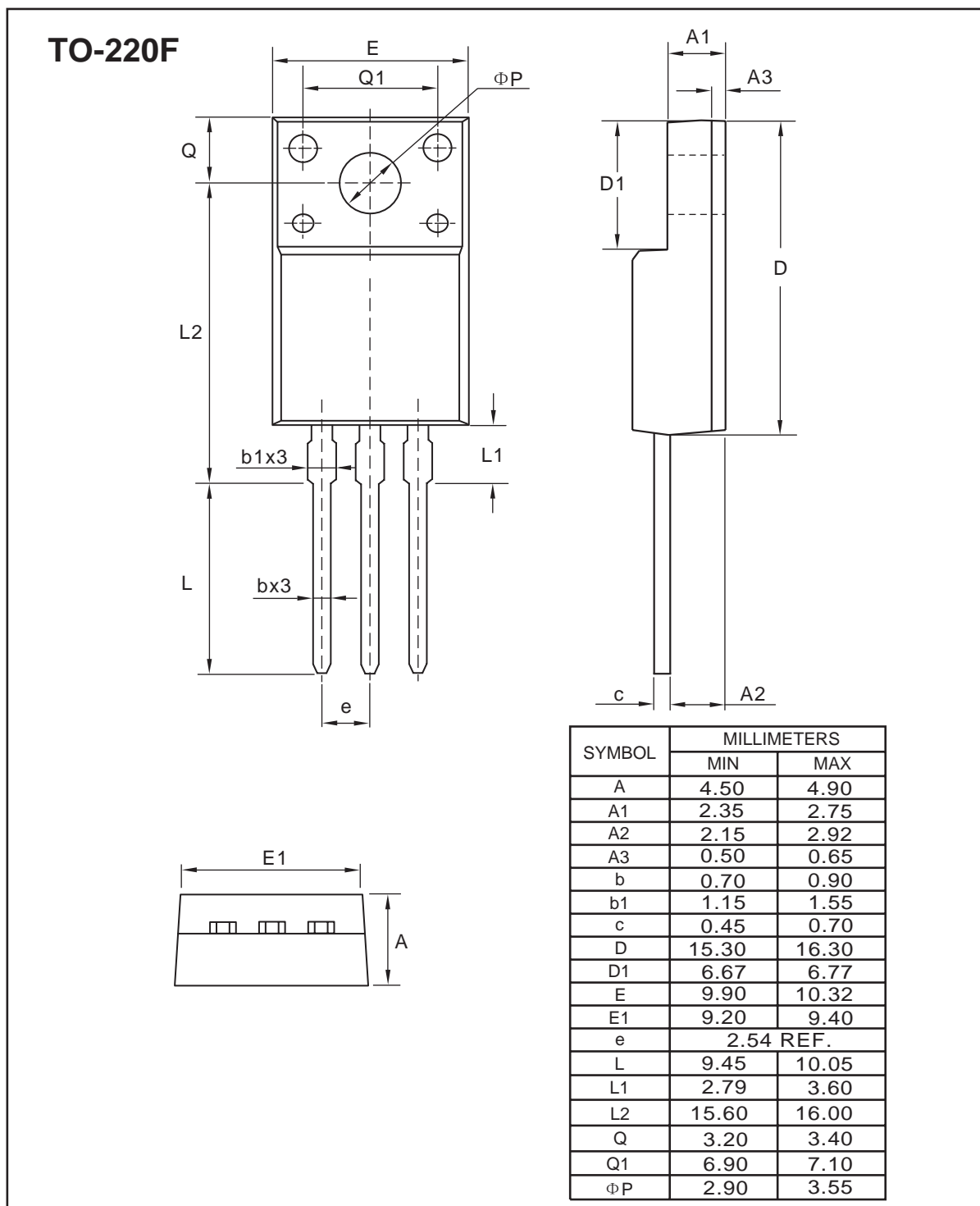
Dec,24,2013

# SDP02N65

## SDF02N65

Ver 2.1

### PACKAGE OUTLINE DIMENSIONS

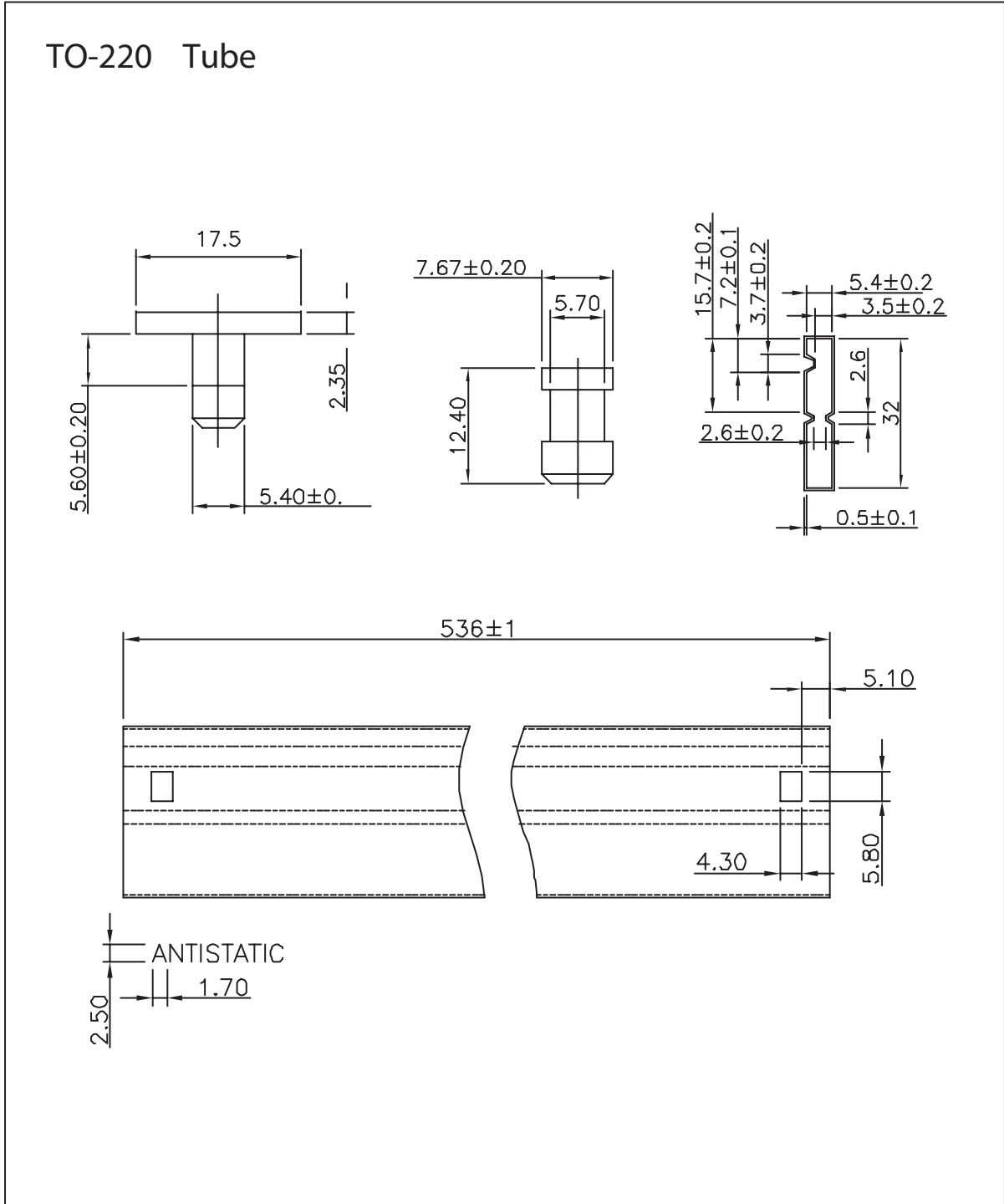


Dec,24,2013

# SDP02N65

## SDF02N65

Ver 2.1



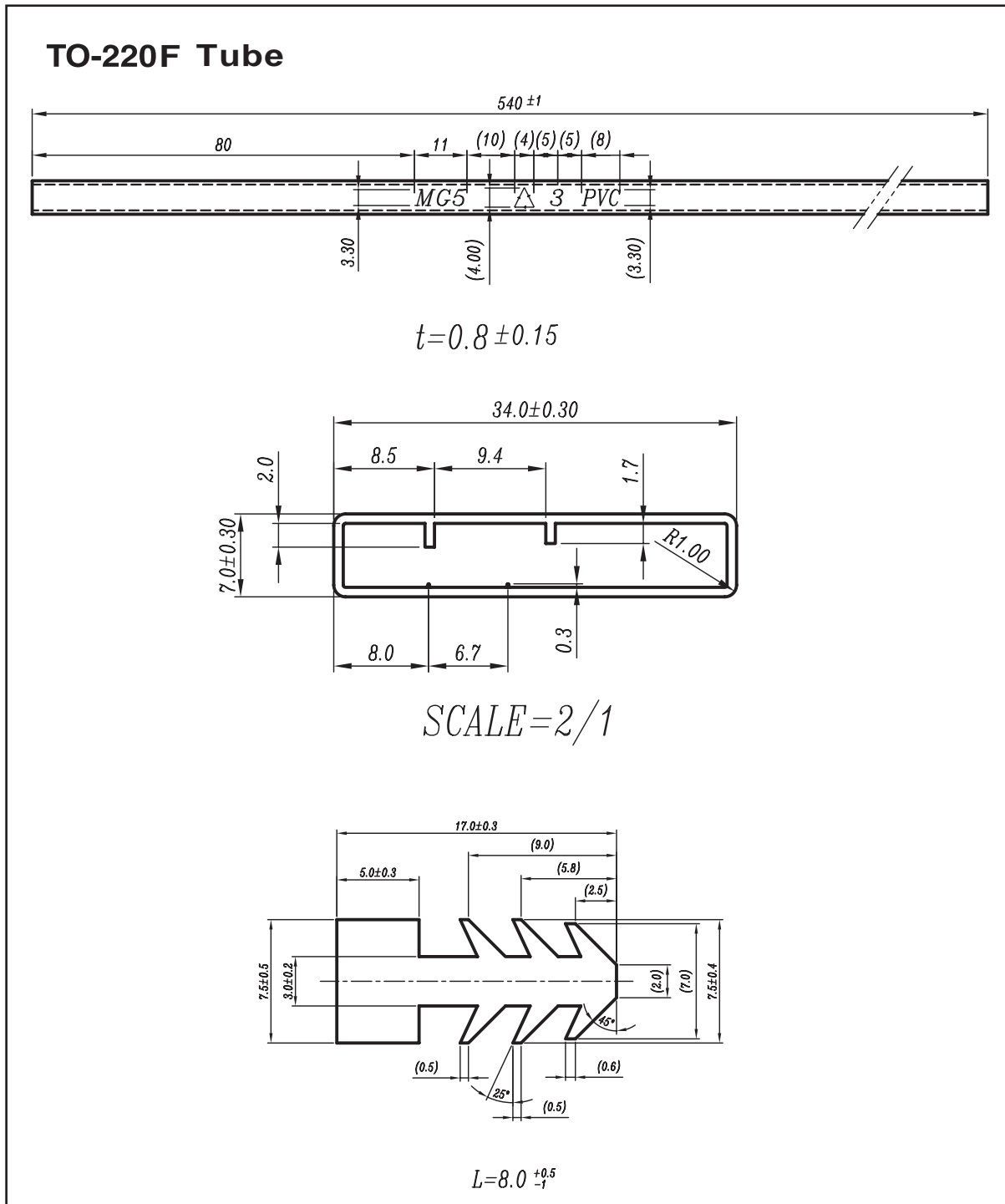
Dec,24,2013



# SDP02N65

## SDF02N65

Ver 2.1



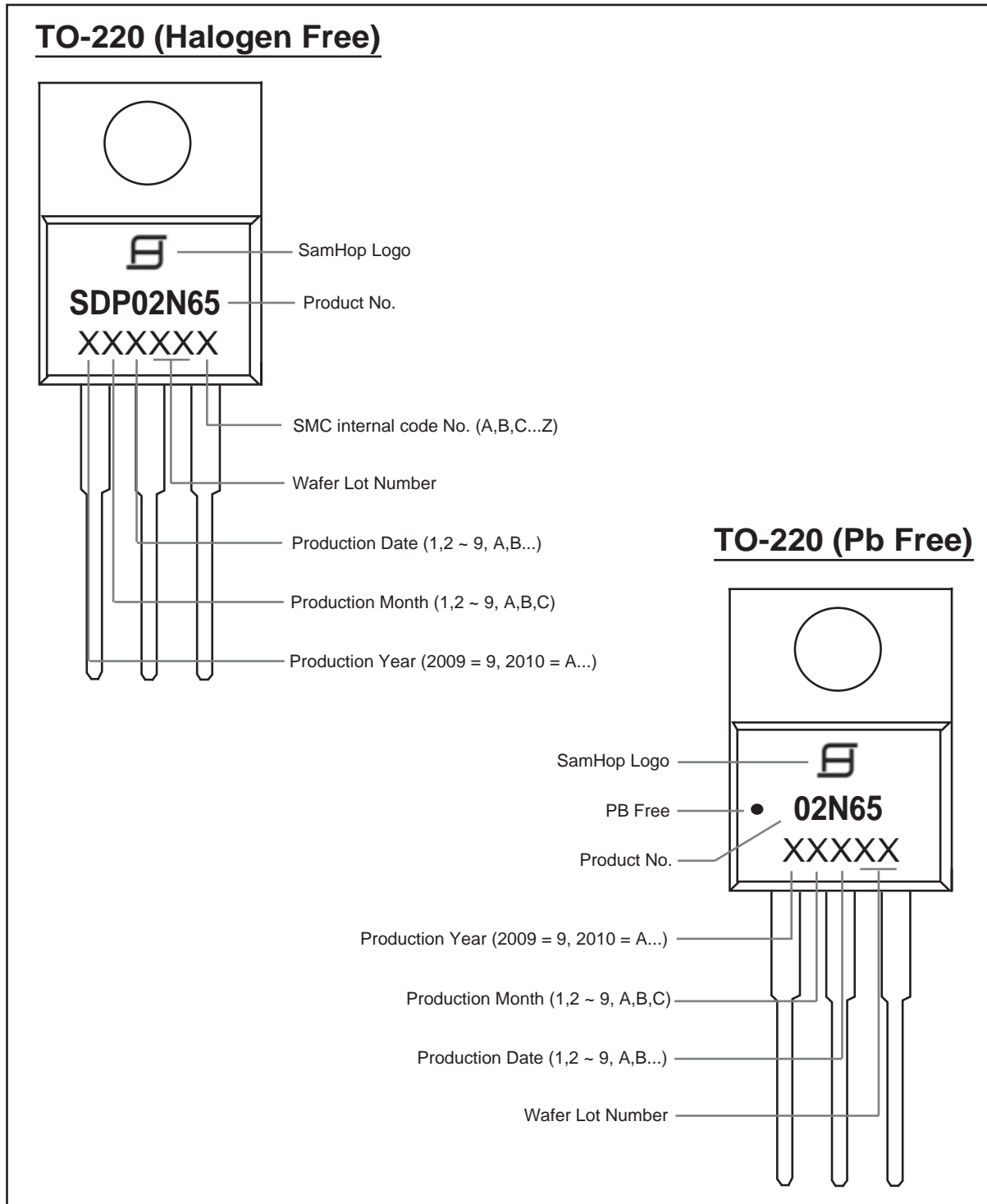
Dec, 24, 2013

# SDP02N65

# SDF02N65

Ver 2.1

## TOP MARKING DEFINITION



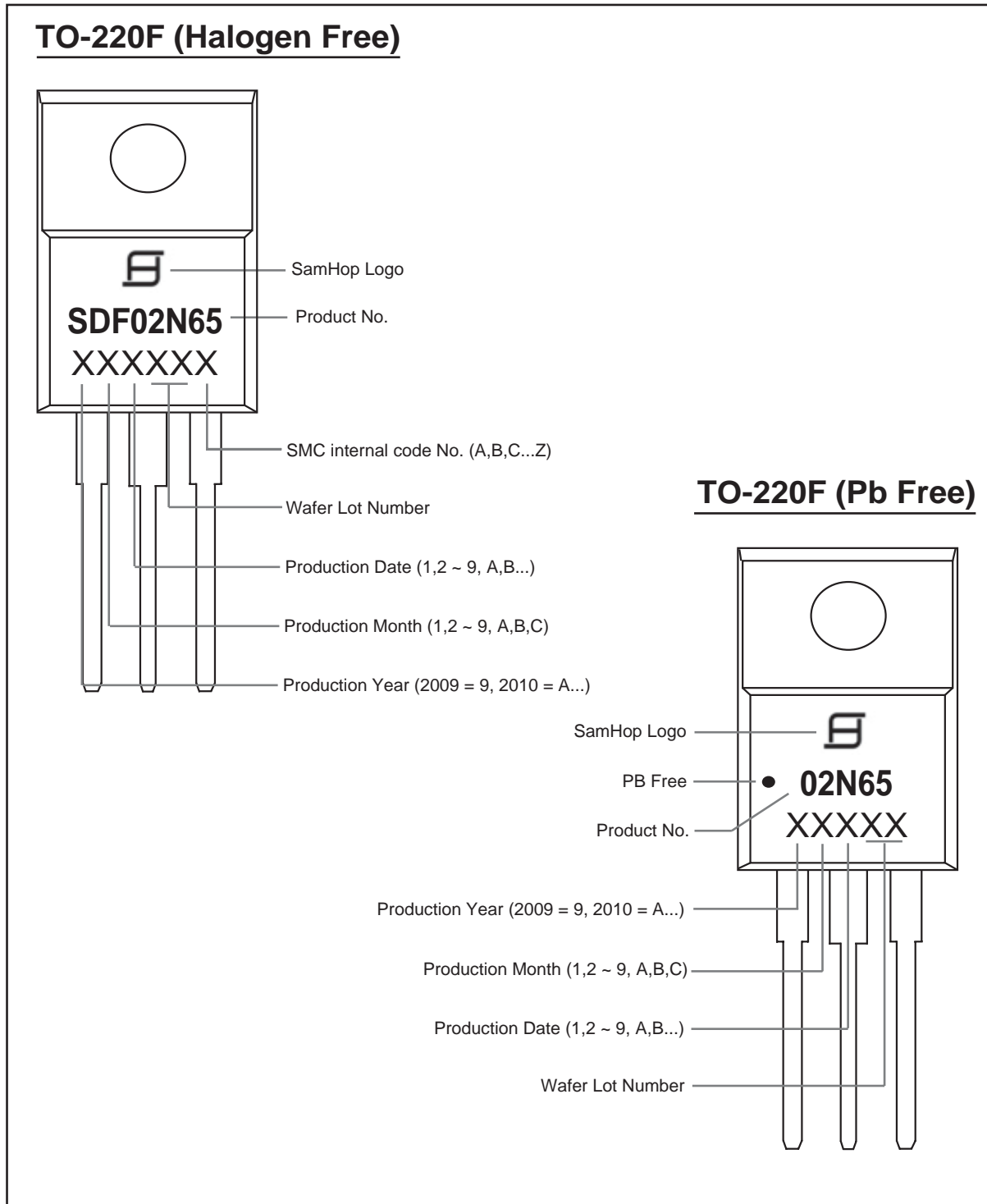
Dec,24,2013

# SDP02N65

# SDF02N65

Ver 2.1

## TOP MARKING DEFINITION



Dec,24,2013