



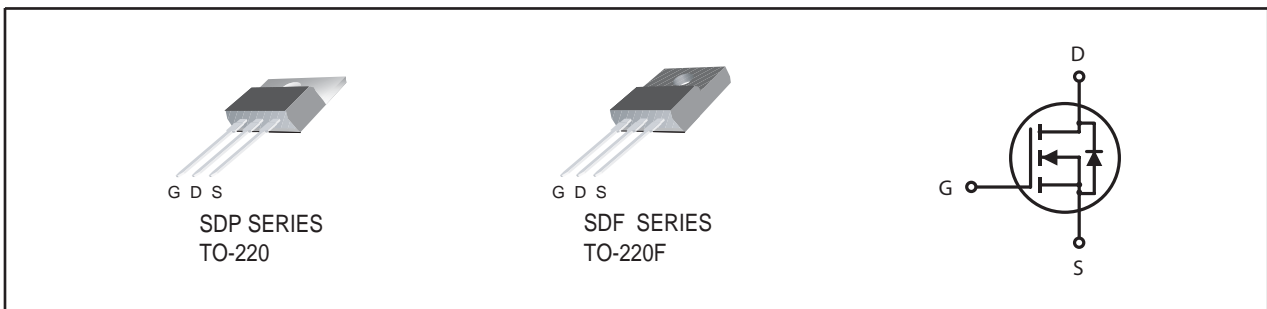
N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY

| V _{DSS} | I _D | R _{DS(ON)} (Ω) Typ |
|------------------|----------------|-----------------------------|
| 800V | 3.0A | 3.3 @ V _{GS} =10V |

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- TO-220 and TO-220F Package.



ORDERING INFORMATION

| Ordering Code | Package | Marking Code | Delivery Mode | RoHS Status |
|---------------|---------|--------------|---------------|--------------|
| SDP03N80HZ | TO-220 | SDP03N80 | Tube | Halogen Free |
| SDP03N80PZ | TO-220 | 03N80 | Tube | Pb Free |
| SDF03N80HZ | TO-220F | SDF03N80 | Tube | Halogen Free |
| SDF03N80PZ | TO-220F | 03N80 | Tube | Pb Free |

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

| Symbol | Parameter | SDP03N80 | SDF03N80 | Units | |
|-----------------------------------|--|----------------------|------------------|------------------|---|
| V _{DS} | Drain-Source Voltage | 800 | | V | |
| V _{GS} | Gate-Source Voltage | ±30 | ±30 | V | |
| I _D | Drain Current-Continuous ^a | T _C =25°C | 3 | 3 ^e | A |
| | | T _C =70°C | 2.5 | 2.5 ^e | A |
| I _{DM} | -Pulsed ^b | 8.9 | 8.9 ^e | A | |
| E _{AS} | Single Pulse Avalanche Energy ^d | 100 | | mJ | |
| P _D | Maximum Power Dissipation ^a | T _C =25°C | 84 | 42 | W |
| | | T _C =70°C | 58 | 29 | W |
| T _J , T _{STG} | Operating Junction and Storage Temperature Range | -55 to 175 | | °C | |

THERMAL CHARACTERISTICS

| | | | | |
|------------------|--|------|------|------|
| R _{θJC} | Thermal Resistance, Junction-to-Case ^a | 1.8 | 3.6 | °C/W |
| R _{θJA} | Thermal Resistance, Junction-to-Ambient ^a | 62.5 | 62.5 | °C/W |

SDP03N80

SDF03N80

Ver 1.1

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|----------------------------------|---|---|------|------|-------|
| OFF CHARACTERISTICS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} =0V , I _D =250uA | 800 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =640V , V _{GS} =0V | | | 1 | uA |
| I _{GSS} | Gate-Body Leakage Current | V _{GS} = ±30V , V _{DS} =0V | | | ±100 | nA |
| ON CHARACTERISTICS | | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250uA | 3 | 4 | 5 | V |
| R _{DS(ON)} | Drain-Source On-State Resistance | V _{GS} =10V , I _D =1.5A | | 3.3 | 4.2 | ohm |
| g _{FS} | Forward Transconductance | V _{DS} =20V , I _D =1.5A | | 2.2 | | S |
| DYNAMIC CHARACTERISTICS ^c | | | | | | |
| C _{ISS} | Input Capacitance | V _{DS} =25V, V _{GS} =0V f=1.0MHz | | 607 | | pF |
| C _{OSS} | Output Capacitance | | | 60 | | pF |
| C _{RSS} | Reverse Transfer Capacitance | | | 12 | | pF |
| SWITCHING CHARACTERISTICS ^c | | | | | | |
| t _{D(ON)} | Turn-On Delay Time | V _{DD} =400V I _D =1A V _{GS} =10V R _{GEN} = 6 ohm | | 27 | | ns |
| t _r | Rise Time | | | 21 | | ns |
| t _{D(OFF)} | Turn-Off Delay Time | | | 30.5 | | ns |
| t _f | Fall Time | | | 14.7 | | ns |
| Q _g | Total Gate Charge | | V _{DS} =400V, I _D =1A, V _{GS} =10V | | 12.5 | |
| Q _{gs} | Gate-Source Charge | V _{DS} =400V, I _D =1A, V _{GS} =10V | | 2.5 | | nC |
| Q _{gd} | Gate-Drain Charge | | | 6 | | nC |
| DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS | | | | | | |
| V _{SD} | Diode Forward Voltage | V _{GS} =0V, I _S =2A | | 0.81 | 1.4 | V |
| Notes | | | | | | |
| <p>a.Surface Mounted on FR4 Board, t ≤ 10sec.</p> <p>b.Pulse Test:Pulse Width ≤ 300us, Duty Cycle ≤ 2%.</p> <p>c.Guaranteed by design, not subject to production testing.</p> <p>d.Starting T_J=25°C, L=50mH, V_{DD} = 50V.(See Figure12)</p> <p>e.Drain current limited by maximum junction temperatruue.</p> | | | | | | |

Dec,24,2013

SDP03N80

SDF03N80

Ver 1.1

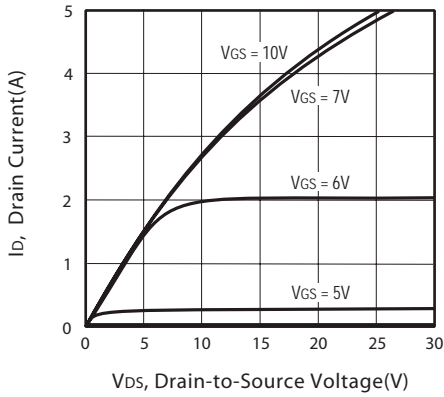


Figure 1. Output Characteristics

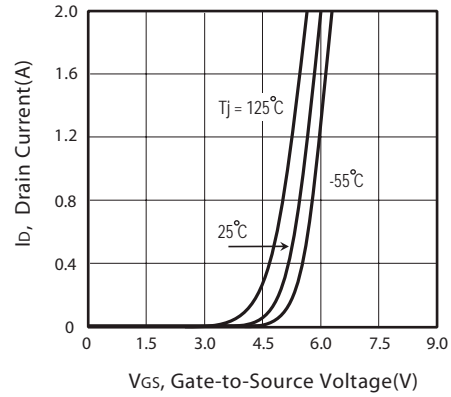


Figure 2. Transfer Characteristics

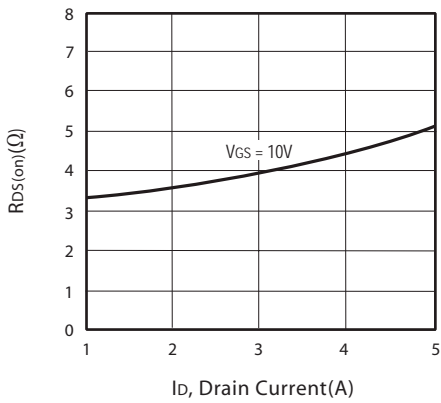


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

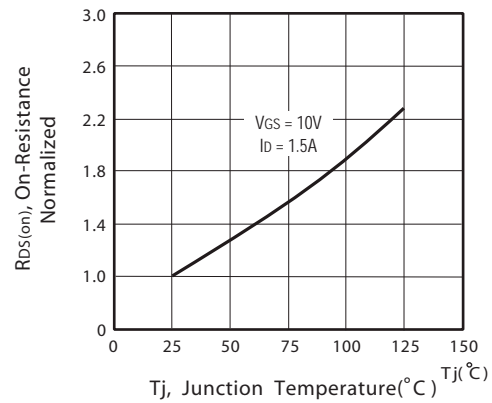


Figure 4. On-Resistance Variation with Drain Current and Temperature

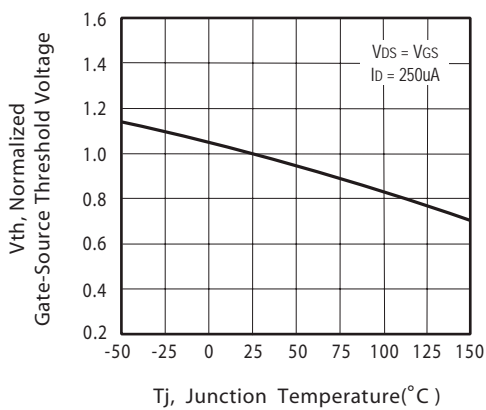


Figure 5. Gate Threshold Variation with Temperature

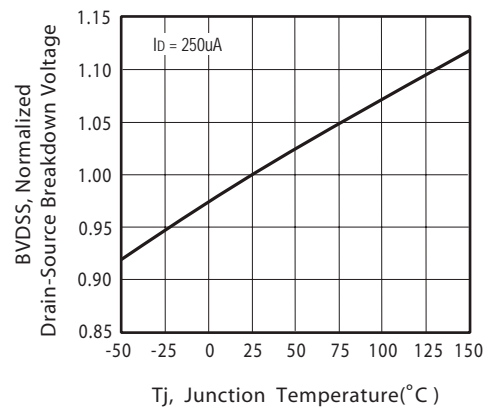


Figure 6. Breakdown Voltage Variation with Temperature

Dec,24,2013

SDP03N80

SDF03N80

Ver 1.1

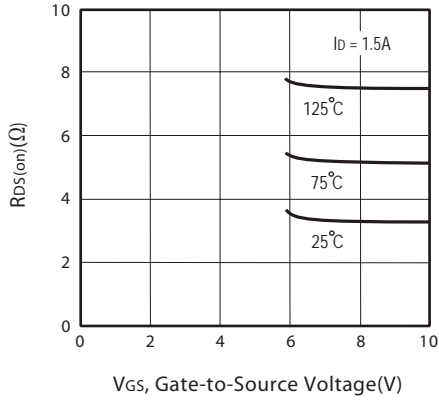


Figure 7. On-Resistance vs. Gate-Source Voltage

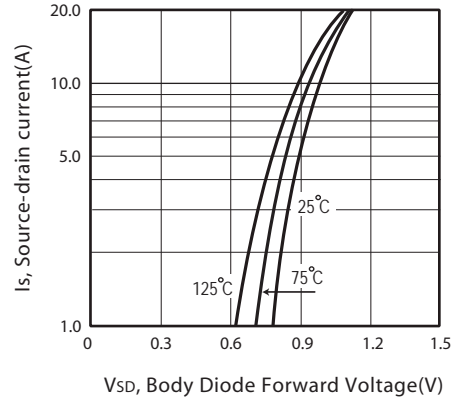


Figure 8. Body Diode Forward Voltage Variation with Source Current

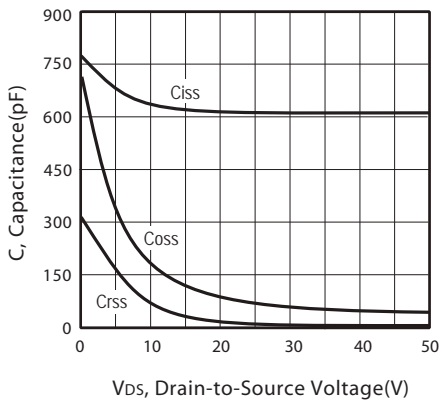


Figure 9. Capacitance

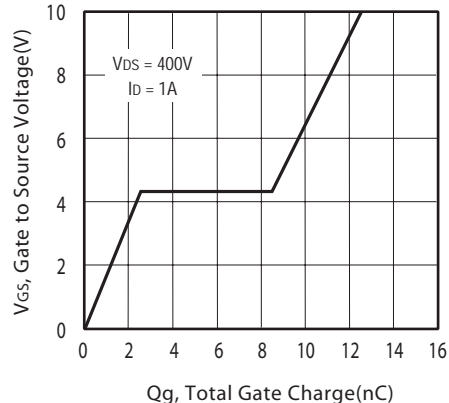


Figure 10. Gate Charge

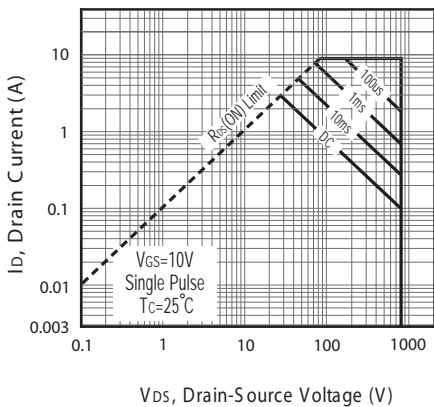


Figure 11a. Maximum Safe Operating Area for SDP03N80

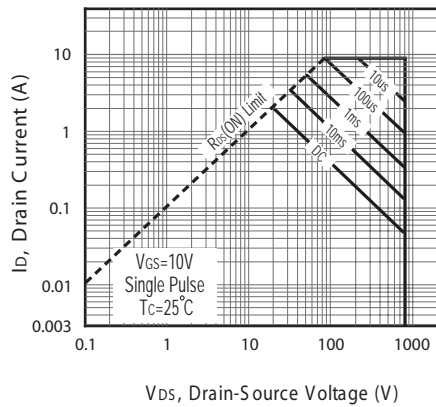


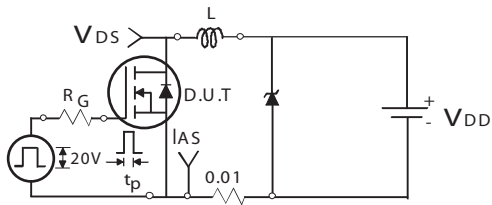
Figure 11b. Maximum Safe Operating Area for SDF03N80

Dec,24,2013

SDP03N80

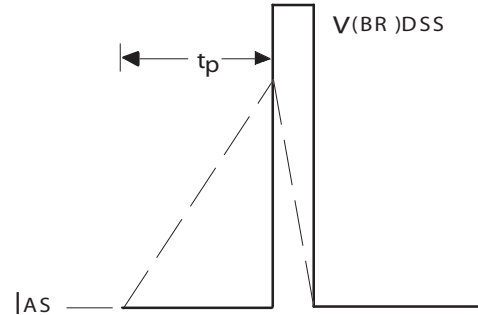
SDF03N80

Ver 1.1



Unclamped Inductive Test Circuit

Figure 12a.



Unclamped Inductive Waveforms

Figure 12b.

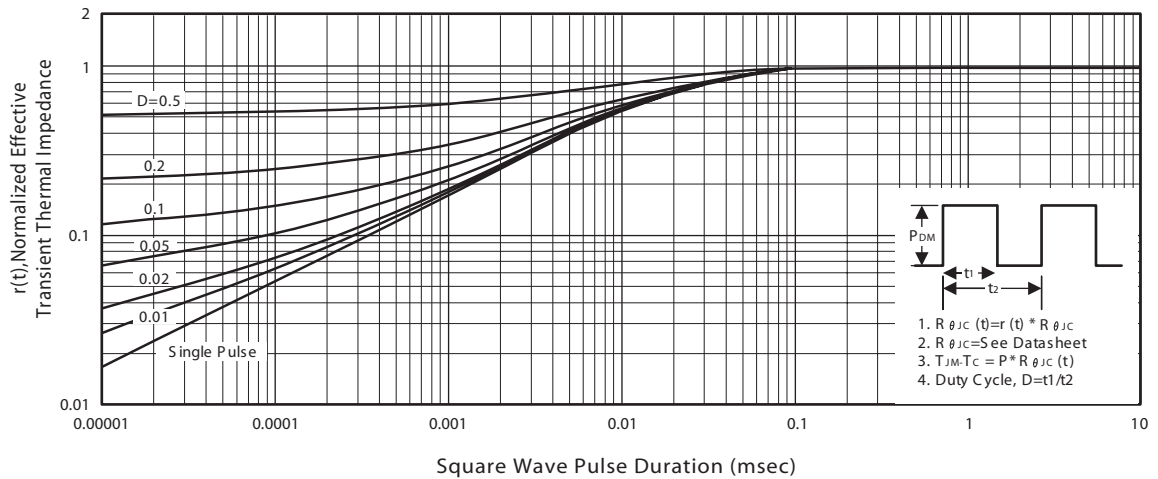


Figure 13a. Normalized Thermal Transient Impedance Curve for SDP03N80

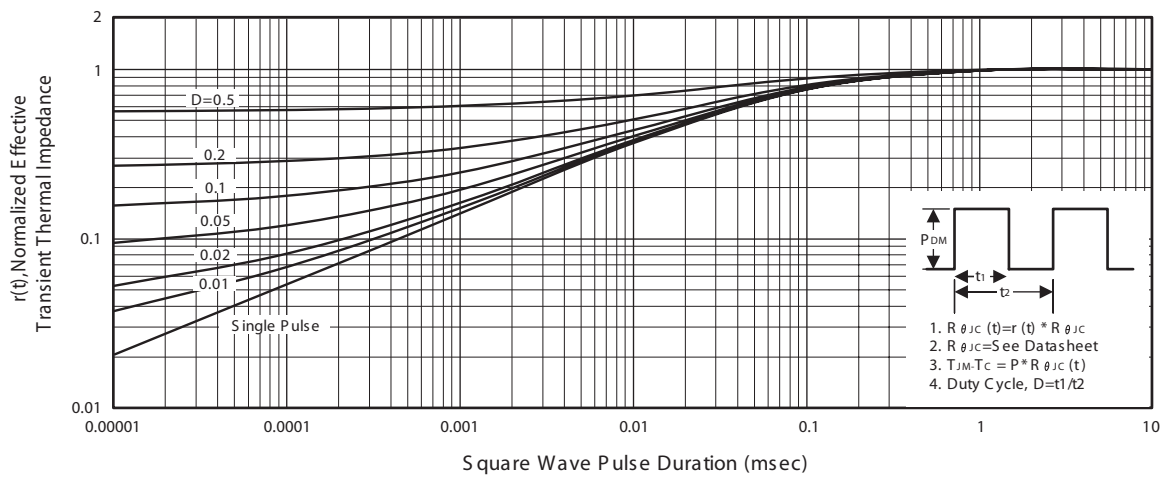


Figure 13b. Normalized Thermal Transient Impedance Curve for SDF03N80

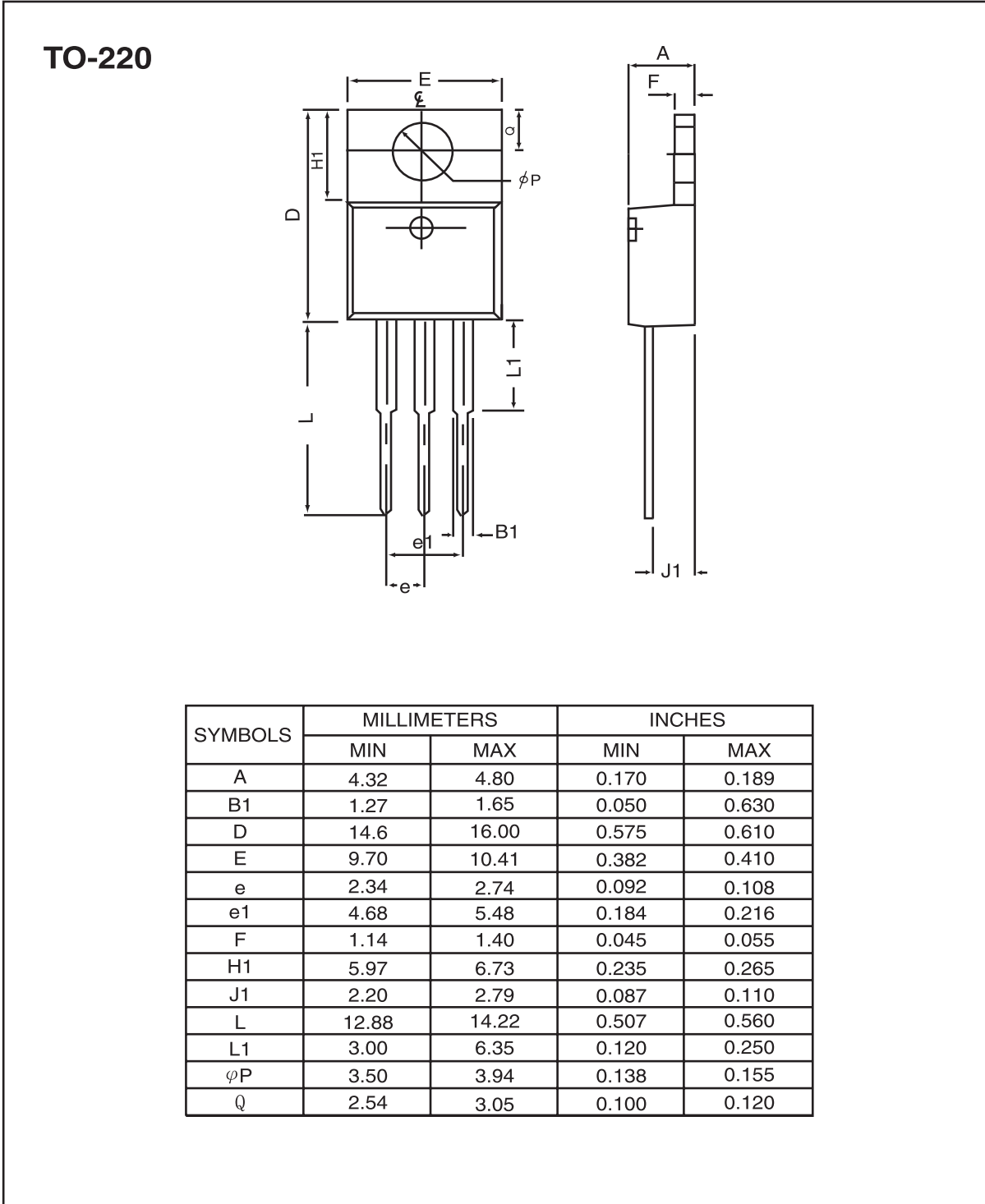
Dec,24,2013

SDP03N80

SDF03N80

Ver 1.1

PACKAGE OUTLINE DIMENSIONS



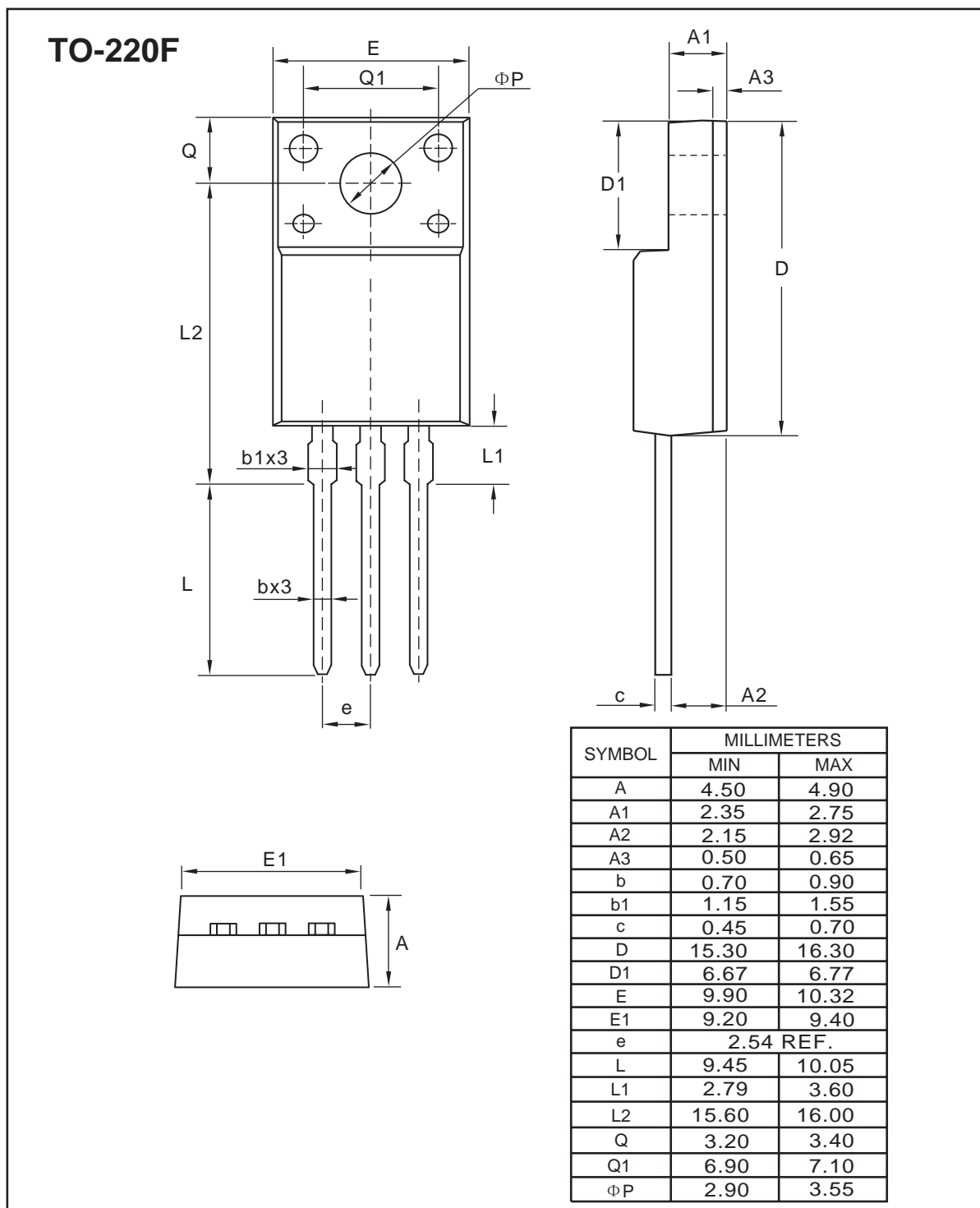
Dec,24,2013

SDP03N80

SDF03N80

Ver 1.1

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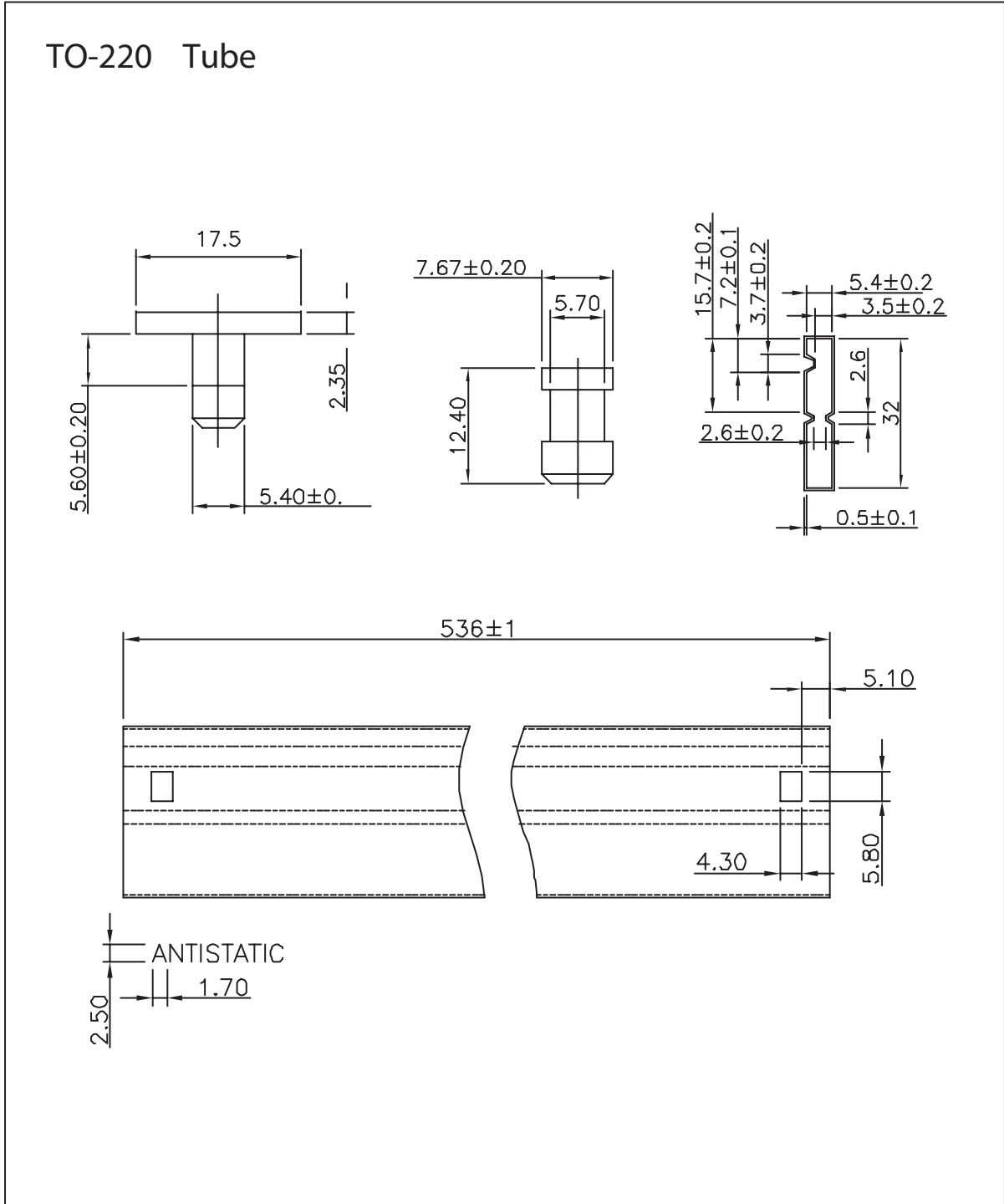


Dec,24,2013

SDP03N80

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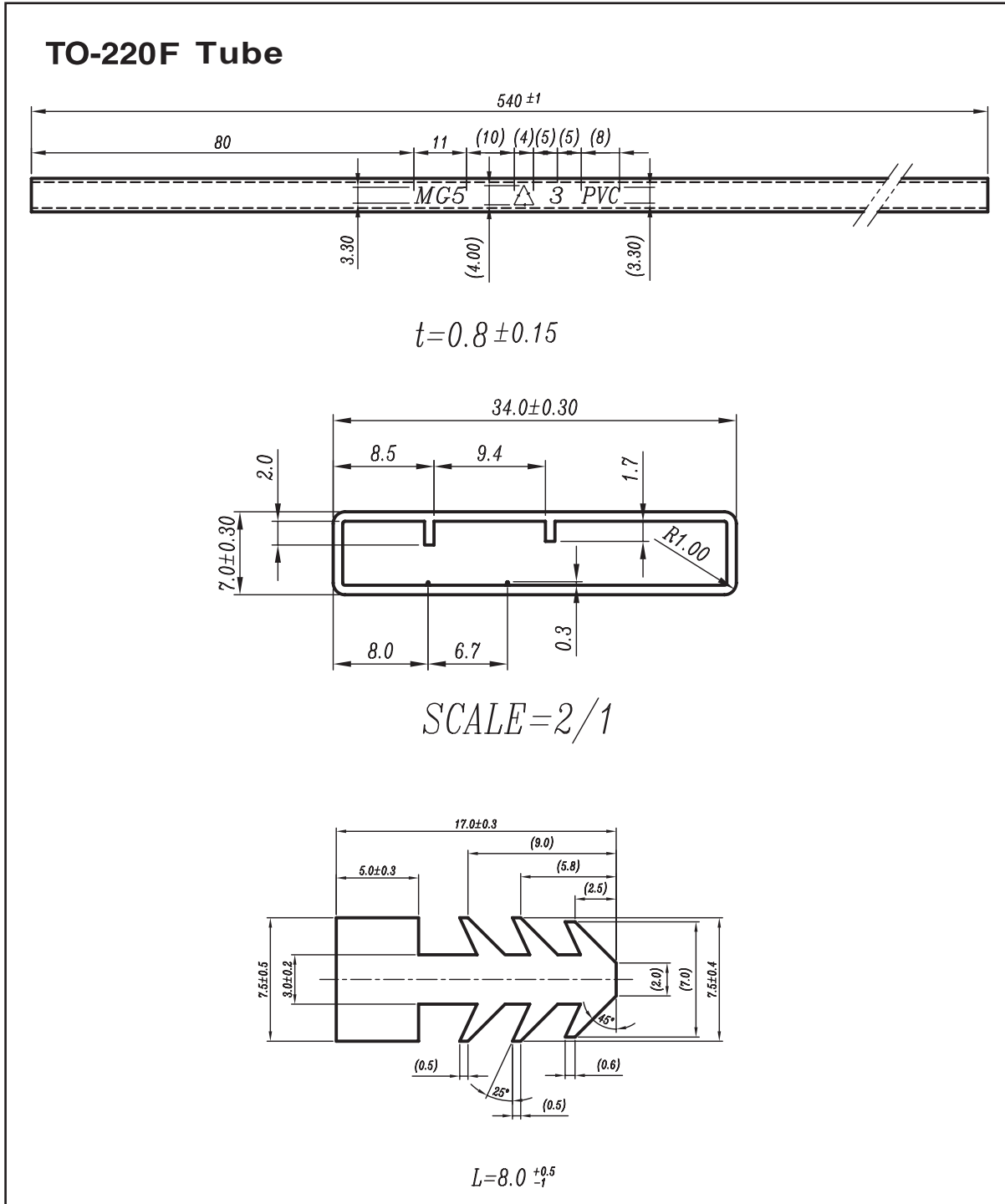
Ver 1.1



Dec,24,2013

SDP03N80
SDF03N80

Ver 1.1



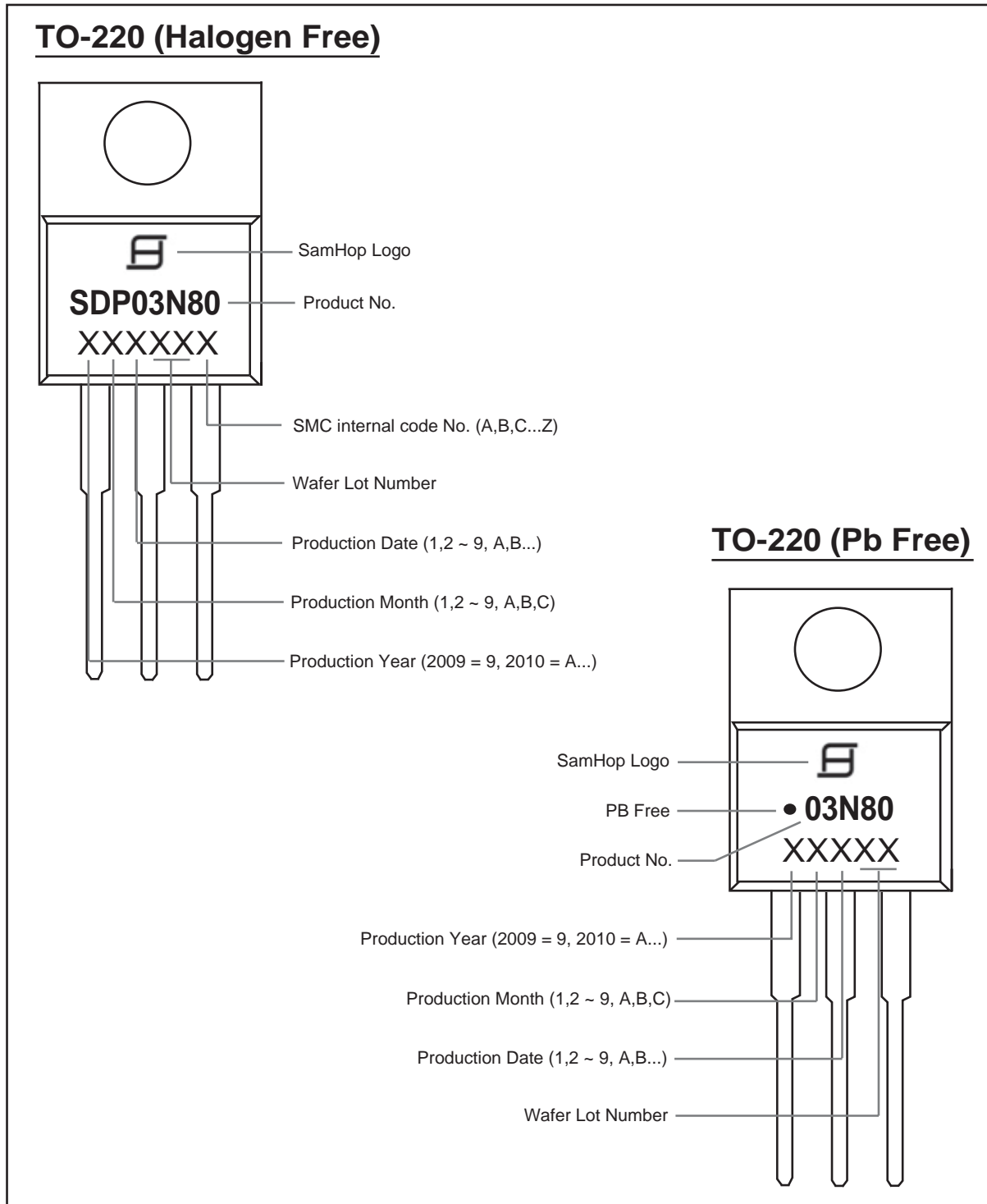
Dec,24,2013

SDP03N80

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Ver 1.1

TOP MARKING DEFINITION



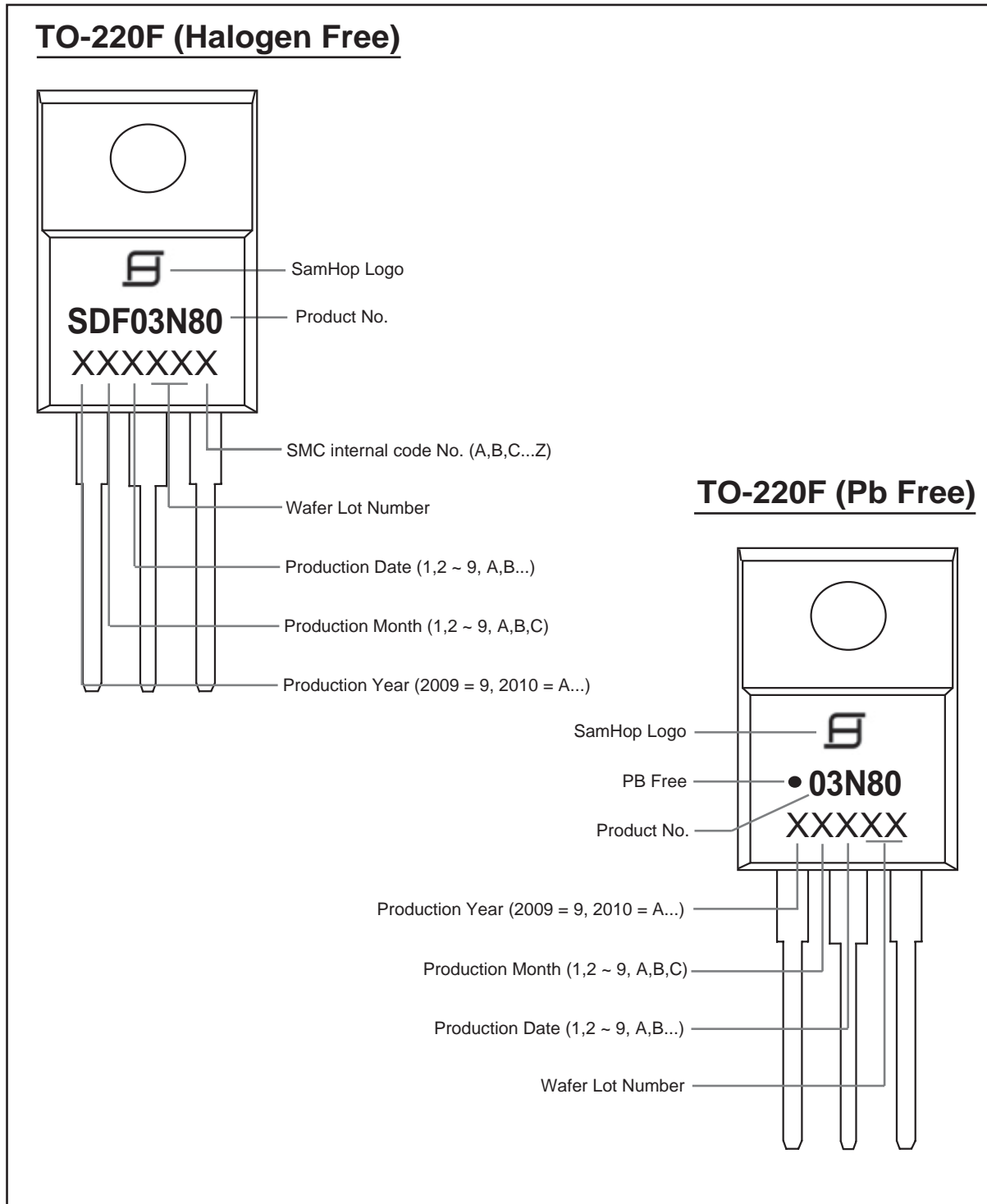
Dec,24,2013

SDP03N80

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Ver 1.1

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Dec,24,2013