

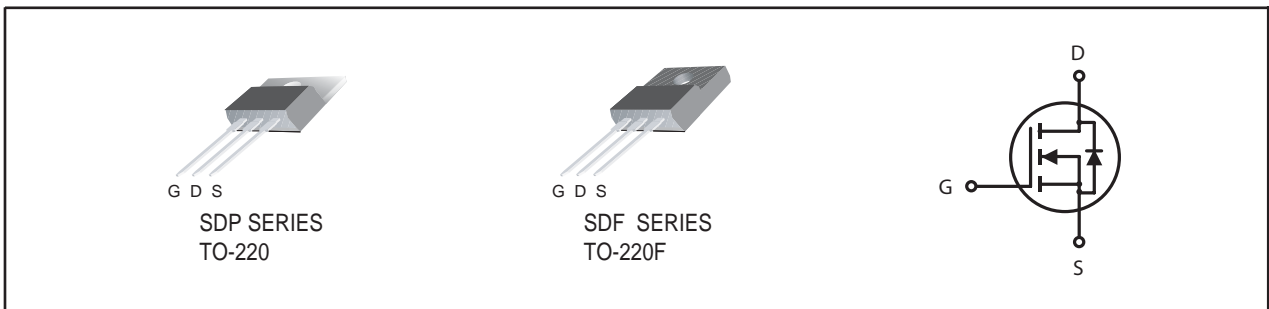


## N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (Ω) Typ
600V	4A	2.0 @ V <sub>GS</sub> =10V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- TO-220 and TO-220F Package.



### ORDERING INFORMATION

Ordering Code	Package	Marking Code	Delivery Mode	RoHS Status
SDP04N60HZ	TO-220	SDP04N60	Tube	Halogen Free
SDP04N60PZ	TO-220	04N60	Tube	Pb Free
SDF04N60HZ	TO-220F	SDF04N60	Tube	Halogen Free
SDF04N60PZ	TO-220F	04N60	Tube	Pb Free

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	SDP04N60	SDF04N60	Units	
V <sub>DS</sub>	Drain-Source Voltage	600		V	
V <sub>GS</sub>	Gate-Source Voltage	±30	±30	V	
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>C</sub> =25°C	4	4	A
		T <sub>C</sub> =100°C	2.8	2.8	A
I <sub>DM</sub>	-Pulsed <sup>a</sup>	12	12	A	
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>c</sup>	90		mJ	
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> =25°C	88	29	W
		T <sub>C</sub> =100°C	44	14.7	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 175		°C	

### THERMAL CHARACTERISTICS

R <sub>θ JC</sub>	Thermal Resistance, Junction-to-Case	1.7	5.1	°C/W
R <sub>θ JA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

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### ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	600			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =480V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±30V , V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2	3	4	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =2A		2.0	2.5	ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =20V , I <sub>D</sub> =2A		2.5		S
<b>DYNAMIC CHARACTERISTICS <sup>b</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		500		pF
C <sub>OSS</sub>	Output Capacitance			57		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			14		pF
<b>SWITCHING CHARACTERISTICS <sup>b</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =300V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> = 6 ohm		20		ns
t <sub>r</sub>	Rise Time			17		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			24		ns
t <sub>f</sub>	Fall Time			11		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =300V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V		11.5		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =300V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V		2		nC
Q <sub>gd</sub>	Gate-Drain Charge			5.3		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =1A		0.765	1.4	V
<b>Notes</b>						
a. Drain current limited by maximum junction temperature.						
b. Guaranteed by design, not subject to production testing.						
c. Starting T <sub>J</sub> =25°C, L=50mH, V <sub>DD</sub> = 50V. (See Figure 12)						

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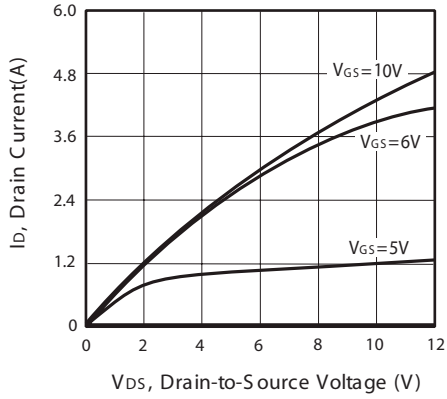


Figure 1. Output C characteristics

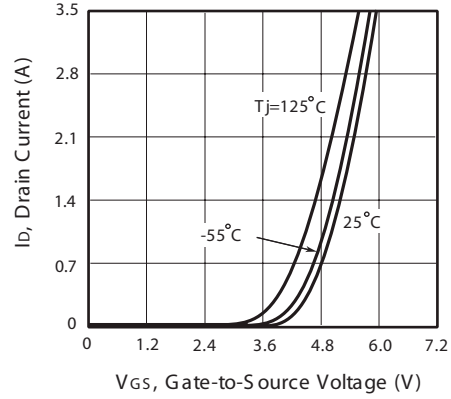


Figure 2. Transfer C characteristics

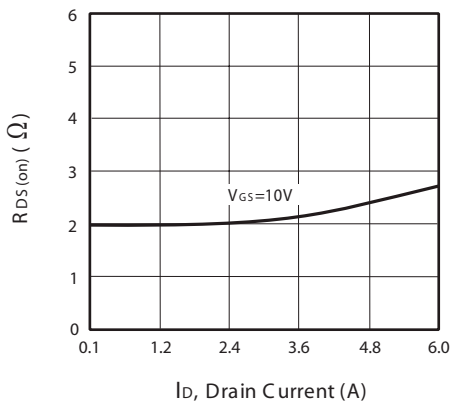


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

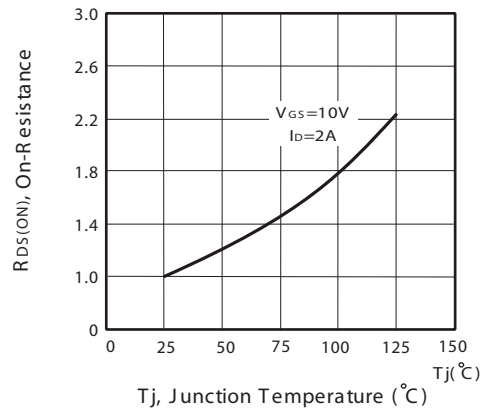


Figure 4. On-R resistance Variation with Drain Current and Temperature

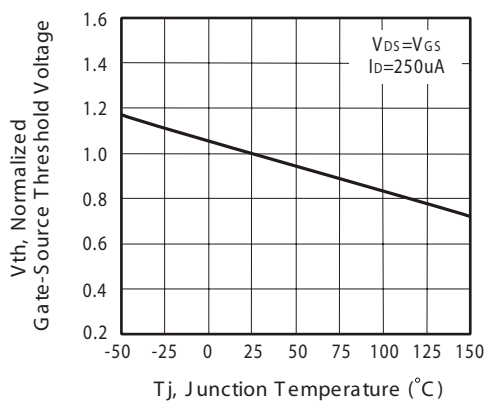


Figure 5. Gate Threshold Variation with Temperature

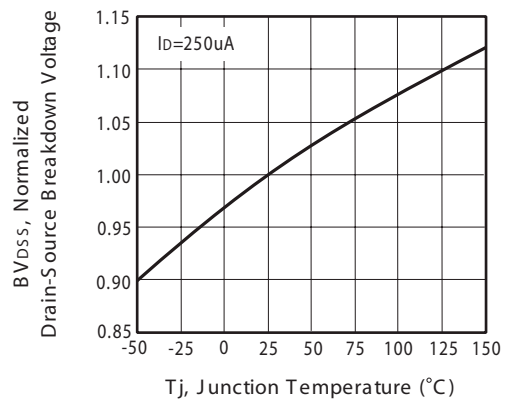


Figure 6. Breakdown Voltage Variation with Temperature

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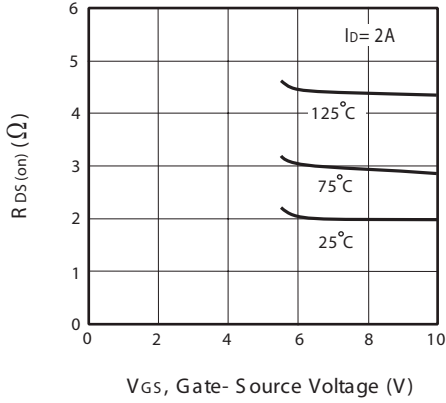


Figure 7. On-Resistance vs. Gate-Source Voltage

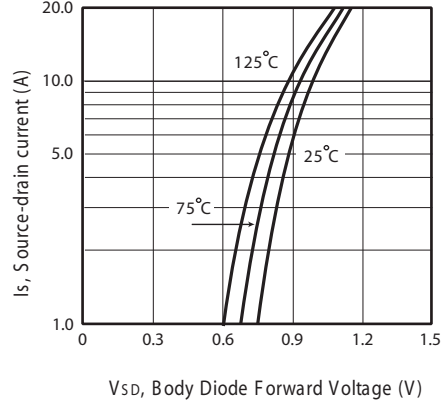


Figure 8. Body Diode Forward Voltage Variation with Source Current

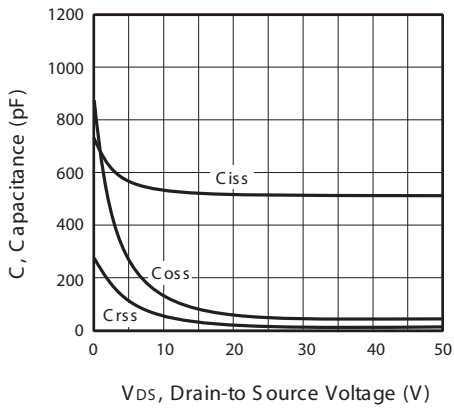


Figure 9. Capacitance

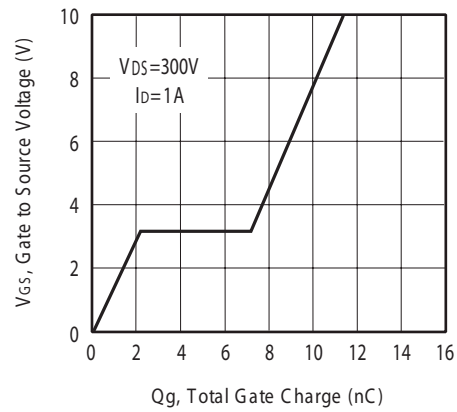


Figure 10. Gate Charge

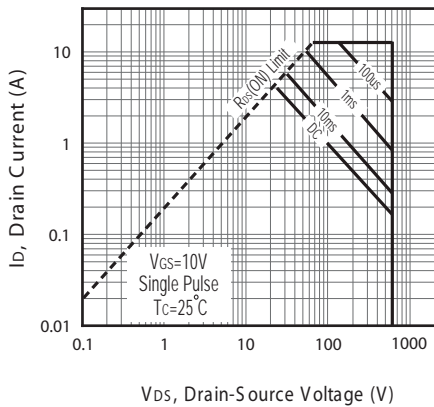


Figure 11a. Maximum Safe Operating Area for SDP04N60

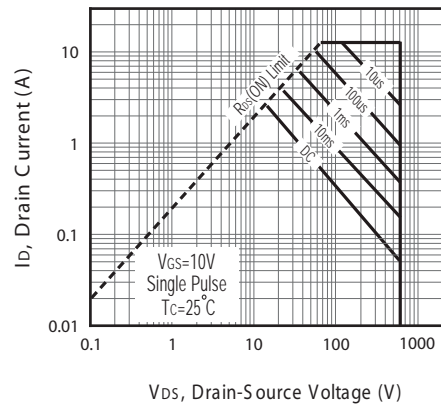
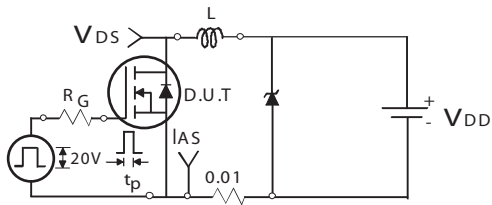


Figure 11b. Maximum Safe Operating Area for SDF04N60

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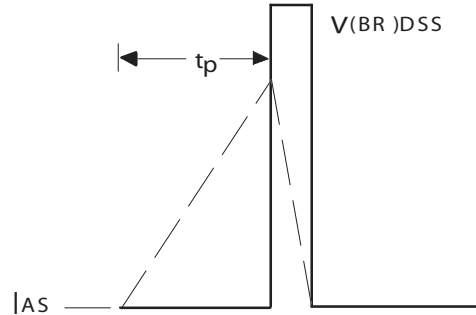
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Unclamped Inductive Test Circuit

Figure 12a.



Unclamped Inductive Waveforms

Figure 12b.

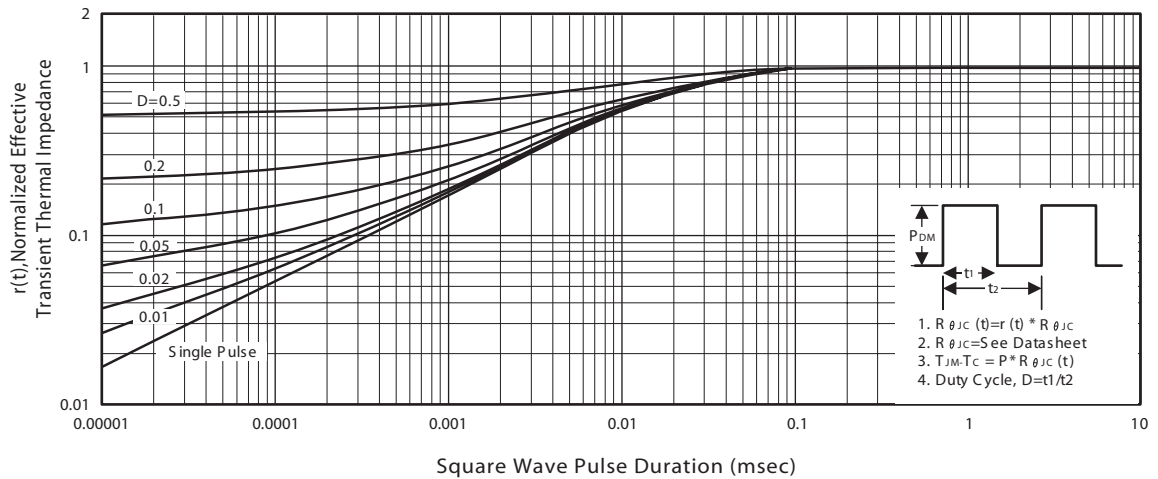


Figure 13a. Normalized Thermal Transient Impedance Curve for SDP04N60

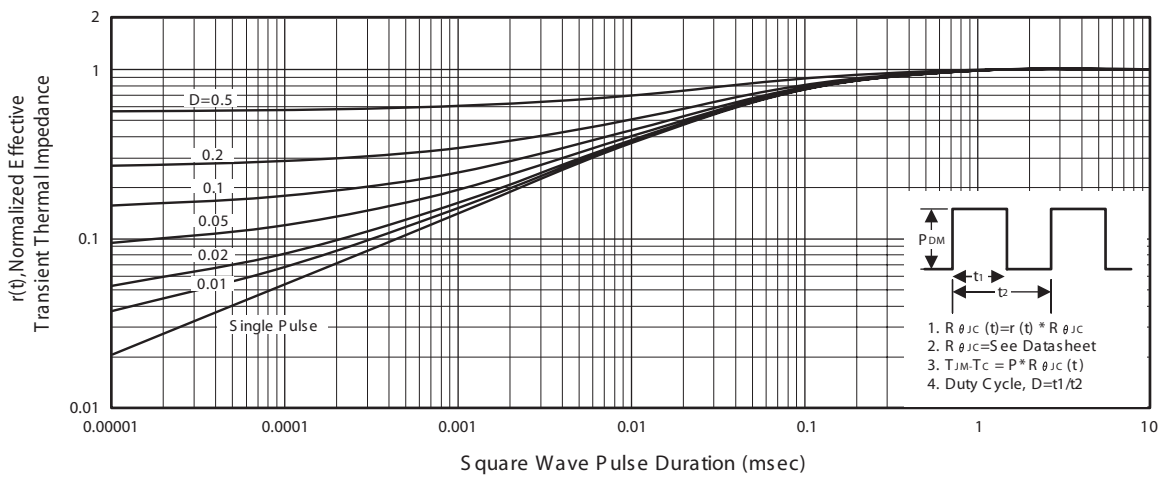


Figure 13b. Normalized Thermal Transient Impedance Curve for SDF04N60

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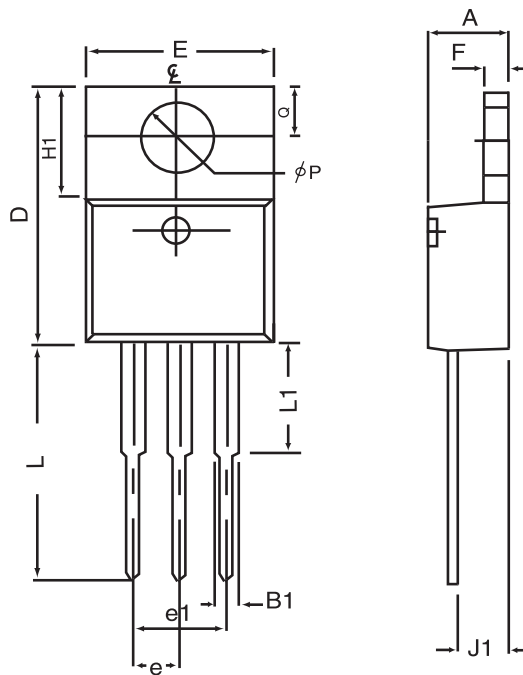
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### PACKAGE OUTLINE DIMENSIONS

TO-220



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.80	0.170	0.189
B1	1.27	1.65	0.050	0.630
D	14.6	16.00	0.575	0.610
E	9.70	10.41	0.382	0.410
e	2.34	2.74	0.092	0.108
e1	4.68	5.48	0.184	0.216
F	1.14	1.40	0.045	0.055
H1	5.97	6.73	0.235	0.265
J1	2.20	2.79	0.087	0.110
L	12.88	14.22	0.507	0.560
L1	3.00	6.35	0.120	0.250
φP	3.50	3.94	0.138	0.155
Q	2.54	3.05	0.100	0.120

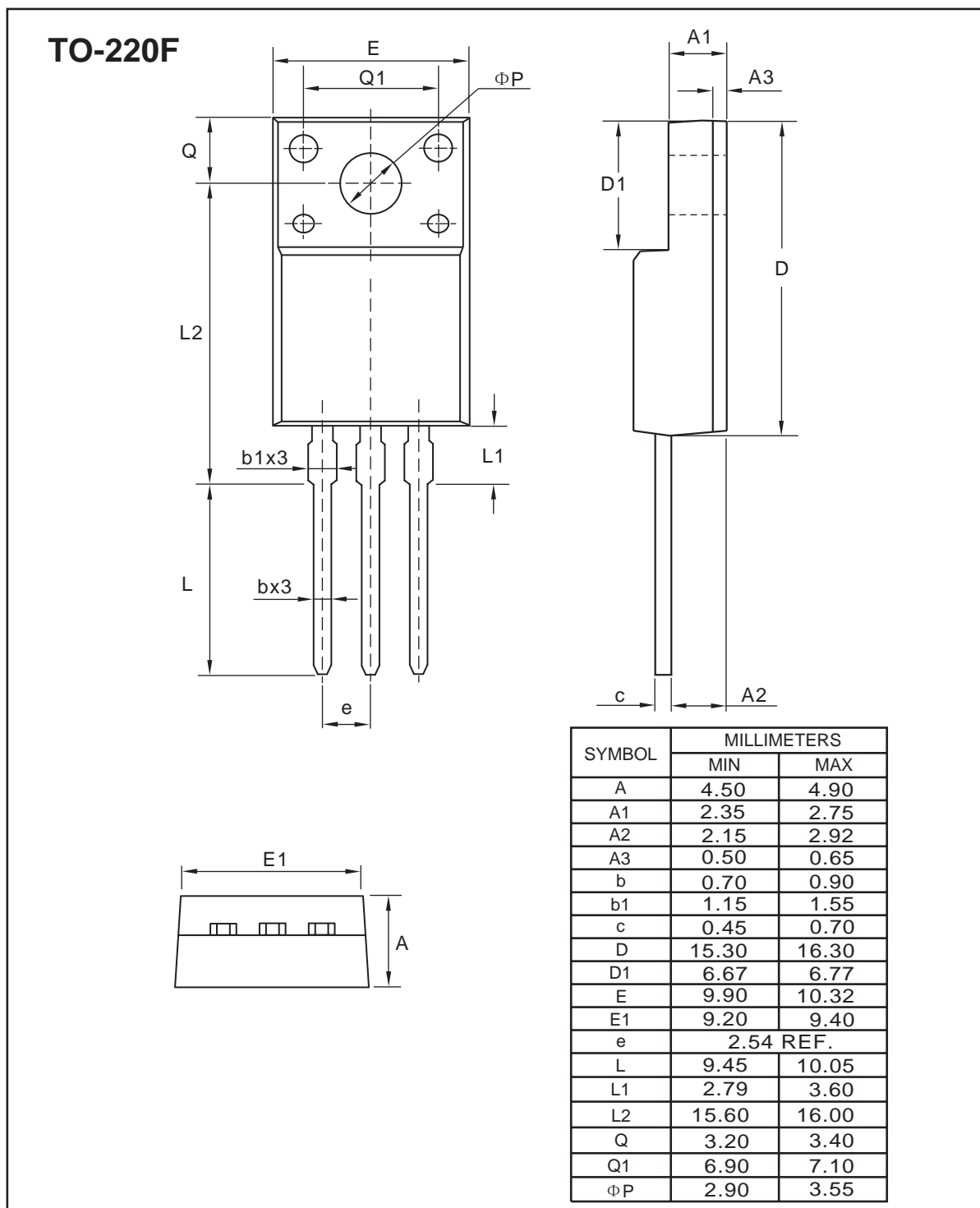
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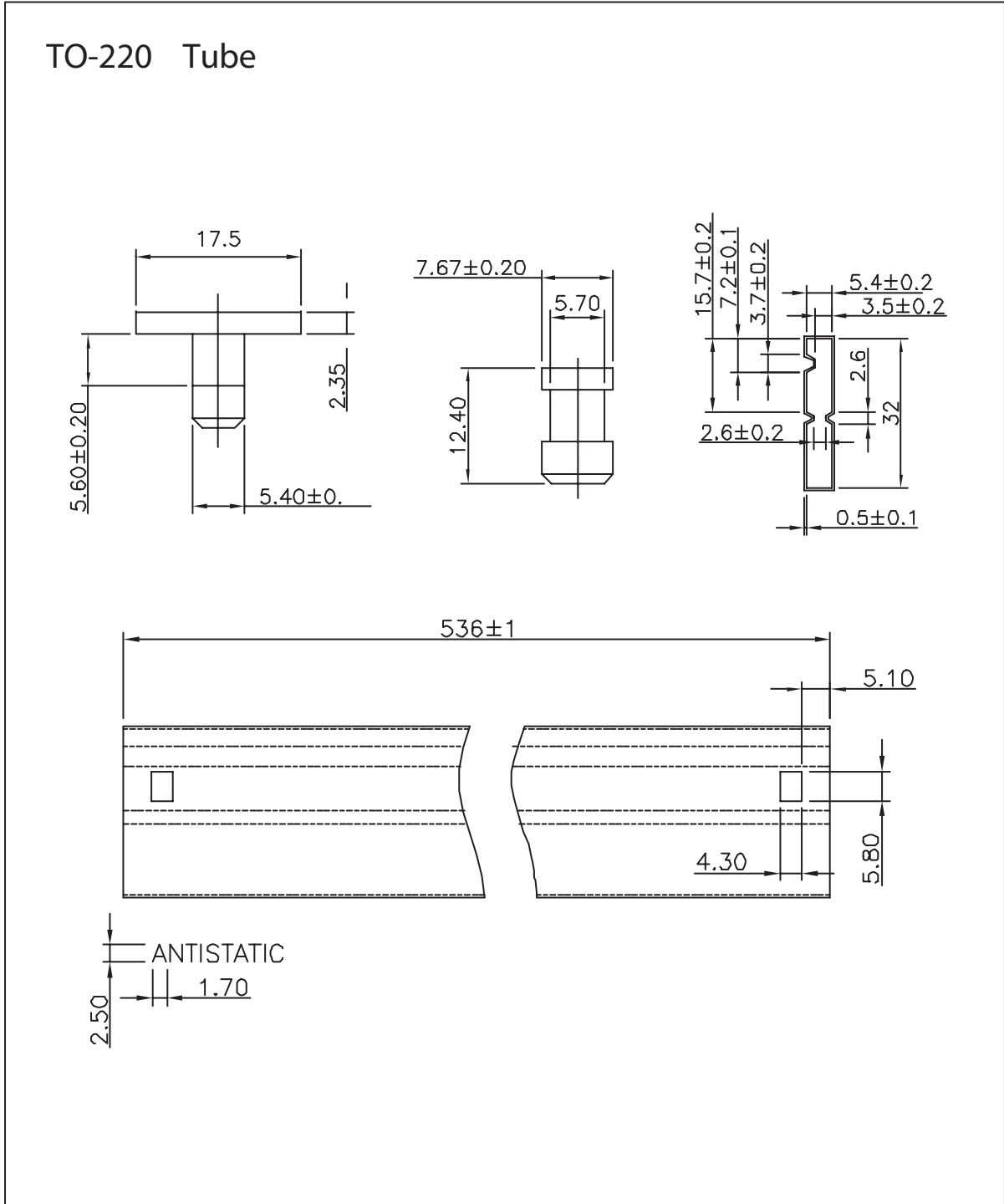


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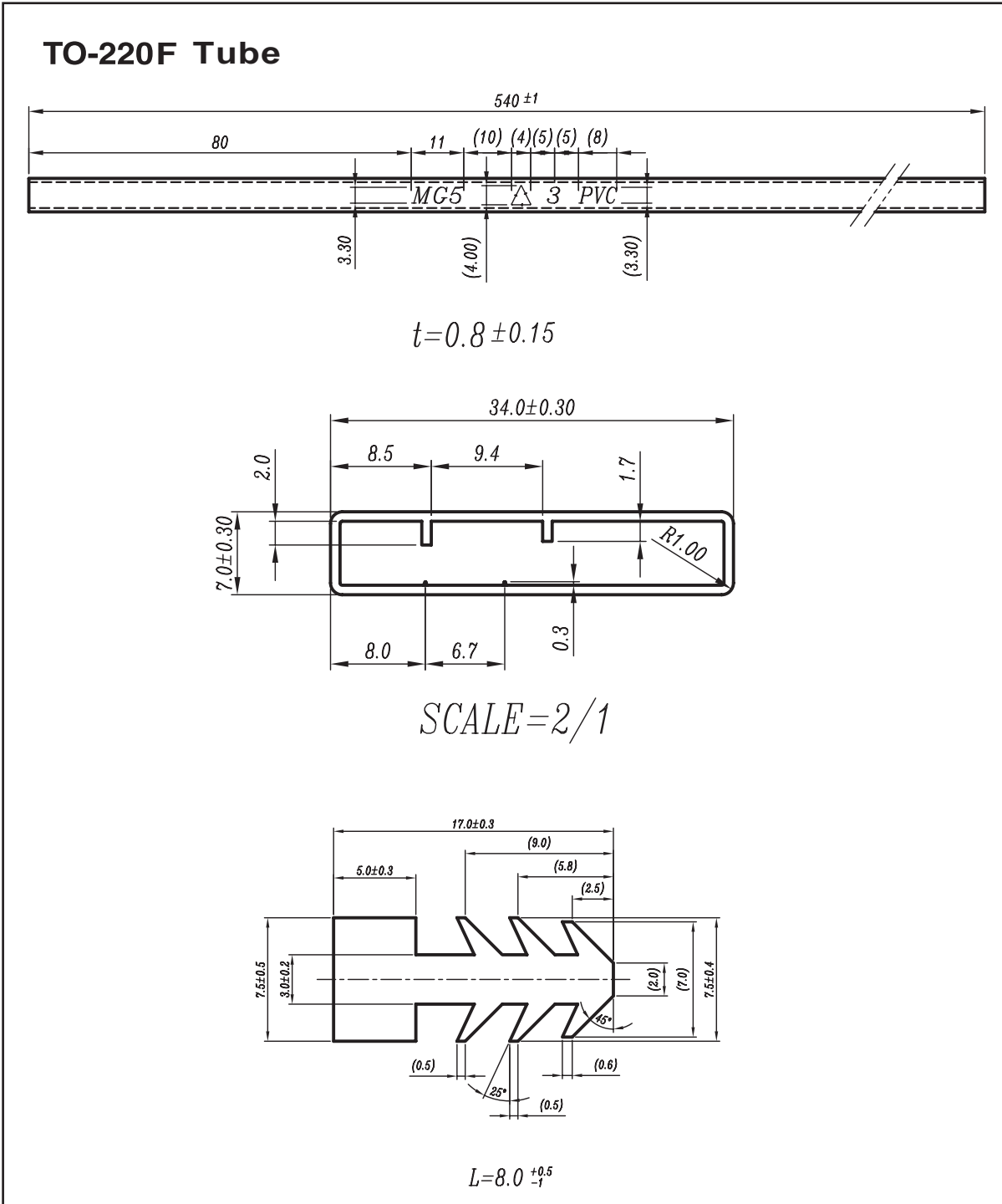


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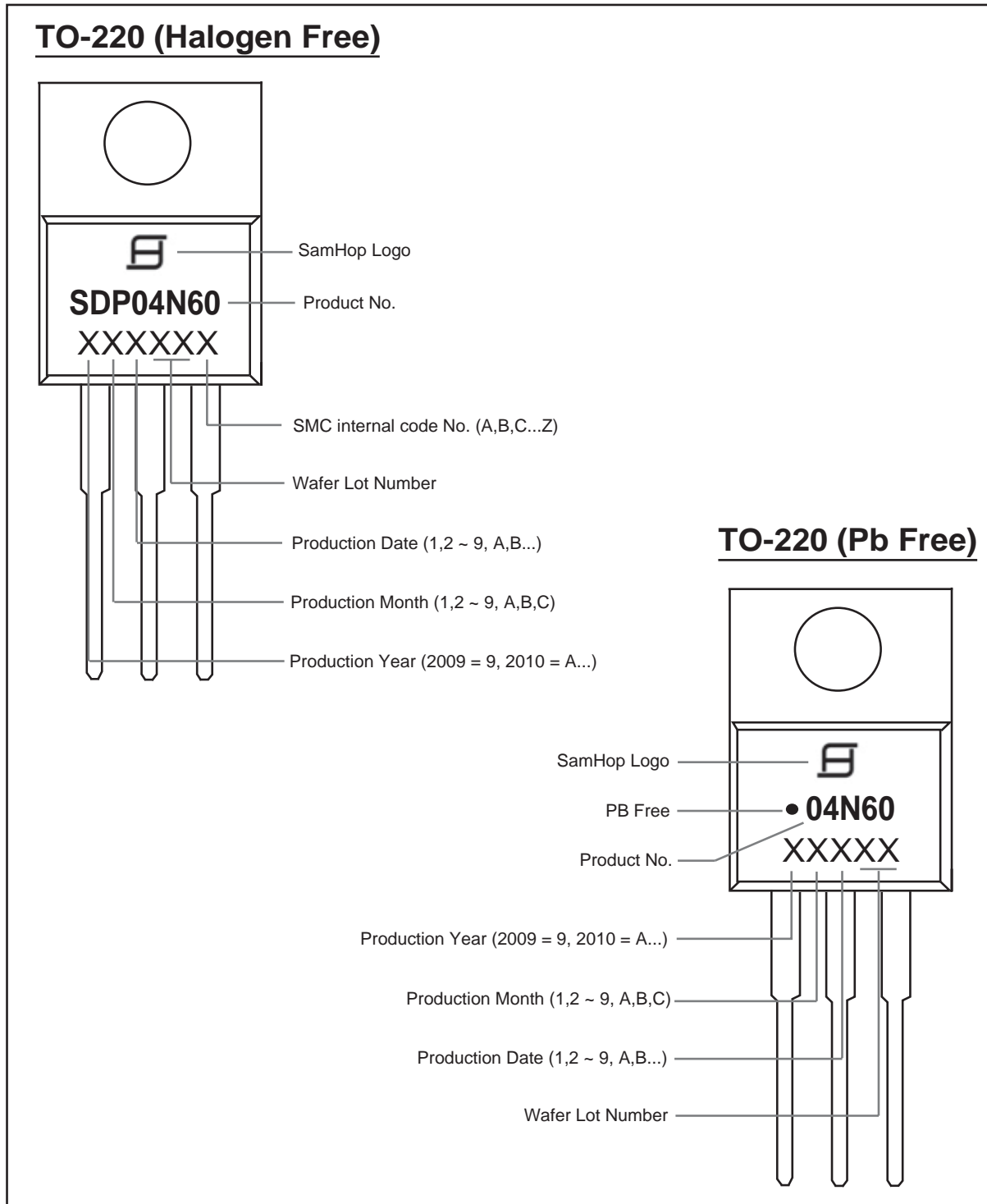
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## TOP MARKING DEFINITION



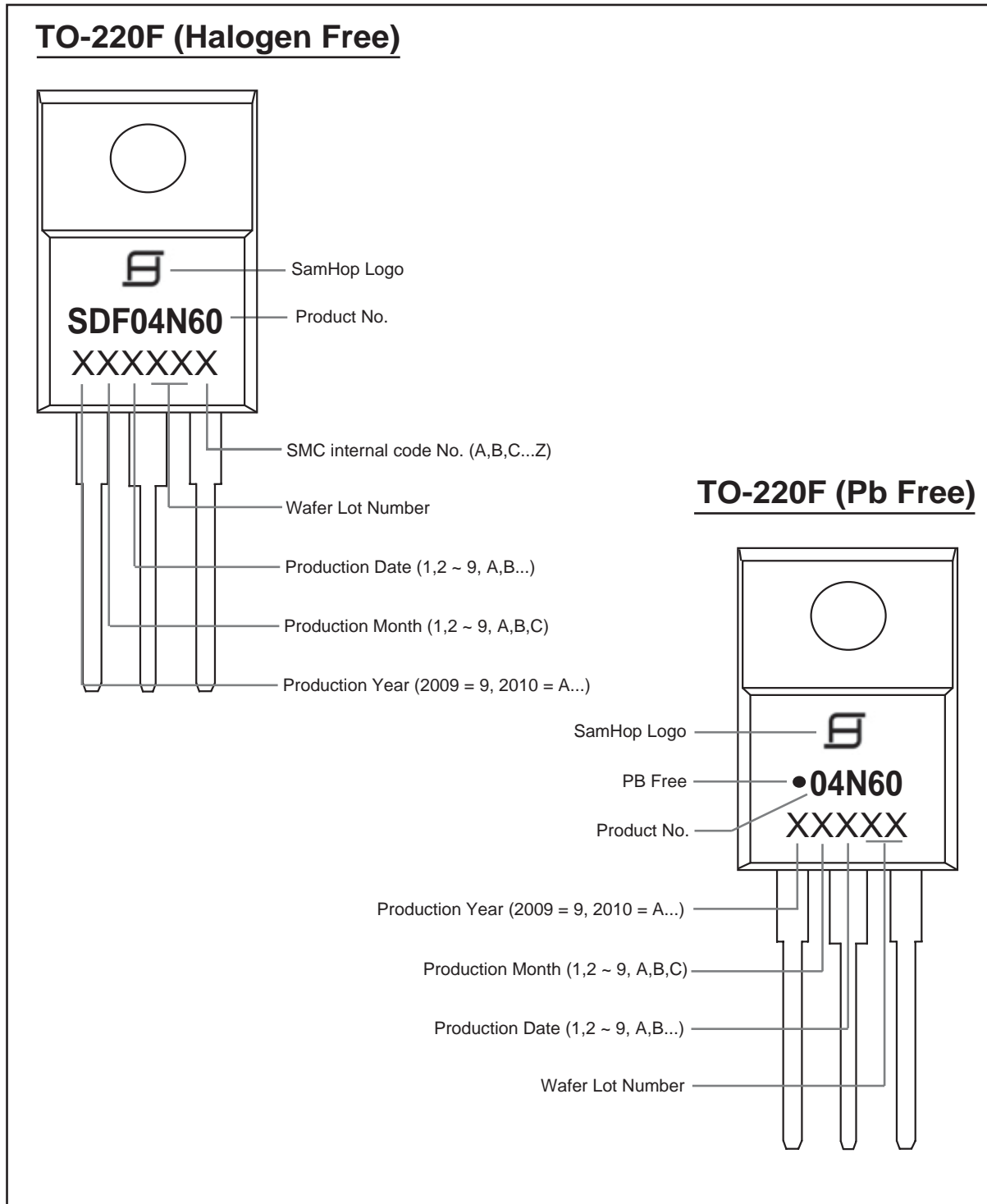
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