Elektronische Bauelemente

# SDG5521C

**N-Ch: 5A, 20V, $R_{DS(ON)}$ 58 mΩ**
**P-Ch: -4.7A, -20V, $R_{DS(ON)}$ 77 mΩ**
**N & P-Ch Enhancement Mode Power MOSFET**

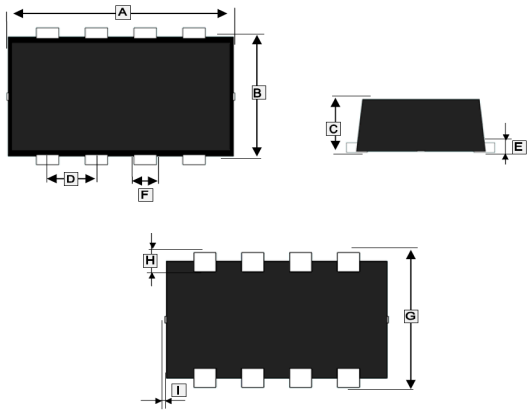
RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

## DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

**DFN2*3**




| REF. | Millimeter | | REF. | Millimeter | |
|---|---|---|---|---|---|
| | Min. | Max. | | Min. | Max. |
| A | 3.00 BSC. | | F | 0.24 | 0.35 |
| B | 1.70 BSC. | | G | 2.00 BSC. | |
| C | 0.70 | 0.90 | H | 0.20 | 0.40 |
| D | 0.65 BSC. | | I | 0 | 0.15 |
| E | 0.08 | 0.25 | | | |

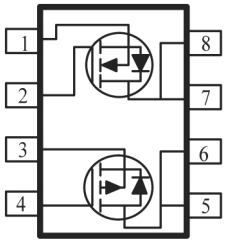
## FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe DFN2*3 saves board space.
- Fast switching speed.
- High performance trench technology.

## PACKAGE INFORMATION

| Package | MPQ | Leader Size |
|---|---|---|
| DFN2*3 | 3K | 13' inch |

**Top View**




## ABSOLUTE MAXIMUM RATINGS ($T_A$=25°C unless otherwise specified)

| Parameter | | Symbol | Rating | | Unit |
|---|---|---|---|---|---|
| | | | N-CH | P-CH | |
| Drain-Source Voltage | | $V_{DS}$ | 20 | -20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±8 | ±8 | V |
| Continuous Drain Current [1] | $T_A$= 25℃ | $I_D$ | 5 | -4.7 | A |
| | $T_A$= 70℃ | | 4.1 | -3.9 | A |
| Pulsed Drain Current [2] | | $I_{DM}$ | 8 | -8 | A |
| Continuous Source Current (Diode Conduction) [1] | | $I_S$ | 4.5 | -4.5 | A |
| Total Power Dissipation [1] | $T_A$= 25℃ | $P_D$ | 2.1 | | W |
| | $T_A$= 70℃ | | 1.3 | | W |
| Operating Junction & Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 ~ 150 | | ℃ |
| **Thermal Resistance Ratings** | | | | | |
| Maximum Junction-to-Ambient [1] | t≦10 sec | $R_{\theta JA}$ | 62.5 | | ℃ / W |
| | Steady State | | 80 | | ℃ / W |

Notes:
1 Surface Mounted on 1" x 1" FR4 Board.
2 Pulse width limited by maximum junction temperature.

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**N & P-Ch Enhancement Mode Power MOSFET**

## ELECTRICAL CHARACTERISTICS ($T_A$=25°C unless otherwise specified)

| Parameter | Symbol | Ch | Min. | Typ. | Max. | Unit | Teat Conditions |
|---|---|---|---|---|---|---|---|
| **Static** | | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | N | 1 | - | - | V | $V_{DS}$=$V_{GS}$, $I_D$=250μA |
| | | P | -1 | - | - | | $V_{DS}$=$V_{GS}$, $I_D$= -250μA |
| Gate-Body Leakage | $I_{GSS}$ | N | - | - | 100 | μA | $V_{DS}$=0, $V_{GS}$=8V |
| | | P | - | - | -100 | | $V_{DS}$=0, $V_{GS}$= -8V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | N | - | - | 1 | μA | $V_{DS}$=16V, $V_{GS}$=0 |
| | | P | - | - | -1 | | $V_{DS}$= -16V, $V_{GS}$=0 |
| | | N | - | - | 10 | | $V_{DS}$=16V, $V_{GS}$=0, $T_J$=55℃ |
| | | P | - | - | -10 | | $V_{DS}$= -16V, $V_{GS}$=0, $T_J$=55℃ |
| On-State Drain Current [1] | $I_{D(on)}$ | N | 5 | - | - | A | $V_{DS}$=5V, $V_{GS}$=4.5V |
| | | P | -5 | - | - | | $V_{DS}$= -5V, $V_{GS}$= -4.5V |
| Drain-Source On-Resistance [1] | $R_{DS(ON)}$ | N | - | - | 58 | mΩ | $V_{GS}$=4.5V, $I_D$=1A |
| | | | - | - | 64 | | $V_{GS}$=2.5V, $I_D$=1A |
| | | P | - | - | 77 | | $V_{GS}$= -4.5V, $I_D$= -1A |
| | | | - | - | 85 | | $V_{GS}$= -2.5V, $I_D$= -1A |
| Forward Tranconductance [1] | $g_{fS}$ | N | - | 10 | | S | $V_{DS}$=5V, $I_D$=1A |
| | | P | - | 5 | | | $V_{DS}$= -5V, $I_D$= -1A |
| Diode Forward Voltage [1] | $V_{SD}$ | N | - | 0.8 | - | V | $V_{GS}$=0, $I_S$=1A |
| | | P | - | -0.83 | - | | $V_{GS}$=0, $I_S$= -1A |
| **Dynamic [2]** | | | | | | | |
| Total Gate Charge | $Q_g$ | N | - | 2 | - | nC | N-Channel<br>$I_D$=1A, $V_{DS}$=15V, $V_{GS}$=4.5V<br><br>P-Channel<br>$I_D$= -1A, $V_{DS}$= -15V, $V_{GS}$= -4.5V |
| | | P | - | 7 | - | | |
| Gate-Source Charge | $Q_{gs}$ | N | - | 0.4 | - | | |
| | | P | - | 1 | - | | |
| Gate-Drain Charge | $Q_{gd}$ | N | - | 0.7 | - | | |
| | | P | - | 2 | - | | |
| Turn-On Delay Time | $T_{d(on)}$ | N | - | 6 | - | nS | N-Channel<br>$V_{DD}$=15V, $V_{GEN}$=4.5V<br>$I_D$=1A, $R_{GEN}$=15Ω<br><br>P-Channel<br>$V_{DD}$= -15V, $V_{GEN}$= -4.5V<br>$I_D$=1A, $R_{GEN}$=15Ω |
| | | P | - | 10 | - | | |
| Rise Time | $T_r$ | N | - | 9 | - | | |
| | | P | - | 1 | - | | |
| Turn-Off Delay Time | $T_{d(off)}$ | N | - | 5 | - | | |
| | | P | - | 11 | - | | |
| Fall Time | $T_f$ | N | - | 16 | - | | |
| | | P | - | 12 | - | | |

Notes:
1. Pulse test：PW≦300μs duty cycle≦2%.
2. Guaranteed by design, not subject to production testing.