



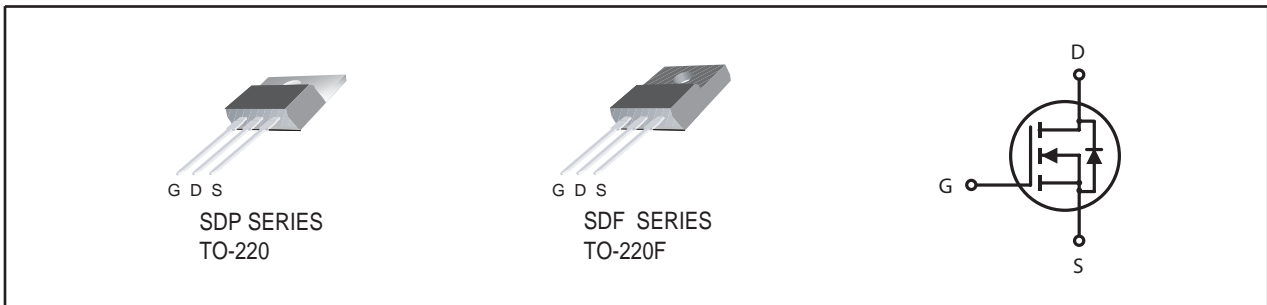
N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY

| V _{DSS} | I _D | R _{DS(ON)} (Ω) Typ |
|------------------|----------------|-----------------------------|
| 200V | 2A | 3.0 @ V _{GS} =10V |

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- TO-220 and TO-220F Package.



ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

| Symbol | Parameter | SDP02N20 | SDF02N20 | Units | |
|-----------------------------------|--|-----------------------|----------|-------|---|
| V _{DS} | Drain-Source Voltage | 200 | | V | |
| V _{GS} | Gate-Source Voltage | ±30 | ±30 | V | |
| I _D | Drain Current-Continuous ^a | T _C =25°C | 2 | 2 | A |
| | | T _C =100°C | 1.4 | 1.4 | A |
| I _{DM} | -Pulsed ^a | 5.9 | 5.9 | A | |
| E _{AS} | Single Pulse Avalanche Energy ^c | 81 | | mJ | |
| P _D | Maximum Power Dissipation | T _C =25°C | 75 | 25 | W |
| | | T _C =100°C | 37.5 | 12.5 | W |
| T _J , T _{STG} | Operating Junction and Storage Temperature Range | -55 to 175 | | °C | |

THERMAL CHARACTERISTICS

| Symbol | Parameter | SDP02N20 | SDF02N20 | Units |
|------------------|---|----------|----------|-------|
| R _{θJC} | Thermal Resistance, Junction-to-Case | 2 | 6 | °C/W |
| R _{θJA} | Thermal Resistance, Junction-to-Ambient | 62.5 | 62.5 | °C/W |

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ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|----------------------------------|---|-----|------|------|-------|
| OFF CHARACTERISTICS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} =0V , I _D =250uA | 200 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =160V , V _{GS} =0V | | | 1 | uA |
| I _{GSS} | Gate-Body Leakage Current | V _{GS} = ±30V , V _{DS} =0V | | | ±100 | nA |
| ON CHARACTERISTICS | | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250uA | 2 | 3 | 4 | V |
| R _{DS(ON)} | Drain-Source On-State Resistance | V _{GS} =10V , I _D =1A | | 3.0 | 3.9 | ohm |
| g _{FS} | Forward Transconductance | V _{DS} =10V , I _D =1A | | 1.3 | | S |
| DYNAMIC CHARACTERISTICS ^b | | | | | | |
| C _{ISS} | Input Capacitance | V _{DS} =25V, V _{GS} =0V f=1.0MHz | | 183 | | pF |
| C _{OSS} | Output Capacitance | | | 30 | | pF |
| C _{RSS} | Reverse Transfer Capacitance | | | 6 | | pF |
| SWITCHING CHARACTERISTICS ^b | | | | | | |
| t _{D(ON)} | Turn-On Delay Time | V _{DD} =100V I _D =1A V _{GS} =10V R _{GEN} = 6 ohm | | 9.5 | | ns |
| t _r | Rise Time | | | 10 | | ns |
| t _{D(OFF)} | Turn-Off Delay Time | | | 15.4 | | ns |
| t _f | Fall Time | | | 5.2 | | ns |
| Q _g | Total Gate Charge | V _{DS} =100V, I _D =1A, V _{GS} =10V | | 2.8 | | nC |
| Q _{gs} | Gate-Source Charge | V _{DS} =100V, I _D =1A, V _{GS} =10V | | 0.95 | | nC |
| Q _{gd} | Gate-Drain Charge | | | 0.92 | | nC |
| DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS | | | | | | |
| V _{SD} | Diode Forward Voltage | V _{GS} =0V, I _S =1A | | 0.82 | 1.4 | V |
| Notes | | | | | | |
| a. Drain current limited by maximum junction temperature. | | | | | | |
| b. Guaranteed by design, not subject to production testing. | | | | | | |
| c. Starting T _J =25°C, L=50mH, V _{DD} = 50V. (See Figure 12) | | | | | | |

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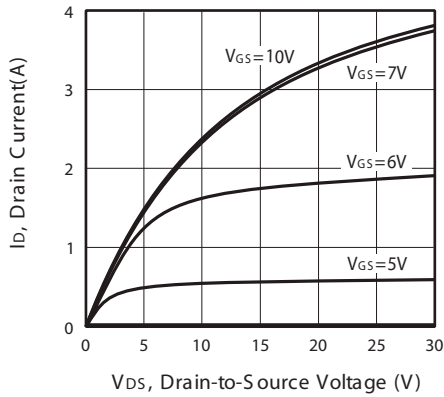


Figure 1. Output Characteristics

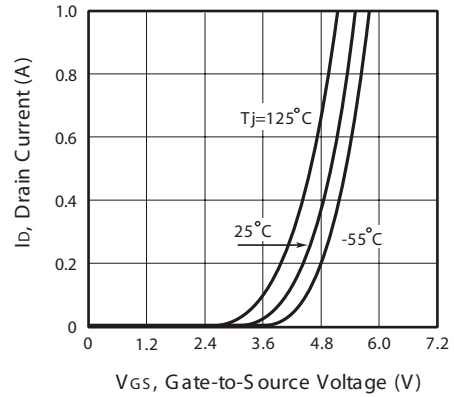


Figure 2. Transfer Characteristics

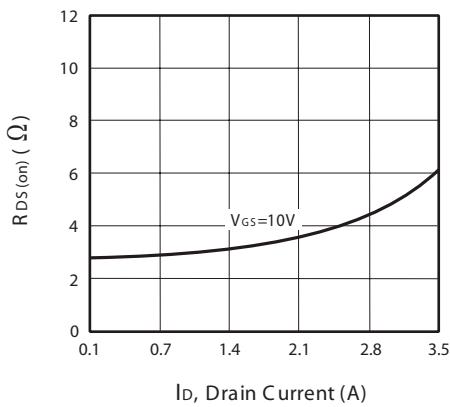


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

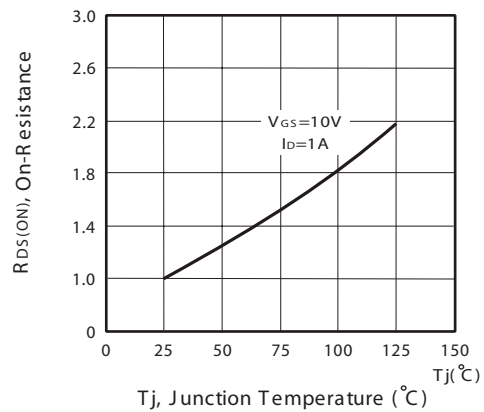


Figure 4. On-Resistance Variation with Drain Current and Temperature

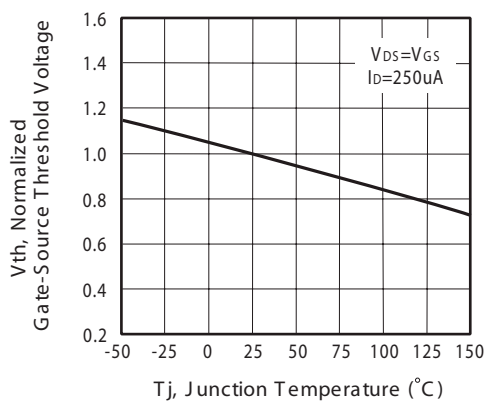


Figure 5. Gate Threshold Variation with Temperature

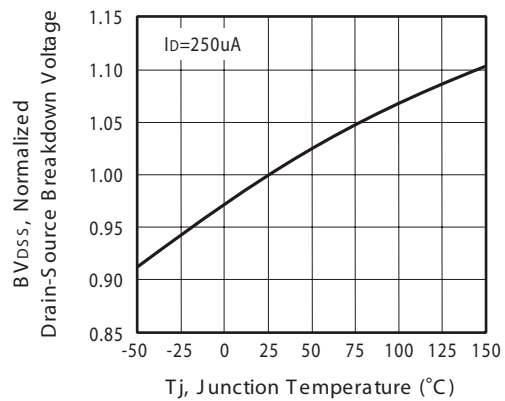


Figure 6. Breakdown Voltage Variation with Temperature

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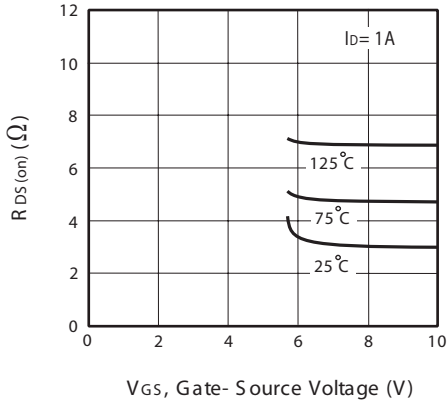


Figure 7. On-Resistance vs. Gate-Source Voltage

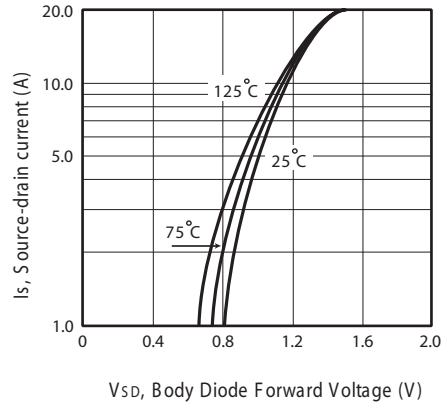


Figure 8. Body Diode Forward Voltage Variation with Source Current

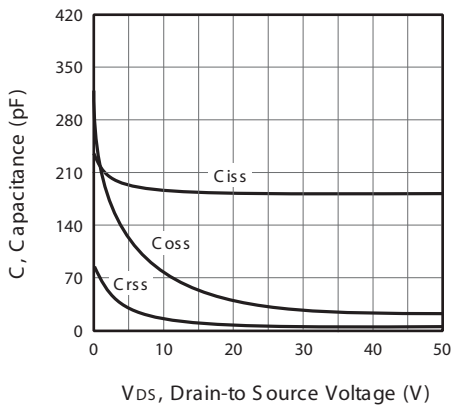


Figure 9. Capacitance

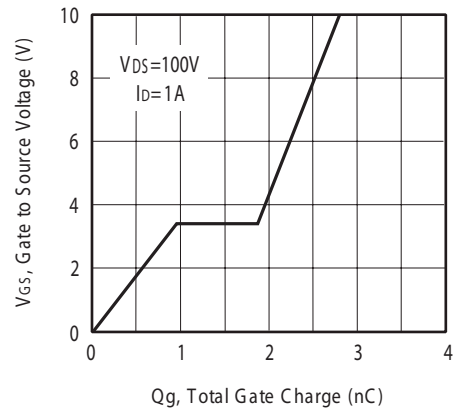


Figure 10. Gate Charge

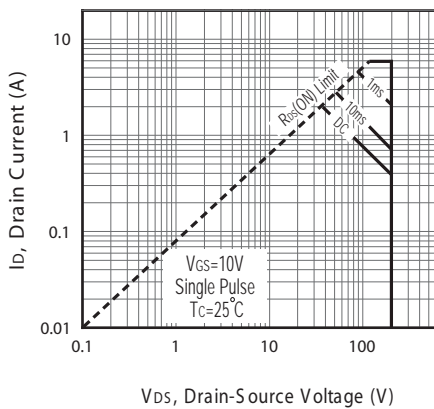


Figure 11a. Maximum Safe Operating Area for SDP02N20

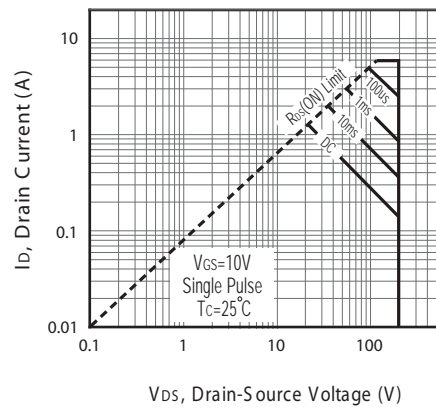
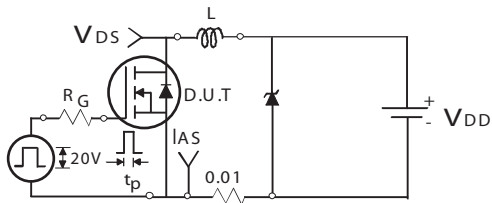


Figure 11b. Maximum Safe Operating Area for SDF02N20

SDP02N20

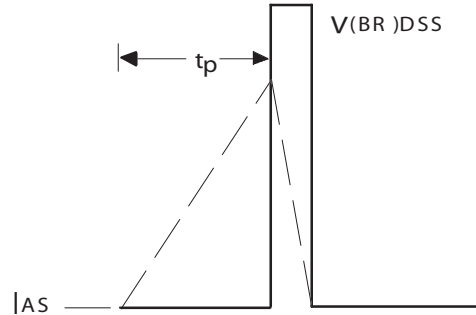
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Unclamped Inductive Test Circuit

Figure 12a.



Unclamped Inductive Waveforms

Figure 12b.

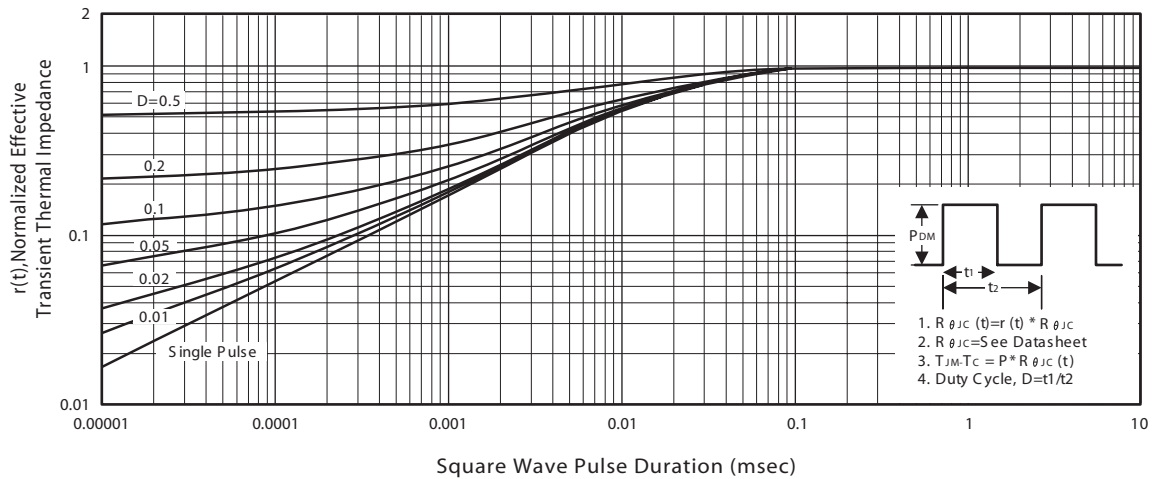


Figure 13a. Normalized Thermal Transient Impedance Curve for SDP02N20

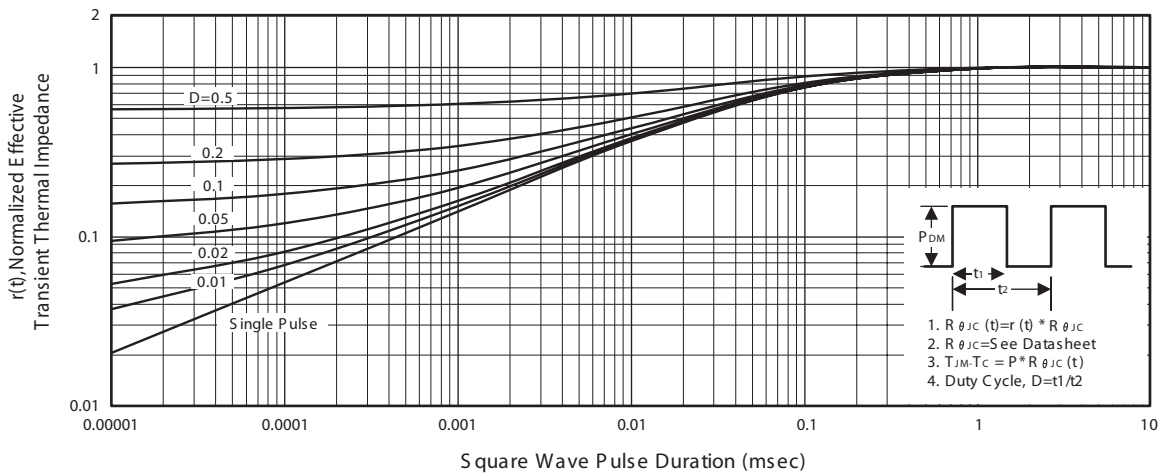


Figure 13b. Normalized Thermal Transient Impedance Curve for SDF02N20

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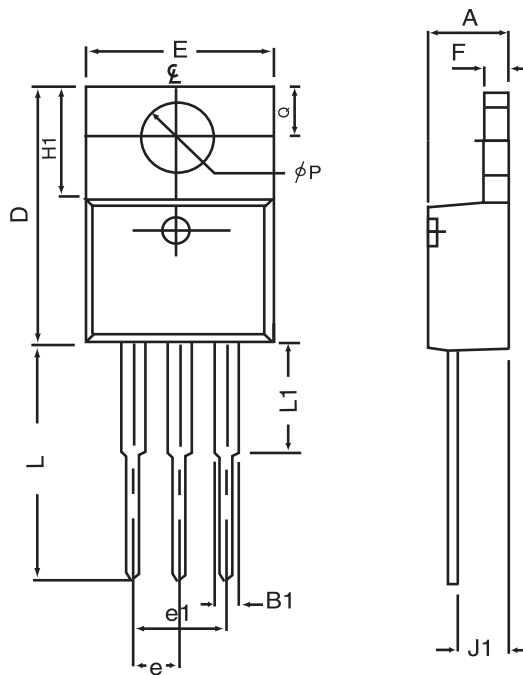
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PACKAGE OUTLINE DIMENSIONS

TO-220



| SYMBOLS | MILLIMETERS | | INCHES | |
|---------|-------------|-------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.32 | 4.80 | 0.170 | 0.189 |
| B1 | 1.27 | 1.65 | 0.050 | 0.630 |
| D | 14.6 | 16.00 | 0.575 | 0.610 |
| E | 9.70 | 10.41 | 0.382 | 0.410 |
| e | 2.34 | 2.74 | 0.092 | 0.108 |
| e1 | 4.68 | 5.48 | 0.184 | 0.216 |
| F | 1.14 | 1.40 | 0.045 | 0.055 |
| H1 | 5.97 | 6.73 | 0.235 | 0.265 |
| J1 | 2.20 | 2.79 | 0.087 | 0.110 |
| L | 12.88 | 14.22 | 0.507 | 0.560 |
| L1 | 3.00 | 6.35 | 0.120 | 0.250 |
| phi P | 3.50 | 3.94 | 0.138 | 0.155 |
| Q | 2.54 | 3.05 | 0.100 | 0.120 |

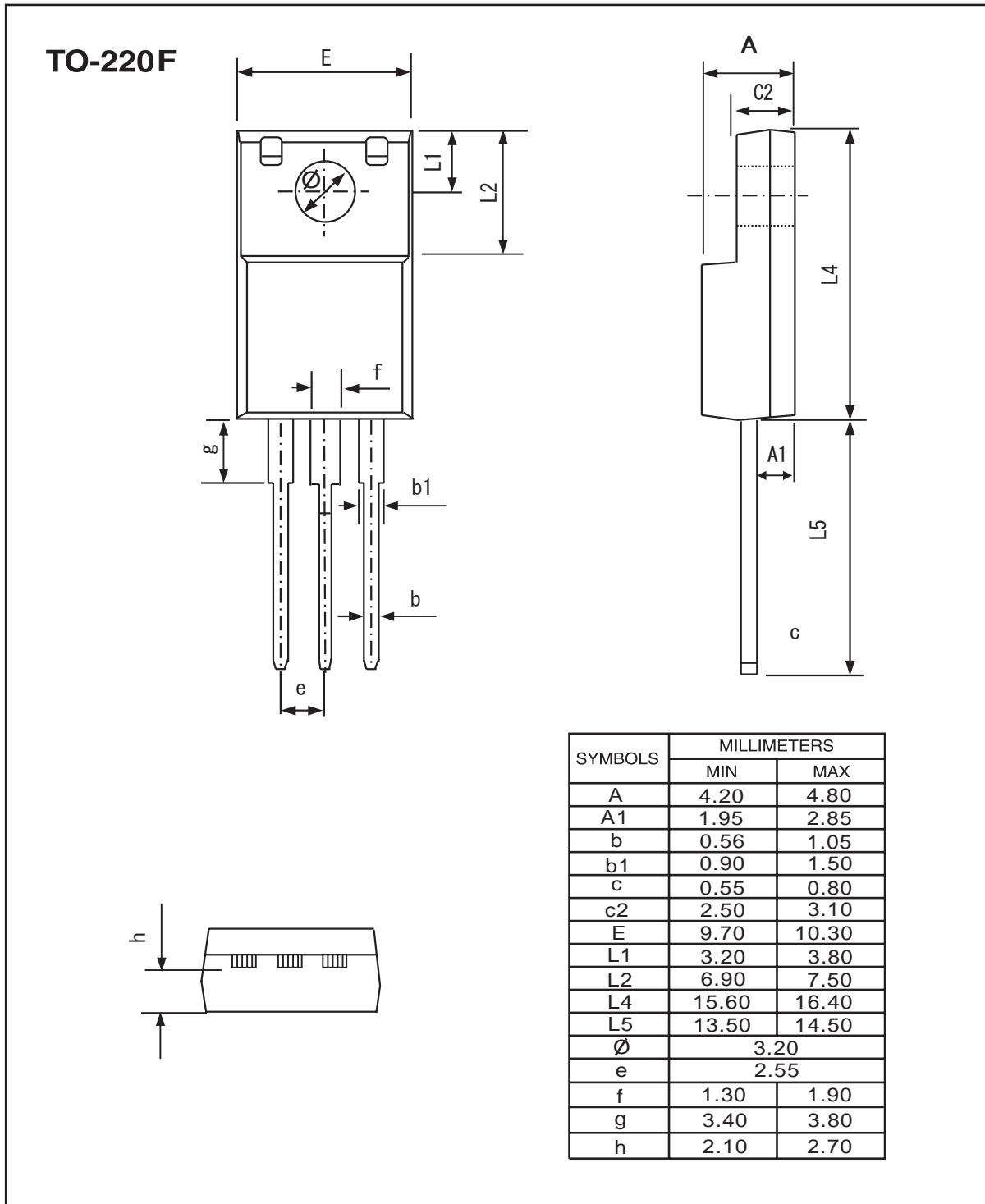
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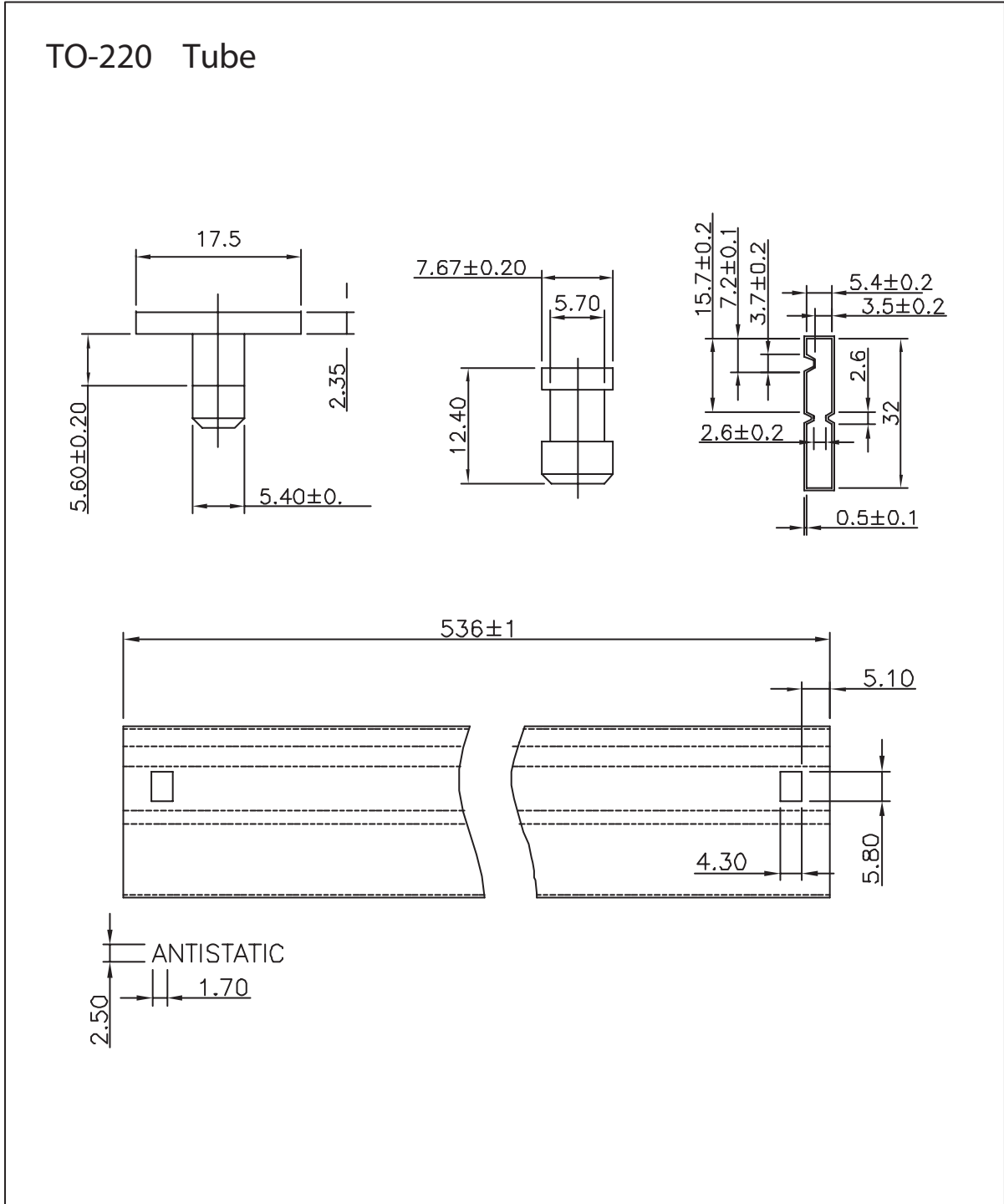


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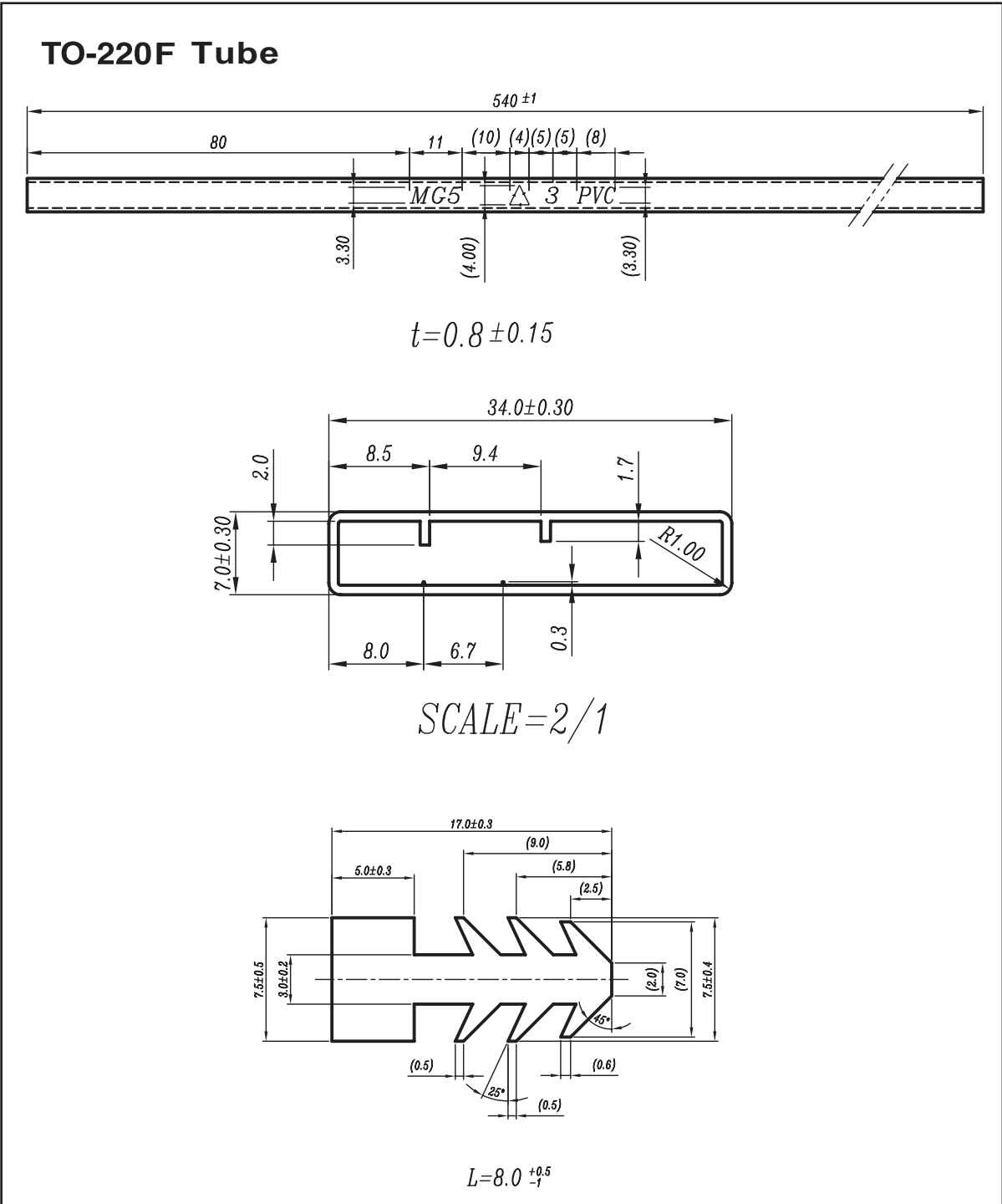
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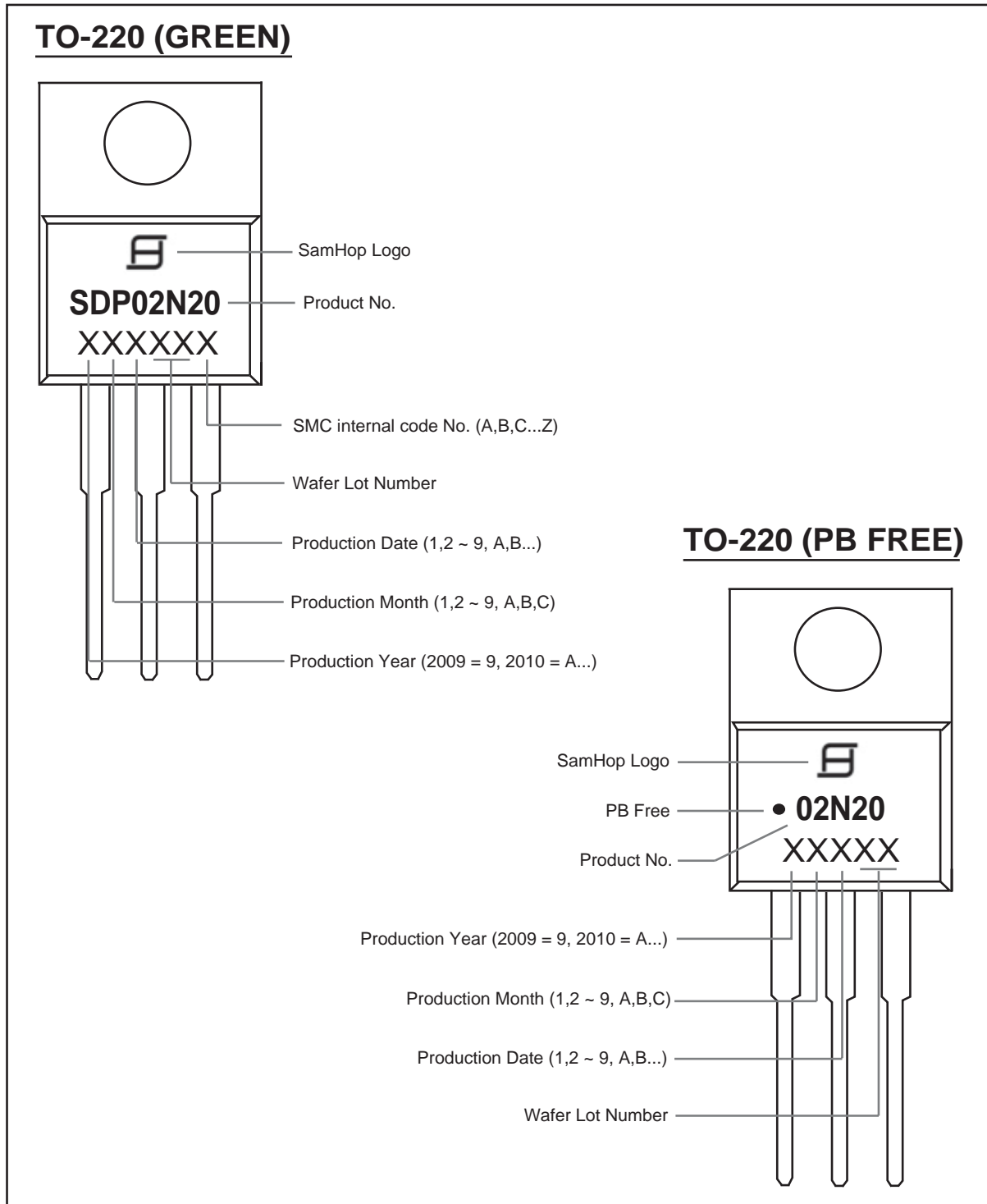
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TOP MARKING DEFINITION



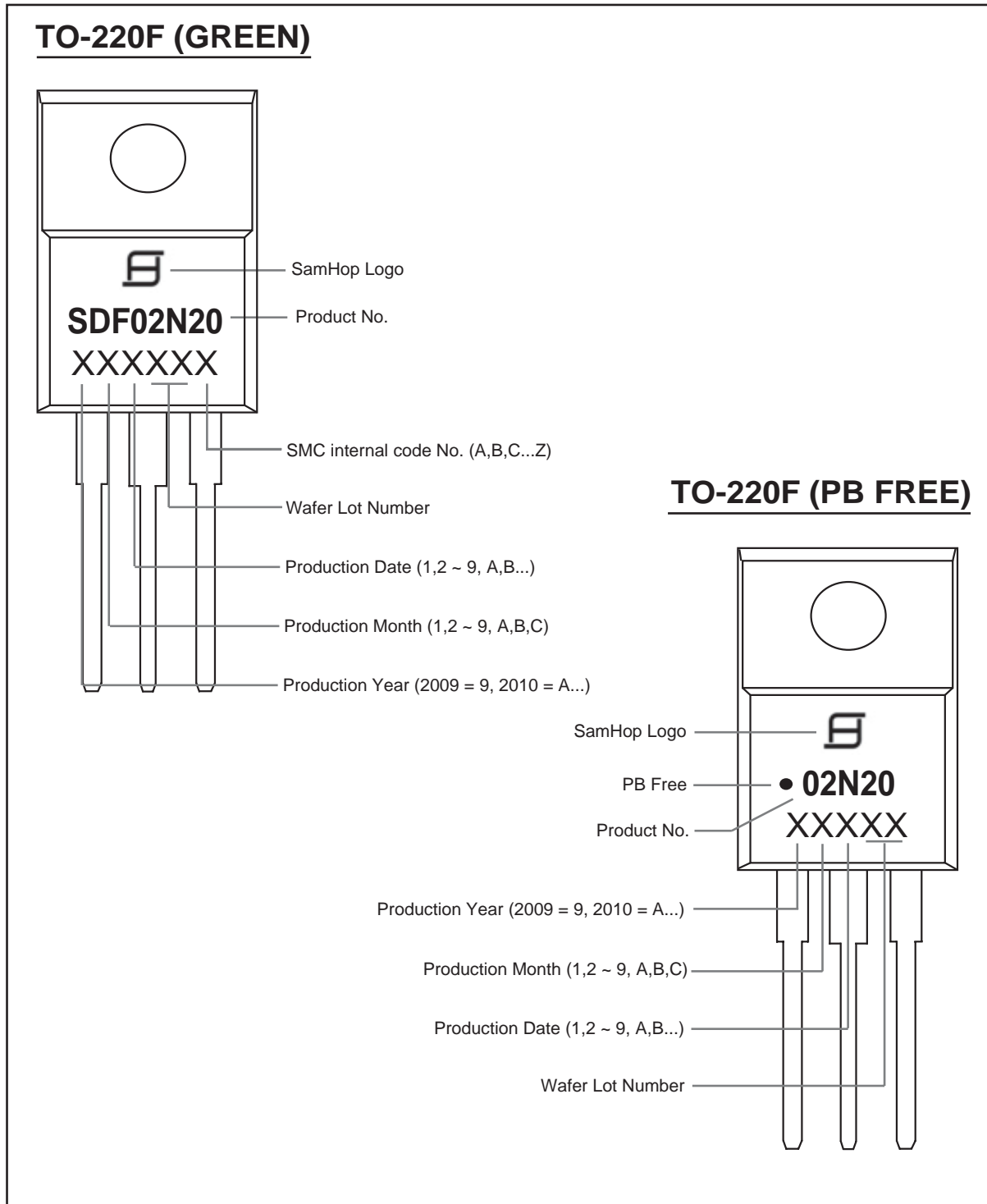
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