大唐移动
DTmobile

SDTM810 Module Specification

Rev. A

Revision History

Revision	Date	Reviser	Description
A	Apr. 2016	Taylor.Wu	Initial release

Contents

1 Introduction

1.1 Documentation overview

This document describes electrical specifications, RF specifications, function interface, mechanical information and testing conclusions of the SDTM810. With the help of this document, the users can easily and quickly use SDTM810 on their own applications.

1.2 Key features

1.21 Feature introduction

SDTM810 is a very powerful baseband module with 148 pins interface, it can supports TDD-LTE/FDD-LTE/WCDMA/DC-HSPA+/TD-SCDMA/GSM/EDGE/CDMA/EVDO. As a baseband module for Voice and data phones, smartphone/Music palyer-enabled devices and applications/camera phones/Multimedia phones/GPS for global location-based services/many other terminals,SDTM810 supports Voice-service, Data-service and many peripheral equipment, which can be supported by Qualcomm's MSM8909 platform. The module also support security solutions cloak sensitive data under multiple layers of advanced physical security to provide the most secure key storage possible. It includes all the essential functions of mobile POS terminal including a cryptographic engine, a true random number generator, battery-backed RTC, environmental and tamper detection circuitry, a magnetic stripe reader, a smart card controller with embedded transceiver to directly support 1.8V, 3.3V, and 5V cards, and an integrated secure keypad controller.

1.22 Summary of features

SDTM810 features are listed on the following table (**Table1-1**)

Table1-1 SDTM810 features

Feature	Capability
Processors	
Processors	■ Qualcomm MSM8909:Quad-ARM® Cortex™-A7 application processors up to 1.094GHz + 512KB L2 cache ■ Modem system: QDSP6 v5 core at up to 691MHz 768 kB L2 caches Support for Single Radio LTE(SRLTE) Dual SIM Dual Standby(DSDS) ■ RPM system :Cortex-M3 for the RPM
Memory support	
System memory via EBI	■ 1x LPDDR3 SDRAM; 32-bit wide; up to 533 MHz ■ 1GB,support up to 2GB
External memory via SDC1	■ eMMC v4.5/SD flash devices ■ 8GB, support up to 16GB.

RF support	
RF operating bands	■ GSM Three Band 850/900/1800; ■ WCDMA Band1/3/5; ■ CDMA Evdo Rev.A 800MHz; ■ TD-SCDMA Band 34/Band 39
	■ TDD-LTE Band38/39/40/41
	■ FDD-LTE Band1/Band 3
Air interfaces ■ GSM ■ WCDMA ■ CDMA ■ TD-SCDMA ■ FDD-LTE ■ TDD-LTE	 ■ GSM 900/850/DCS/GPRS ■ WCDMA HSDPA, HSUPA, HSPA+, DC-HSPA+ DL 42Mbps/ UL 5.76Mbps ■ CDMA REVA, REVB DO: DL 3.1Mbps/ UL 1.8Mbps 1x: DL / UL 307.2kbps ■ TD-SCDMA : DL 2.8Mbps/ UL 2.2Mbps ■ Cat 4 ■ Cat 4
GNSS – GPS One engine	■ Gen 8C ■ GPS, Beidou , Glonass
Multimedia	
Display interfaces ■ MIPI_DSI ■ General display features	One ■ 4-lane – 1.5 Gbps per lane; WVGA, up to HD(720p), 60fps ■ Color depth – 24-bit pp(RGB888) ■ Panel types – Most MIPI DSI compliant panels supported;
Camera interfaces ■ Number of CSIs ■ Primary (CSI0) ■ Secondary (CSI1) ■ Configurations supported	■ Two; 1.5 Gbps per lane ■ 2-lane MIPI_CSI0； supports CMOS and CCD sensors Up to 8MP sensors ■ 1-lane MIPI_CSI1;webcam support 3MP ■ I2C controls
Video applications performance	■Encode: H.264 BP/MP – HD(720p),30 fps MPEG-4 SP/H.263P0 –WVGA, 30 fps VP8 – WVGA, 30 fps ■ Encode: H.264 BP/MP/HP – 1080p, 30 fps MPEG-4 SP/ASP – 1080p, 30 fps DivX 4x/5x/6x – 1080p, 30 fps H.263 P0 – WVGA, 30 fps VP8 – 1080p, 30 fps (HEVC) H.265 MP 8 bit–1080p, 30 fps
Graphics	■ Adreno 304; up to 400 MHz 3D graphics accelerator
Audio	
Codec ■ Low-power audio ■ Voice codec support	Integrated within the MSM8909 device ■ Low power audio for mp3 and AAC playback; surround sound ■ Versatile – many audio playback & voice modes; encoders

■ Audio codec support ■ Enhanced audio ■ Synthesizer	for audio; many concurrency modes ■ G711; Raw PCM; QCELP; EVRC, -B, -WB; AMR-NB, -WB; GSM-EFR, -FR, -HR; ■ MP3; AAC+, eAAC; AMR-NB, -WB, G.711, WMA 9/10 Pro ■ Dolby Digital Plus and DTS-HD surround Fluence Noise Cancellation； QAudioFX/Qconcert/QEnsemble; 128-voice polyphony wavetable
Audio inputs	■ Up to 3 analog microphones, with integrated MIC bias
Audio outputs	■ Four outputs: Earpiece Mono AB Headphones Stereo AB 800mW CLASS-D
Connectivity	
BLSP ports ■ UART ■ I2C ■ SPI (master only)	6,4 at 4-bits each, 2 at 2-bits each; multiplexed serial interface functions ■ Yes – One ports up to 4 Mbps ■ Yes – cameras, sensors, NFC, SMB charger, etc. ■ Yes – cameras, sensors, etc.
USB interface	■ One USB 2.0 high-speed
UIM interface	■ Two – dual voltage (1.8 V/2.85 V)
Secure digital interfaces	■ Up to two ports, both dual-voltage ■ One 8-bit and one 4-bit ■ SD 3.0; SD/MMC card; eMMC v4.5
Wireless connectivity ■ WLAN ■ Bluetooth	With WCN3610 ■ WCN3610 : 802.11 b/g/n , 2.4G ■ Optional: WCN3660B 802.11 a/b/g/n ■ BT 4.0 LE and earlier
Touch screen support	■ Capacitive panels via external IC (I2C, SPI, & interrupts)
TDB	

1.3 Block diagram

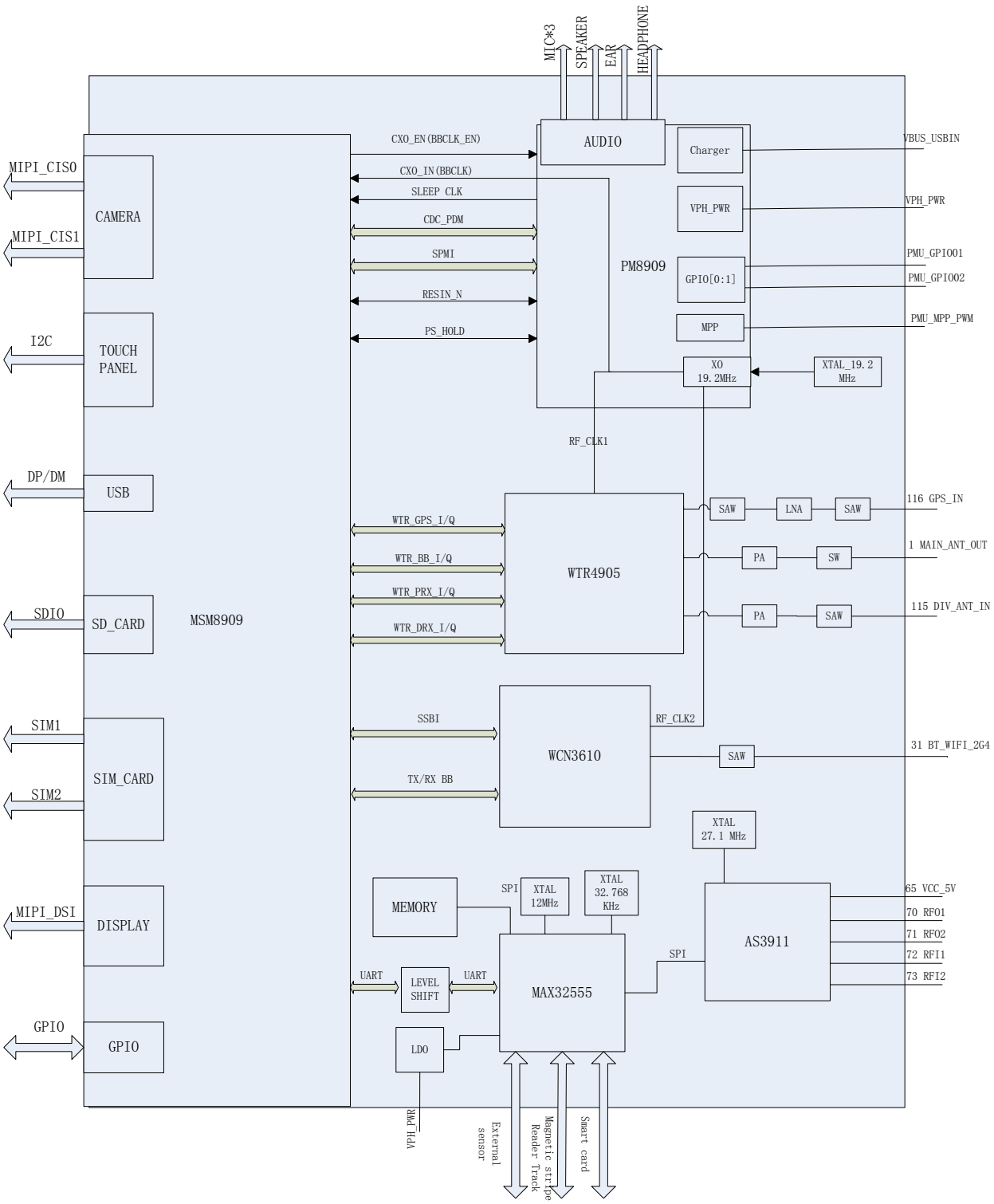


Figure1-2 SDTM810 functional block diagram

1.4 Terms and acronyms

Table1-2 Terms and acronyms

Term	Definition
ADC	Analog-to-digital converter
BER	Bit error rate
bps	Bits per second
BT	Bluetooth
CDMA	Code division multiple access
CRC	Cyclic redundancy code
CSI	Camera serial interface
CTP	Capacitive touch panel
DAC	Digital-to-analog converter
DBHSPA	Dual-band HSPA
DC-HSPA+	Dual-carrier HSPA+
DCUPA	Dual-carrier HSPA
DDR	Double data rate
DMB	Digital mobile broadcast
DRM	Digital Rights Management
DSI	Display serial interface
DSP	Digital signal processor
EBI	External bus interface
EDGE	Enhanced data rates for GSM evolution
EDR	Enhanced data rate
ETB	Embedded trace buffer
QDSS	Embedded trace macrocell
EV-DO	Evolution data optimized
FDD	Frequency division duplex
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPRS	General packet radio services
GPS	Global positioning system
GPU	Graphics processing unit
GRFC	Generic RF controller
GSM	Global system for mobile communications
HDCP	High-bandwidth digital content protection
HSDPA	High-speed downlink packet access
HSIC	High-speed inter-chip
HSPA+	High-speed packet access
HSUPA	High-speed uplink packet access
I2C	Inter-integrated circuit
I2S	Inter-IC sound
ISP	Image signal processing
kbps	kilobits per second

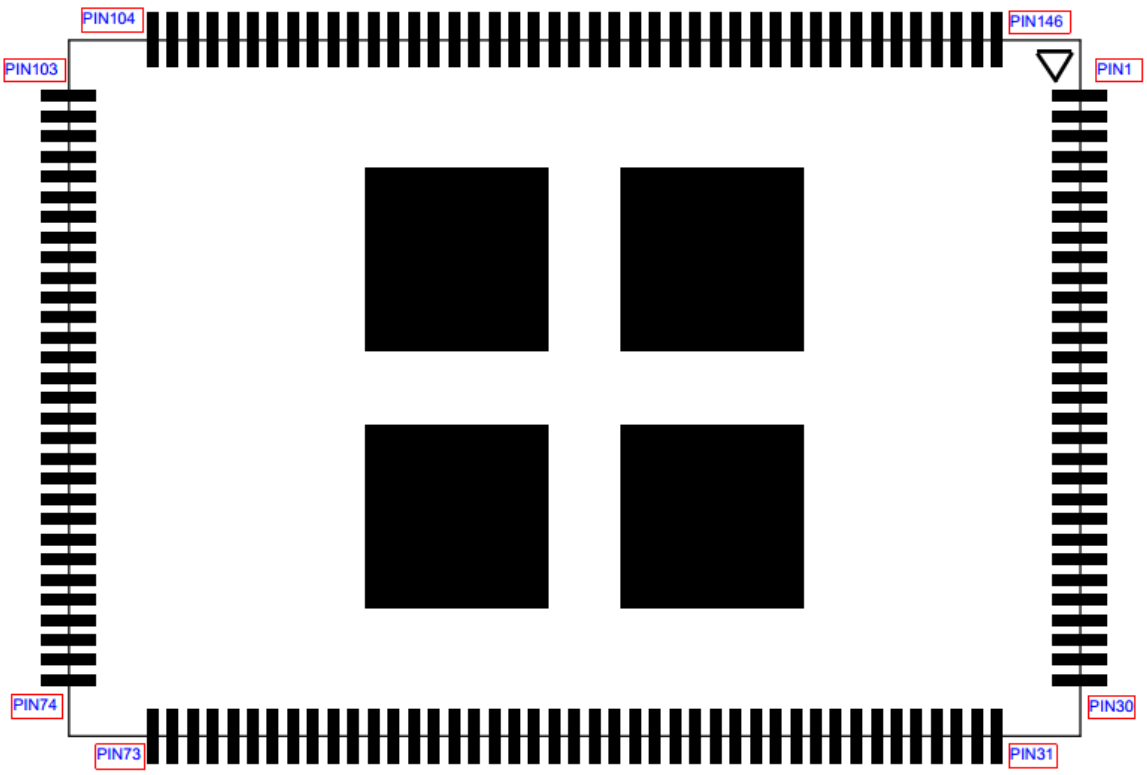
Table1-2 Terms and acronyms (cont.)

Term	Definition
LCD	Liquid crystal display
LPDDR	Low-power DDR
LTE	Long term evolution
MBP	Mobile broadcast platform
MIPI	Mobile industry processor interface
PA	Power amplifier
PCM	Pulse-coded modulation
PI	Power in
PDM	Pulse-density modulation
PM	Power management
PO	Power out
RDS	Radio data system
RPM	Resource power manager
SBI	Serial bus interface
SD	Secure digital
SDC	Secure digital controller
SIM	Subscriber identity module
SPI	Serial peripheral interface
TBD	To be discussed
TCXO	Temperature-compensated crystal oscillator
TDD	Time division duplexing
TSIF	Transport stream interface
UART	Universal asynchronous receiver transmitter
UICC	Universal integrated circuit card
UIM	User identity module
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
USIM	UMTS subscriber identity module
WCDMA	Wideband code division multiple access
WCN	Wireless connectivity network
WLAN	Wireless local area network
WTR	Wafer-scale RF transceiver
XO	Crystal oscillator
ZIF	Zero intermediate frequency

2 Interface Definitions

2.1 Interface configuration

TOP view



BOTTOM view

Figure2-1 SDTM810 pin assignments

2.2 Pin definitions

Table2-1 SDTM810 Pin definitions

Pin#	Pad name	Function	Pad characteristics	Functional description
1	MAIN_ANT_OUT		AO	RF signal
2	GND		GND	GND
3	SCAM_RST_N	GPIO_28	DO;B-PD:nppukp	Web camera (front camera) reset Configurable I/O
4	CAM_MCLK1	GPIO_27	DO;B-PD:nppukp	Camera master clock Configurable I/O
5	MIPI_CSI1_LN0_P	CSI_MIPI	AI, AO	MIPI camera serial interface 1 lane 0 – positive
6	MIPI_CSI1_LN0_N		AI, AO	MIPI camera serial interface 1 lane 0 – negative
7	MIPI_CSI1_CLK_P		AI	MIPI camera serial interface 1 clock – positive
8	MIPI_CSI1_CLK_N		AI	MIPI camera serial interface 1 clock – negative
9	MIC3_IN	Audio	AI	Microphone 3 input, single-ended
10	MIC2_IN		AI	Microphone 2 input, single-ended
11	HS_DET		DI	Headset detection
12	SPKR_DRV_M		AO	Speaker driver output, minus
13	SPKR_DRV_P		AO	Speaker driver output, plus
14	EARO_M		AO	Earpiece amplifier output, differential minus
15	EARO_P		AO	Earpiece amplifier output, differential plus
16	MIC_GND			
17	MIC1_IN		AI	Microphone 1 input, single-ended
18	MIC_BIAS1		AO	Microphone bias output voltage
19	HPH_R		AO	Headphone right output
20	HPH_REF		AI	Headphone driver amplifier ground reference
21	HPH_L		AO	Headphone left output
22	GPIO_14	GPIO_14	DO;B-PD:nppukp	Configurable I/O;,SPI,or I2C BLSP#4

Pin#	Pad name		Pad characteristics	Functional description
23	GPIO_15	GPIO_15	DO;B-PD:nppukp	Configurable I/O: SPI,or I2C BLSP#4
24	GPIO_6/ UART_CTS_N	GPIO_6	B-PD:nppukp	Configurable I/O UART,SPI,or I2C BLSP#1
25	GPIO_7/ UART_RFR_N	GPIO_7	B-PD:nppukp	Configurable I/O UART,SPI,or I2C BLSP#1
26	GPIO_4/ UART_TX	GPIO_4	B-PD:nppukp	Configurable I/O UART, SPI, BLSP#1
27	GPIO_5/ UART_RX	GPIO_5	B-PD:nppukp	Configurable I/O UART, SPI, BLSP#1
28	GPIO_111/ UART_CTS_N/SDA	GPIO_111	DOB-PD:nppukp	Configurable I/O UART,SPI,or I2C BLSP#2
29	GPIO_112/ UART_CTS_N/SCL	GPIO_112	DOB-PD:nppukp	Configurable I/O UART,SPI,or I2C BLSP#2
30	NC	-	-	-
31	WIFI_BT_RF	-	AO	RF signal input
32	GND		GND	GND
33	TS_INT_N	GPIO_13	DI;B-PD:nppukp	Configurable I/O Touchscreen interrupt
34	TS_I2C_SDA	GPIO_18	B;B-PD:nppukp	Configurable I/O Touchscreen I2C
35	TS_I2C_SCL	GPIO_19	B;B-PD:nppukp	Configurable I/O Touchscreen I2C
36	TS_RST_N	GPIO_12	DO;B-PD:nppukp	Configurable I/O Touchscreen reset
37	SD_CARD_DET__N	GPIO_38	B-PD:nppukp	Configurable I/O Secure digital card detection
38	KYPD_SNS0	GPIO_90	BD;OB-PD:nppukp	Keypad sense bit 0 Configurable I/O
39	KYPD_SNS1	GPIO_91	B;B-PD:nppukp	Keypad sense bit 1 Configurable I/O
40	KYPD_SNS2	GPIO_92	DI;B-PD:nppukp	Keypad sense bit 2 Configurable I/O
41	GND	-	-	GND
42	USB_DM	USB	AI, AO	USB data – minus
43	USB_DP		AI, AO	USB data – plus
44	GND	-	-	GND
45	SDC2_CMD	SD CARD	BH-PD:nppukp	Secure digital controller 2 command

Table2-1 SDTM810 Pin definitions(cont.)

Pin#	Pad name		Pad characteristics	Functional description
46	SDC2_DATA_0	SD CARD	BH-PD:nppukp	Secure digital controller 2 data bit 0
47	SDC2_DATA_1		BH-PD:nppukp	Secure digital controller 2 data bit 1
48	SDC2_DATA_2		BH-PD:nppukp	Secure digital controller 2 data bit 2
49	SDC2_DATA_3		BH-PD:nppukp	Secure digital controller 2 data bit 3
50	SDC2_CLK		BH-NP:pdpukp	Secure digital controller 2 clock
51	VREG_L11_SDC	POWER	PO	Output 2.95V
52	GPIO_29	GPIO_29	B-PD:nppukp	Configurable I/O
53	GPIO_30	GPIO_30	B-PD:nppukp	Configurable I/O
54	UIM2_PRESENT	UIM1	DI,B-PD:nppukp	Configurable I/O UIM2 removal detection
55	UIM2_DATA		B,B-PD:nppukp	Configurable I/O UIM2 data
56	UIM2_CLK		DO,B-PD:nppukp	Configurable I/O UIM2 clock
57	UIM2_RST		DO,B-PD:nppukp	Configurable I/O UIM2 reset
58	UIM1_DATA	UIM2	B,B-PD:nppukp	Configurable I/O UIM1 data
59	UIM1_CLK		DO,B-PD:nppukp	Configurable I/O UIM1 clock
60	UIM1_RST		DO,B-PD:nppukp	Configurable I/O UIM1 reset
61	UIM1_PRESENT		DI,B-PD:nppukp	Configurable I/O UIM2 removal detection
62	GND	-	-	GND
63	VREG_L14_UIM1	POWER	PO	POWER for UIM1
64	USB_HS_ID	USB	AI	USB HS ID
65	VCC_5V	POWER	PI	POWER for NFC
66	MAX_VBAT	POWER	PI	Back battery for secure circuit
67	ADC0	ADC	AI	ADC for back battery
68	TCLK6	GPIO	DI,DO	GPIO(3.3V)
69	GND	-	-	GND
70	RFO1	NFC	AO	RF Antenna Output 1

Table2-1 SDTM810 Pin definitions(cont.)

Pin#	Pad name		Pad characteristics	Functional description
71	RFO2	NFC	AO	RF Antenna Output 2
72	RFI1		AI	RF Antenna Input 1
73	RFI2		AI	RF Antenna Input 2
74	VREG_L15	UIM2 POWER	PO	POWER for UIM2
75	EXTS1_OUT	External Tamper sensor	AO	External Sensor1 Output
76	EXTS0_IN		AI	External Sensor0 Input
77	EXTS2_OUT		AO	External Sensor2 Output
78	EXTS3_IN		AI	External Sensor3 Input
79	EXTS0_OUT		AO	External Sensor0 Output
80	EXTS2_IN		AI	External Sensor2 Input
81	EXTS1_IN		AI	External Sensor1 Input
82	EXTS3_OUT		AO	External Sensor3 Output
83	GND	-	-	GND
84	MCR_2P	Magnetic Stripe Reader Track	AI	Magnetic Stripe Reader Track2 Positive Input
85	MCR_2N		AI	Magnetic Stripe Reader Track2 Negative Input
86	MCR_3P		AI	Magnetic Stripe Reader Track3 Positive Input
87	MCR_3N		AI	Magnetic Stripe Reader Track3 Negative Input
88	MCR_1P		AI	Magnetic Stripe Reader Track1 Positive Input
89	MCR_1N		AI	Magnetic Stripe Reader Track1 Negative Input
90	SC_IO	Smart card	DI,DO	Smart Cart I/O
91	SC_VCC		PO	Power for smart card
92	SC_CLK		DO	Smart Cart CLK
93	SC_RST		DO	Smart Cart Reset
94	SC_C8		DI	Smart Cart C8
95	SC_C4		DI	Smart Cart C4
96	SC_DETECT		DI	Smart Cart Detect
97	MAX_RSTIN	-	DO	Reset of secure IC
98	PM_KYPD_PWR_N	-	DI	Power key of system
99	PM_VIB_DRV_N	-	PI	Vibration motor driver output control
100	TCLK7	GPIO	DI,DO	GPIO(3.3V)

Table2-1 SDTM810 Pin definitions(cont.)

Pin#	Pad name		Pad characteristics	Functional description
101	PMU_MPP_2_PWM	PMU CTR	AO-Z;AO	Configurable MPP; The PWM of backlight of LCM
102	GND	-	-	GND
103	PMU_GPIO01	PMU CTR	DO-Z;DI	Configurable GPIO;RF clock 1 enable
104	PM_RESIN_N	PMU CTR	DI	PMIC reset
105	PMU_GPIO02	PMU CTR	DO-Z;DI	Configurable GPIO;RF clock 2 enable
106	VREF_BAT_THERM	POWER	AO	Reference voltage for battery thermistor
107	VREG_L12_2P95V	POWER	PO	PMU supply 2.95V
108	GPIO_24	GPIO_24	B-PD:nppukp	Configurable I/O
109	VBUS_USB	POWER	PI	USB Voltage
110	VBAT_SNS	AI	PI,PO	Battery Voltage sense
111	VCOIN	POWER	PI	BACK BATTERY
112	BAT_THERM	-	DI	Battery therm monitor
113	VBAT	POWER		Battery
114	GND	-	-	GND
115	RF_IN_3	-	AI	Diversity antenna input
116	GPS_IN	-	AI	GPS signal input
117	GND	-	-	GND
118	MIPI_DSI_CLK_P	DSI_MIPI	AO	MIPI display serial interface 0 clock – positive
119	MIPI_DSI_CLK_N		AO	MIPI display serial interface 0 clock – negative
120	MIPI_DSI_LN3_P		AI, AO	MIPI display serial interface 0 lane 3 – positive
121	MIPI_DSI_LN3_N		AI, AO	MIPI display serial interface 0 lane 3 – negative
122	MIPI_DSI_LN2_P		AI, AO	MIPI display serial interface 0 lane 2 – positive
123	MIPI_DSI_LN2_N		AI, AO	MIPI display serial interface 0 lane 2 – negative

Table2-1 SDTM810 Pin definitions(cont.)

Pin#	Pad name		Pad characteristics	Functional description
124	MIPI_DSI_LN1_P	DSI_MIPI	AI, AO	MIPI display serial interface 0 lane 1 – positive
125	MIPI_DSI_LN1_N		AI, AO	MIPI display serial interface 0 lane 1 – negative
126	MIPI_DSI_LN0_P		AI, AO	MIPI display serial interface 0 lane 0 – positive
127	MIPI_DSI_LN0_N		AI, AO	MIPI display serial interface 0 lane 0 – negative
128	GPIO_8	-	B-PD: nppukp	Configurable I/O
129	VREG_L17	POWER	PO	PMU Supply 2.85V
130	GPIO_9	-	B-PD: nppukp	Configurable I/O
131	VREG_L6_1P8	POWER	OUPUT	PMU Supply 1.8V
132	CAM_I2C_SDA	GPIO_10	B	Camera I2C,SDA
133	CAM_I2C_SCL	GPIO_11	B	Camera I2C,SCL
134	CAM1_RST_N	GPIO_35	DO; B-PD :nppukp	Camera 1 (rear camera) reset; Configurable I/O
135	CAM1_STANDBY_N	GPIO_34	DO; B-PD:nppukp	Camera 1 (rear camera) standby Configurable I/O
136	GND	-	GND	GND
137	MIPI_CSI0_LN1_N	CSI_MIPI	AI, AO	MIPI camera serial interface 0 lane 1 – negative
138	MIPI_CSI0_LN1_P		AI, AO	MIPI camera serial interface 0 lane 1 – positive
139	MIPI_CSI0_LN2_P		AI, AO	MIPI camera serial interface 0 lane 2 – positive
140	MIPI_CSI0_LN2_N		AI, AO	MIPI camera serial interface 0 lane 2 – negative
141	MIPI_CSI0_CLK_N		AI	MIPI camera serial interface 0 CLK – negative
142	MIPI_CSI0_CLK_P		AI	MIPI camera serial interface 0 CLK – positive

Table2-1 SDTM810 Pin definitions(cont.)

Pin#	Pad name		Pad characteristics	Functional description
143	GPIO_33	GPIO_33	DIB-PD:nppukp	Web camera (front camera) power down
144	CAM_MCLK	GPIO_26	DOB-PD:nppukp	Camera master clock 0
145	GND		GND	GND
146	VBATT	POWER	PO	Battery

Table2-2 SDTM810 BTB (J2601) connector pin definitions

Pin#	Pad name		Pad characteristics	Functional description
1,15,16, 30	GND	-	GND	GND
2	GPIO_25	GPIO_25	B-PD:nppukp	Configurable I/O
3	GPIO_17	GPIO_17	-	Configurable I/O
4,1117,19 20,21	NC	-	-	NC
5	GPIO_31	GPIO_31	B-PD:nppukp	ConfigurableI/O,CCI_TIMER0, GP_CLK0
6	GPIO_32	GPIO_32	B-PD:nppukp	Configurable I/O,CCI_TIMER1, GP_CLK1 or I2C
7	GPIO_74	GPIO_74	B-PD:nppukp	Configurable I/O
8	GPIO_58	GPIO_58	B-PD:nppukp	Configurable I/O,#SMB_INT#
9	GPIO_93	GPIO_93	BB-PD:nppukp	Configurable I/O
10	GPIO_94	GPIO_94	BB-PD:nppukp	Configurable I/O
12	GPIO_96	GPIO_96	BB-PD:nppukp	Configurable I/O
13	GPIO_97	GPIO_97	BB-PD:nppukp	Configurable I/O
14	GPIO_11 0	GPIO_110	BB-PD:nppukp	Configurable I/O
18	GPIO_73	GPIO_73	BB-PD:nppukp	Configurable I/O
22	GPIO_98	GPIO_98	BB-PD:nppukp	Configurable I/O
23	GPIO_16	GPIO_16	BB-PD:nppukp	Configurable I/O
24	GPIO_3	GPIO_3	BB-PD:nppukp	Configurable I/O
25	GPIO_2	GPIO_2	BB-PD:nppukp	Configurable I/O
26	GPIO_1	GPIO_1	BB-PD:nppukp	Configurable I/O
27	GPIO_0	GPIO_0	BB-PD:nppukp	Configurable I/O
28	GPIO_23	GPIO_23	BB-PD:nppukp	Configurable I/O
29	GPIO_22	GPIO_22	BB-PD:nppukp	Configurable I/O

Table2-2 SDTM810 BTB (J2701) pin definitions

Pin#	Pad name		Pad characteristics	Functional description
1	KBD0	Keyboard	AI	Secure Keyboard I/O 0
2	KBD1		AI	Secure Keyboard I/O 1
3	KBD2		AI	Secure Keyboard I/O 2
4	KBD3		AI	Secure Keyboard I/O 3
5	KBD4		AI	Secure Keyboard I/O 4
6	KBD5		AI	Secure Keyboard I/O 5
7	KBD6		AI	Secure Keyboard I/O 6
8	KBD7		AI	Secure Keyboard I/O 7
9	MAX_SCL			MAX32555 I2C SCL(Reserve)
10	MAX_SDA			MAX32555 I2C SDA(Reserve)
11,27	GND			GND
12	RXD0	UART0		For debug, UART 0 Data Input
13	TXD0			For debug, UART 0 Data Output
14	RTS0			For debug, UART 0 Request To Send
15	CTS0			For debug, UART 0 Clear To Send
16	CTS2	UART2		Reserve ,UART 2 Clear To Send
17	RTS2			Reserve ,UART 2 Request To Send
18	TXD2			Reserve, UART 2 Data Output
19	RXD2			Reserve ,UART 2 Data Input
20	SC_CLK_BYP	SC CARD BYPASS		Smart card clk bypass
21	SC_DETECT_BYP			Smart card detect bypass
22	SC_IO_BYP			Smart IO bypass
23	SC_RST_BYP			Smart reset bypass
24	VBUS_DET	USB for debug		Reserve for debug
25	MAX_USB_DP			USB DP of MAX32555,Reserve for debug
26	MAX_USB_DM			USB DP of MAX32555,Reserve for debug
28	MAX_VBAT	POWER		Back battery for secure circuit
29,30	VDD_3V3	POWER		POWER for debug

3 Electrical Specifications

(TBD)

4 Application Interface Specifications

4.1 Power interface

The power supply of SDTM810 comes from PM8909. See **Table4-1**

Table4-1 Power source description

Signal	Pin#	Direction	Voltage(V)			Current(mA)		
		PI/PO	Min	Typ	Max	Min	Typ	Max
VREG_L11_2P95V	51	PO	TBD	2.95	TBD	TBD	600	TBD
VREG_L14_UIM1	63	PO	TBD	1.8/2.85	TBD	TBD	55	TBD
VREG_L15_UIM2	74	PO	TBD	1.8/2.85	TBD	TBD	55	TBD
VREG_L12_2P95V	107	PO	TBD	1.8/2.95	TBD	TBD	50	TBD
VREG_L17_2P85V	129	PO	TBD	2.85	TBD	TBD	420	TBD
VREG_L6_1P8V	131	PO	TBD	1.8	TBD	TBD	200	TBD

4.2 PMIC GPIO and MPP interface

SDTM810 have two PMIC GPIO interface and one PMIC Multipurpose interface.
See **Table4-2**.

Table4-2 PMIC GPIO and MPP interface description

GPIO/MPP	Pin#	Functions
PMU_GPIO01	103	RFCLK1_EN
PMU_GPIO02	105	RFCLK2_EN
PMU_MPP_2_PWM	101	PWM output

Two GPIOs are available. Some likely GPIO applications, which are described elsewhere: clock outputs; external current driver control; external LDO, SMPS, or power gate controls; status bit; XO controller input; and level translator.

One MPP are available. MPP can be configured as PWM, and MPP can be configured as analog output buffers.

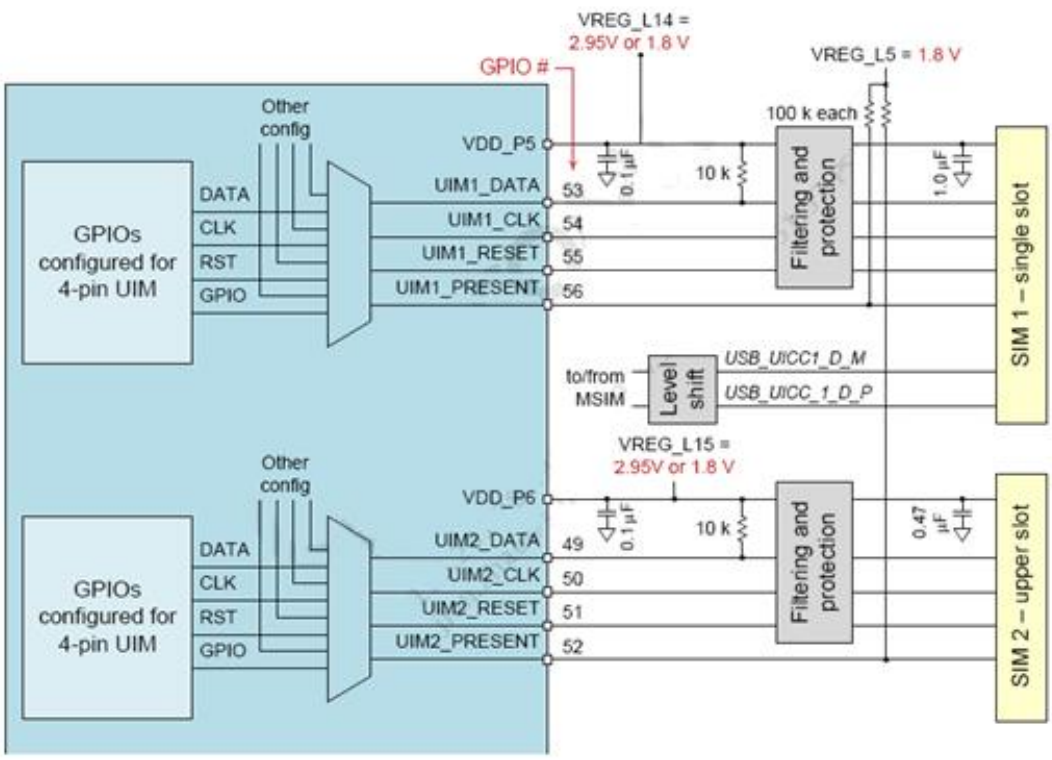
4.3 UIMs interface

There are TWO UIM interfaces on SDTM810. The UIM provides the required subscription verification information to allow the equipment to attach to network.
See Table4-3 and Figure4-1for more details.
- Data rates up to 4 MHz (in Fast mode+)
- Dual-voltage 1.8 or 2.85 V support

Table4-3 UIMs interface description

Signal	Pin#	Description	Direction	Voltage(V)	
			I/O	1.8	2.85
VREG_L14_UIM1	63	Variable supply voltage for external UIM/SIM	O	1.8	2.85
VREG_L15_UIM2	74	Variable supply voltage for external UIM/SIM	O	1.8	2.85
UIM1_PRESENT	61	External UIM/SIM removal detection signal	O	TBD	TBD
UIM1_RESET	60	External UIM/SIM reset signal	O	1.8	2.85
UIM1_CLK	59	External UIM/SIM clock signal	O	1.8	2.85
UIM1_DATA	58	External UIM/SIM data signal	I/O	1.8	2.85
UIM2_PRESENT	54	External UIM/SIM removal detection signal	O	TBD	TBD
UIM2_RESET	57	External UIM/SIM reset signal	O	1.8	2.85
UIM2_CLK	56	External UIM/SIM clock signal	O	1.8	2.85
UIM2_DATA	55	External UIM/SIM data signal	I/O	1.8	2.85

Figure4-1 UIM application diagram



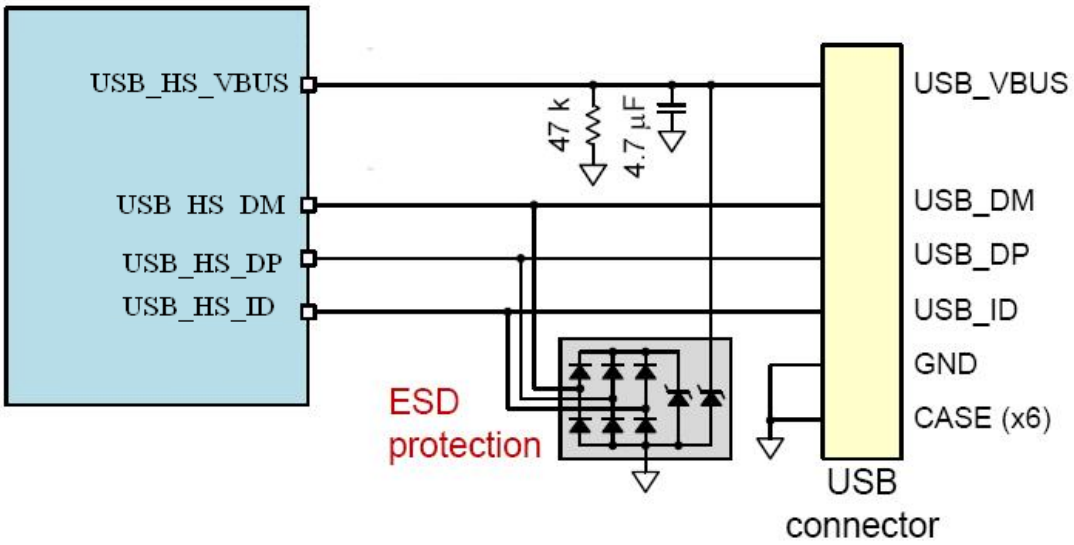
4.4 USB interface

SDTM810 contains a USB interface. It is compliant with the USB2.0 specification. The USB2.0 specification requires hosts to support all three USB speeds, low-speed (1.5Mbps), full-speed (12Mbps) and high-speed (480Mbps).
See Table4-4 and Figure4-2 for more details.

Table4-4 USB interface description

Signal	Pin#	Description	Direction
USB_DM	42	USB 2.0 serial data minus	AI/**A**O
USB_DP	43	USB 2.0 serial data plus	AI/**A**O
USB_HS_ID	64	USB HS ID	AI
VBUS_USBIN	109	USB_IN	POWER

Figure4-2 USB application diagram



4.5 Audio interface

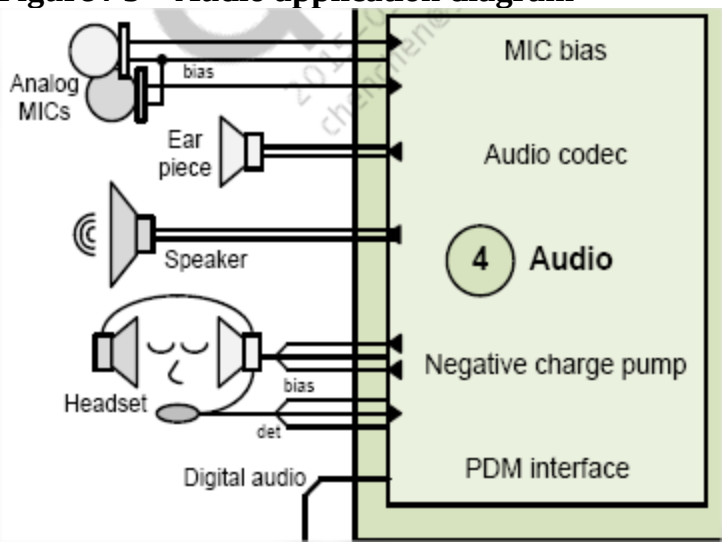
- Codec integrated within PMU
- No SLIMBUS
- No digital mic support
- Audio inputs: Up to three analog micphones, with integrated mic bias;
- Audio output : Headphones with headset detection; Differential earpiece; Differential loud speaker driver; Single-ended line output

See Table4-5 and Figure4-3for more details.

Table4-5 Audio interface description

Signal	Pin#	Description	Direction
			AI/**A**O
MIC3_IN	9	Secondary input, single-ended	AI
MIC2_IN	10	Headset mic input, single-ended	AI
HS_DET	11	Headset detection	DI
SPKR_DRV_M	12	Speaker driver output, minus	AO
SPKR_DRV_P	13	Speaker driver output, plus	AO
EARO_M	14	Earpiece amplifier output, differential minus	AO
EARO_P	15	Earpiece amplifier output, differential plus	AO
MIC_GND	16	GND	GND
MIC1_IN	17	Primary MIC input, single-ended	AI
MIC_BIAS	18	Microphone bias output voltage	AO
CDC_HPH_R	19	Headphone right output	AO
CDC_HPH_REF	20	Headphone driver amplifier ground reference	AI
CDC_HPH_L	21	Headphone left output	AO

Figure4-3 Audio application diagram



4.6 Camera interface

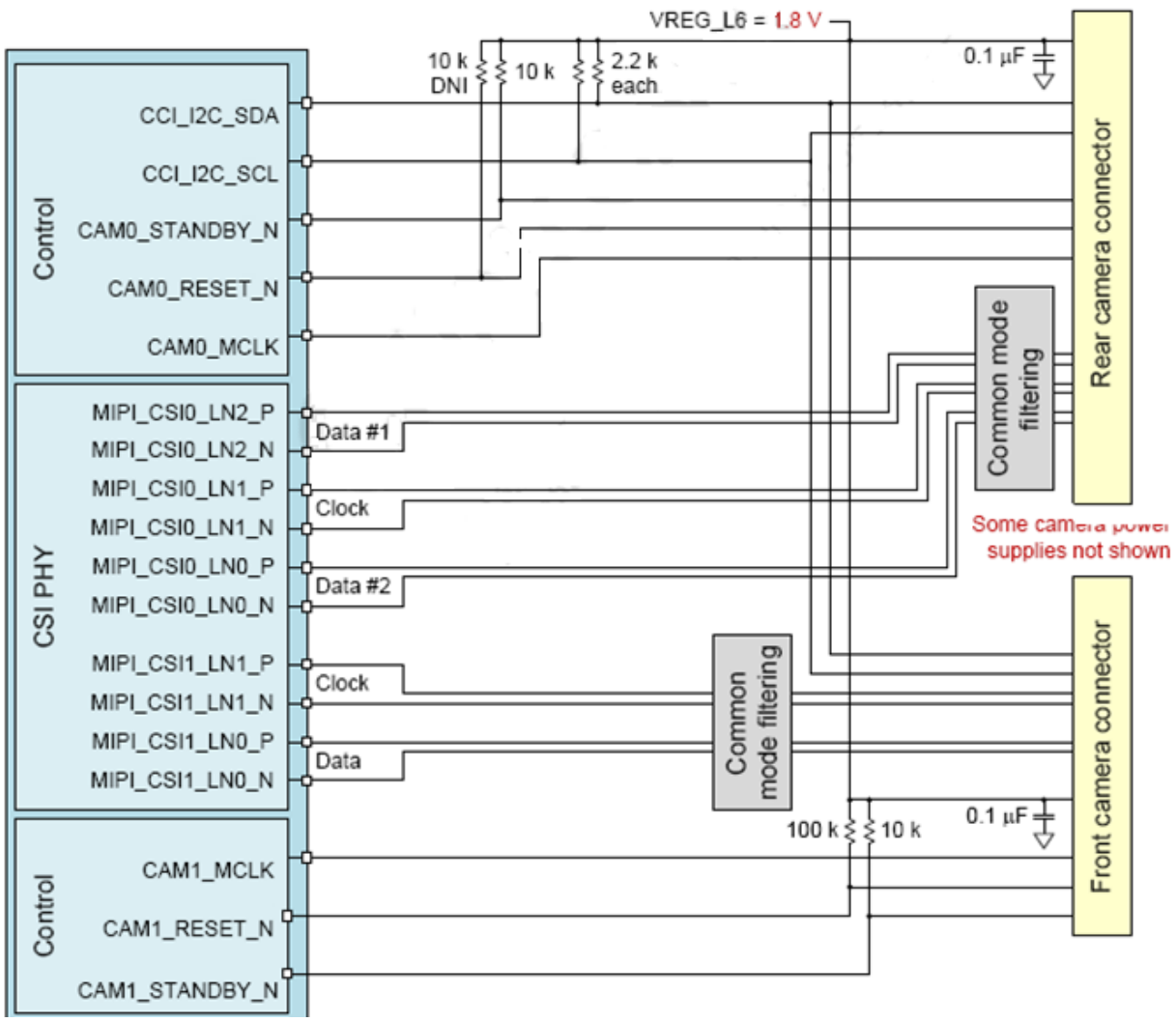
SDTM810 contains two camera interface. Primary camera interface use 2-lane MIPI_CSI0, supports CMOS and CCD sensors, up to 8MP sensors. Secondary camera interface use 1-lane MIPI_CSI1, and 1.5Gbps per lane. Both are controlled by I2C bus.
See Table4-6 and Figure4-4for more details.

Table4-6 Camera interface description

Signal	Pin#	Description	Direction
			AI/**A**O
SCAM_RST_N	3	Camera1 (front camera) reset	DO
SCAM_MCLK1	4	Camera1 master clock 1	DO
MIPI_CSI1_LN0_P	5	MIPI camera serial interface 1 lane 0 – positive	AI**,A**O
MIPI_CSI1_LN0_N	6	MIPI camera serial interface 1 lane 0 – negative	AI, AO
MIPI_CSI1_CLK_P	7	MIPI camera serial interface 1 clock – positive	AI

MIPI_CSI1_CLK_N	8	MIPI camera serial interface 1 clock – negative	AI
GPIO_33	143	Camera1 PWDN	DO
CAM_I2C_SDA	132	Camera I2C,SDA	B
CAM_I2C_SCL	133	Camera I2C,SCL	B
CAM1_RST_N	134	Camera 1 (rear camera) reset	DO
CAM1_STANDBY_N	135	Camera 1 (rear camera) standby	DO
MIPI_CSI0_LN1_N	137	MIPI camera serial interface 0 clock – negative	AI,AO
MIPI_CSI0_LN1_P	138	MIPI camera serial interface 0 clock – positive	AI,AO
MIPI_CSI0_LN2_P	139	MIPI camera serial interface 0 lane 2 – positive	AI,AO
MIPI_CSI0_LN2_N	140	MIPI camera serial interface 0 lane 2 – negative	AI,AO
MIPI_CSI0_CLK_N	141	MIPI camera serial interface 0 clock – negative	AI
MIPI_CSI0_CLK_P	142	MIPI camera serial interface 0 clock – positive	AI
CAM_MCLK0	144	Camera1 master clock 0	DO

Figure4-4 CSI application diagram



Normally, camera need 2.85V and 1.8V voltage, we can use external LDO to replace VREG_L6_1P8 and VERG_L17_2P85.At the same time, if the rear camera have AF function, another external LDO is necessary.

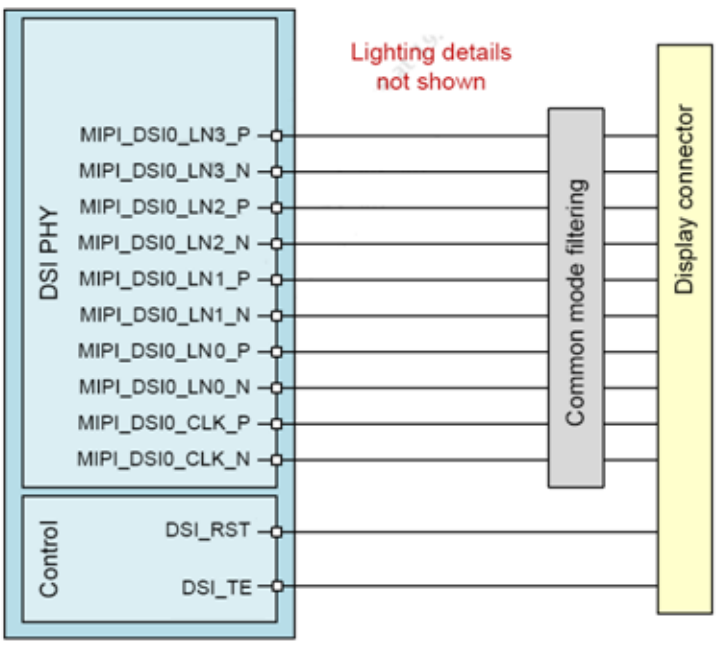
4.7 Display interface

SDTM810 contains one display interface. The interface use MIPI display serial interface, support up to four lanes. Support for the resolution of WVGA, qHD and 720p LCM..
The backlight circuit is not contained in SDTM810, which must be designed in external circuit. See Table4-7 and Figure4-5for more details.

Table4-7 Display interface description

Signal	Pin#	Description	Direction AI/AO
GPIO_24	108	DSI_TE,LCD data write sync signal	DO
PMU_MPP_2_WM	101	The PWM of backlight of LCM	DO
MIPI_DSI_CLK_P	118	MIPI display serial interface 0 clock – positive	AO
MIPI_DSI_CLK_N	119	MIPI display serial interface 0 clock – negative	AO
MIPI_DSI_LN3_P	120	MIPI display serial interface 0 lane 3 – positive	AI,AO
MIPI_DSI_LN3_N	121	MIPI display serial interface 0 lane 3 –negative	AI,AO
MIPI_DSI_LN2_P	122	MIPI display serial interface 0 lane 2 – positive	AI,AO
MIPI_DSI_LN2_N	123	MIPI display serial interface 0 lane 2 – negative	AI,AO
MIPI_DSI_LN1_P	124	MIPI display serial interface 0 lane 1 – positive	AI,AO
MIPI_DSI_LN1_N	125	MIPI display serial interface 0 lane 1 – negative	AI,AO
MIPI_DSI_LN0_P	126	MIPI display serial interface 0 lane 0 – positive	AI,AO
MIPI_DSI_LN0_N	127	MIPI display serial interface 0 lane 0 – negative	AI,AO
GPIO_8	128	LCD RESET, low level is active	B-PD:nppukp

Figure4-5 Display application diagram



4.8 CTP interface

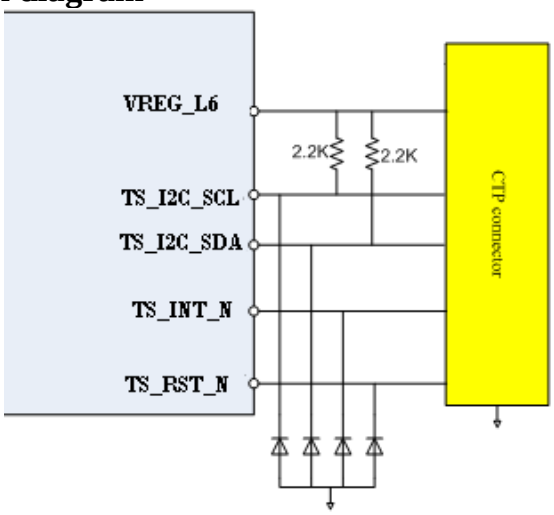
SDTM810 contains one CTP interface, the panel is controlled by I2C bus.

See Table4-8 and Figure4-6 for more details.

Table4-8 CTP interface description

Signal	Pin#	Description	Direction
			AI/AO
TS_INT_N	33	Touchscreen interrupt	DI
TS_I2C_SDA	34	Touchscreen I2C,SDA	B
TS_I2C_SCL	35	Touchscreen I2C,SCL	B
TS_RST_N	36	Touchscreen reset	DO

Figure4-6 CTP application diagram



4.9 SD interface

SDTM810 contains a SD interface, the clock output up to 200MHz,need support 1.8/2.95V dual-voltage. If SD connector have detect pin, the hot plug function can be done.
See Table4-9 and Figure4-7 for more details.

Table4-9 CTP interface description

Signal	Pin#	Description	Direction
			AI/AO
SD_CARD_DET__N	37	Secure digital card detection	DI
SDC2_CMD	45	Secure digital controller 2 command	AI,AO
SDC2_DATA_0	46	Secure digital controller 2 data bit 0	AI,AO
SDC2_DATA_1	47	Secure digital controller 2 data bit 1	AI,AO
SDC2_DATA_2	48	Secure digital controller 2 data bit 2	AI,AO
SDC2_DATA_3	49	Secure digital controller 2 data bit 3	AI,AO
SDC2_CLK	50	Secure digital controller 2 clock	AI,AO

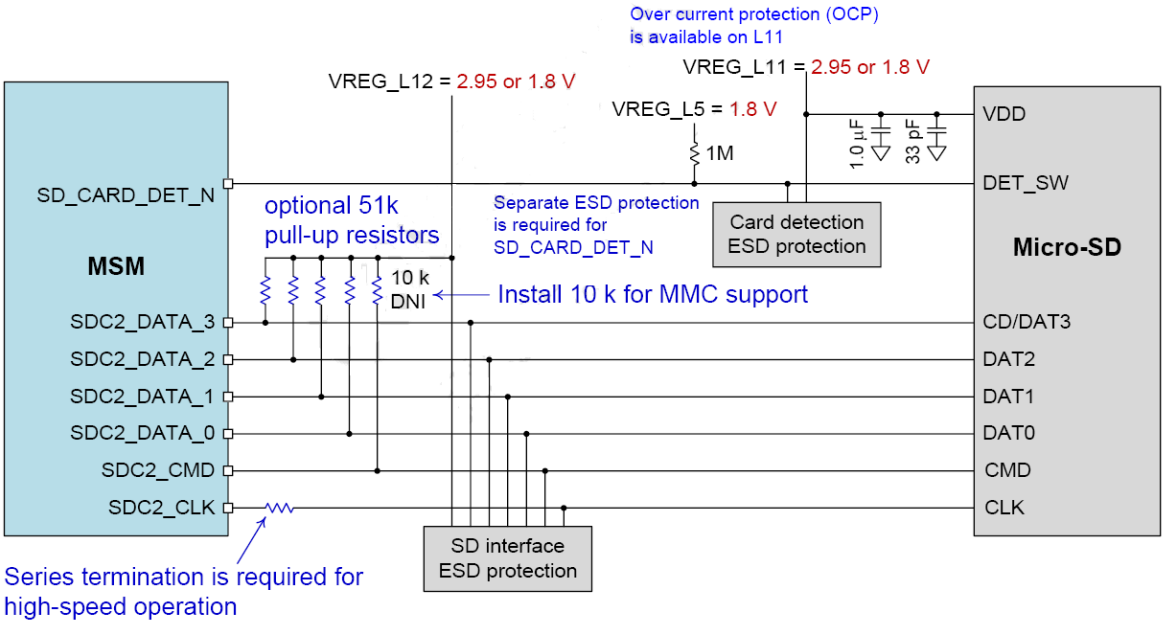


Figure4-6 SD interface application diagram

4.10 Sensors interface

SDTM810 support many sensors via I2C bus, the circuit structure is similar to camera interface. SDTM810 does not contain necessary pull_up resistors internal, which must be designed in external circuit.

4.11 Side keys interface

SDTM810 contains a few keys interfaces, which can be used as functional side keys. KYPD_SNS0,KYPD_SNS1and KYPD_SNS2 can compose matrix keyboard, also can be used as normal configurable GPIO.
See Table4-10 for more details.

Table4-10 Side keys interface description

Signal	Pin#	Description	Direction
			DI/DO
KYPD_SNS0	38	Keypad sense bit 0	DI
KYPD_SNS1	39	Keypad sense bit 1	DI
KYPD_SNS2	40	Keypad sense bit 2	DI
PM_KYPD_PWR_N	98	Power on key	DI
PM_RESIN_N	104	PMIC reset input	DI

4.12 Battery connector interface

SDTM810 must be provided voltage by external voltage source.
See Table4-11 for more details.

Table4-11 Battery connector description

Signal	Pin#	Description	Direction
			AI/AO
BAT_THERM	106	Battery therm monitor	AI
VBATT	113,146	Battery power supply	AI
GND	2,32,41,44,62,69,83,102,114,117,136,145	Ground	-

4.13 I2C , UART and SPI interface

4.13.1 UART

SDTM810 only contains one group UART_DM .The UART_DM is used to support high-speed UART operation up to 4 Mbps for debug and system log.

See Table4-12 and Figure4-7 for more details:

Table4-12 UART interface description

Signal	Pin#	Description	Direction
			I/O
GPIO_4	26	UART1 TX	O
GPIO_5	27	UART1 RX	I
GPIO_6	24	UART1 CTS_N	I
GPIO_7	25	UART1 RTS_N	O

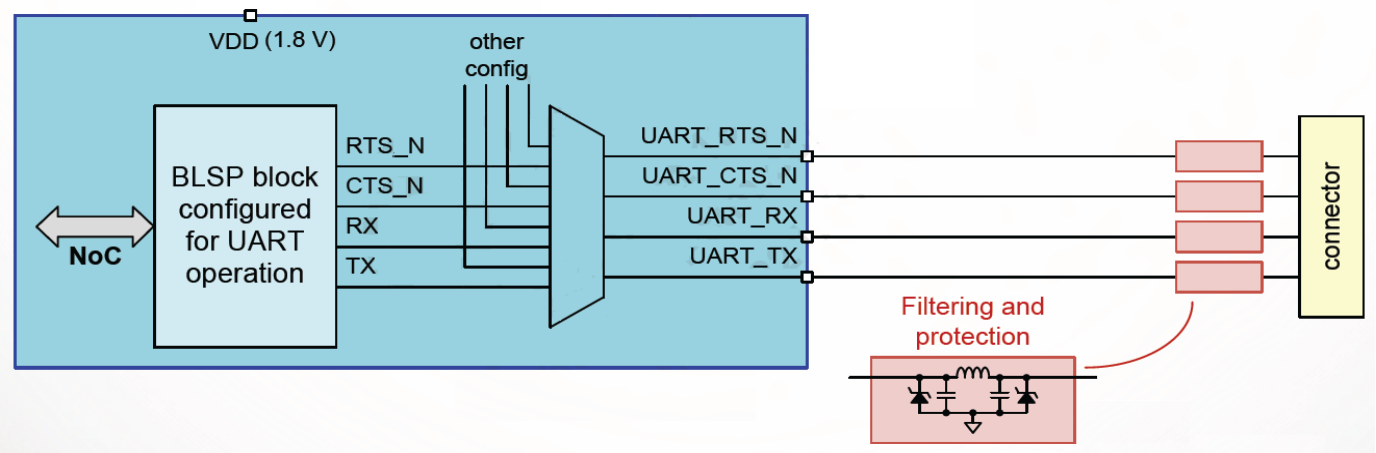


Figure4-7 UART application diagram

4.13.2 I2C

SDTM810 contains two groups special functional and four groups configurable I2C, which multiplexed with UART function. I2C pins use GPIOs configured as open-drain outputs; the pull-up resistor(2.2K) must be provided by external circuit(1.8V). High speed mode I2C running at 3.4 MHz.

See Table4-13:

Table4-13 I2C interface description

Signal	Pin#	Description	Direction
			AI/AO
TS_I2C_SDA	34	Touch Panel I2C,SDA	B
TS_I2C_SCL	35	Touch Panel I2C,SCL	B
CAM_I2C_SDA	132	Camera I2C,SDA	B
CAM_I2C_SCL	133	Camera I2C,SCL	B

The rest of I2C interface is multiplexed with UART function, See Table4-14 for more details.

Table4-14 I2C interface alternate function description

Signal	Pin#	Alternate function	
GPIO_6	24	UART2 CTS_N/GP	BLSP#1_I2C_SDA_B
GPIO_7	25	UART2 RTS_N/GP	BLSP#1_I2C_SCL_B
GPIO_111	28	UART2 CTS_N/GP	BLSP#2_I2C_SDA_B
GPIO_112	29	UART2 RTS_N/GP	BLSP#2_I2C_SCL_B
GPIO_14	22		BLSP4#_I2C_SDA_B
GPIO_15	23		BLSP4#_I2C_SCL_B
GPIO_29	52		BLSP3_I2C_SDA
GPIO_30	53		BLSP3_I2C_SCL

4.13.2 SPI

SDTM810 contains three groups configurable SPI, which multiplexed with UART/I2C function. But, SDTM810 only be used for master device.

Table4-15 SPI interface alternate function description

Signal	Pin#	Description	Direction
			I/O
GPIO_4	26	SPI1 MOSI	O
GPIO_5	27	SPI1 MISO	I
GPIO_6	24	SPI1 CS_N	O
GPIO_7	25	SPI1 CLK	O
GPIO_0	27(on J2601)	SPI2 MOSI	O
GPIO_1	26(on J2601)	SPI2 MISO	I
GPIO_2	25(on J2601)	SPI2 CS_N	O
GPIO_3	24(on J2601)	SPI2 CLK	O

4.14 Special interface

4.14.1 Camera flash Signal

In order to get good effect of camera flash, you can use external flash driver IC. It can be control by GPIO to get flash/torch mode.

4.14.2 PM_VIB_DRV_N Signal

The PM_VIB_DRV_N is used to control vibration intensity. The vibration driver is a programmable voltage output that is referenced to VDD; when off, its output voltage is VDD. The motor is connected between VDD and the PM_VIB_DRV_N pin.
See **Table4-16**

Table4-16 PM_VIB_DRV_N Signal

Signal	Pin#	Description	Direction
			I/O
PM_VIB_DRV_N	99	Vibration motor driver output control	AO

4.14.3 USB_HS_ID Signal

The USB_HS_ID pin is used for OTG. But if need support OTG, external circuit is needed.
See Table4-17.

Table4-17 USB_HS_ID Signal

Signal	Pin#	Description	Direction
			I/O
USB_HS_ID	64	Hardware identification	AI

4.14.4 VCOIN Signal

VCOIN requires either a lithium manganese dioxide rechargeable coin cell or a keep-alive capacitor, so that the appropriate oscillator and real-time clock circuits continue to run when the phone is off.
See Table4-18.

Table4-18 VCOIN Signal

Signal	Pin#	Description	Direction
			I/O
VCOIN	111	Sense input or charge output	AI,AO

4.14.5 RF Signal input port

SDTM810 contains four RF signal input port: BT/WIFI, GPS, main antenna and diversity antenna.

Table4-19 RF Signal input port

Signal	Pin#	Description	Direction
			I/O
MAIN_INT_OUT	1	MAIN_IN	AI
WIFI_BT_RF	31	BT/WIFI	AI
DIV_ANT_IN	115	DIV_IN	AI
GPS_IN	116	GPS_IN	AI

4.15 Secure payment interfaces

SDTM810 supports secure payment, includes all the essential functions of mobile POS terminal including a cryptographic engine, a true random number generator, environmental and tamper detection circuitry, a magnetic stripe reader, a smart card controller with embedded transceiver to directly support 1.8V, 3.3V, and 5V cards, an integrated secure keypad controller, and NFC Initiator/HF Reader.

4.15.1 External Tamper Sensors

SDTM810 there are four external tamper sensor with independent random dynamic patterns. Every group in/out can not close to each.

See Table4-20.

Table4-20 RF Signal input port

Signal	Pin#	Description	Direction
			I/O
EXTS1_OUT	75	External Sensor1 Output	AO
EXTS0_IN	76	External Sensor0 Input	AI
EXTS2_OUT	77	External Sensor2 Output	AO
EXTS3_IN	78	External Sensor3 Input	AI
EXTS0_OUT	79	External Sensor0 Output	AO
EXTS2_IN	80	External Sensor2 Input	AI
EXTS1_IN	81	External Sensor1 Input	AI
EXTS3_OUT	82	External Sensor3 Output	AO

4.15.2 Magnetic Stripe Reader

SDTM810 includes Triple-Track Magnetic Stripe Head Interface. See Table 4-21 for details.

Table 4-21

Signal	Pin#	Description	Direction
			I/O
MCR_2P	84	Magnetic Stripe Reader Track2 Positive Input	AI
MCR_2N	85	Magnetic Stripe Reader Track2 Negative Input	AI
MCR_3P	86	Magnetic Stripe Reader Track3 Positive Input	AI
MCR_3N	87	Magnetic Stripe Reader Track3 Negative Input	AI
MCR_1P	88	Magnetic Stripe Reader Track1 Positive Input	AI
MCR_1N	89	Magnetic Stripe Reader Track1 Negative Input	AI

4.15.3 Smart card

SDTM810 supports a smart card controller with embedded transceiver to directly support 1.8V, 3.3V, and 5V cards. See Table 4-22 in details.

Table 4-22

Signal	Pin#	Description	Direction
			I/O
SC_IO	90	Smart Cart I/O	DI,DO
SC_VCC	91	Power for smart card	PO
SC_CLK	92	Smart Cart CLK	DO
SC_RST	93	Smart Cart Reset	DO
SC_C8	94	Smart Cart C8	DI
SC_C4	95	Smart Cart C4	DI
SC_DETECT	96	Smart Cart Detect	DI
SC_RST_BYP	23(on J2701)	Reserve	DO
SC_IO_BYP	22(on J2701)	Reserve	DI,DO
SC_DETECT_BYP	21(on J2701)	Reserve	DI
SC_CLK_BYP	20(on J2701)	Reserve	DO

4.15.4 NFC Initiator/HF Reader

SDTM810 includes the analog front end (AFE) and a highly integrated data framing system for ISO 18092 (NFCIP-1) initiator, ISO 18092 (NFCIP-1) active target, ISO 14443 A and B reader (including high bit rates) and FeliCa™ reader. Compared with concurrent NFC devices designed with the mobile phone in mind, the module is positioned perfectly for the infrastructure side of the NFC system, where users need optimal RF performance and flexibility combined with low power.SDTM810 is alone in the domain of HF Reader ICs in that it contains two differential low impedance (1Ω) antenna drivers. The power and antenna interface in Table 4-23.

Table 4-23

Signal	Pin#	Description	Direction
			I/O
VCC_5V	65	Power	PI
RFO1	70	RF Antenna Output 1	AO
RFO2	71	RF Antenna Output 2	AO
RFI1	72	RF Antenna Input 1	AI
RFI2	73	RF Antenna Input 2	AI

4.15.5 Secure Keypad

SDTM810 includes 8-Line Secure Keypad Controller, these interface on J2701 (BTB connector).See Table 4-24 in details.

Table 4-24

Signal	Pin#	Description	Direction
			I/O
KBD0	1(on J2701)	Keyboard I/O 0	AI
KBD1	2(on J2701)	Keyboard I/O 1	AI
KBD2	3(on J2701)	Keyboard I/O 2	AI
KBD3	4(on J2701)	Keyboard I/O 3	AI
KBD4	5(on J2701)	Keyboard I/O 4	AI
KBD5	6(on J2701)	Keyboard I/O 5	AI
KBD6	7(on J2701)	Keyboard I/O 6	AI
KBD7	8(on J2701)	Keyboard I/O 7	AI

4.15.5 Backup battery

SDTM810's secure payment need independent backup battery. Once power off, useful data can be reserve .

See Table 4-25 in details.

Table 4-25

Signal	Pin#	Description	Direction
			I/O
MAX_VBAT	66	Back battery for secure circuit	PI
ADC0	67	Detect back battery voltage	AI

4.15.6 TCLK

SDTM810 there are two tclk interface, as 3.3V GPIO, they are reserved.

See Table 4-26.

Table 4-26

Signal	Pin#	Description	Direction
			I/O
TCLK6	68	GPIO(3.3V), reserve	BI,BO
TCLK7	100	GPIO(3.3V), reserve	BI,BO

5 Mechanical Specification

5.1 Overview

This specification defines a small form factor module for systems in which a Stamp hole package add-in module can not be used due to mechanical system design constraints. The specification defines a smaller module based on a single 146-pin Leadless Chip Carriers encapsulation for system interfaces by card edge type. The specification also defines the Stamp hole package system.

5.2 SDTM810 specifications

There is Stamp hole package add-in SDTM810 size.
For purposes of the drawings in this specification, the following notes apply:
- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ±0.15 mm, unless otherwise specified.
- Dimensions marked with an asterisk (*) are overall envelope dimensions and include space allowances for insulation to comply with regulatory and safety requirements.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.

5.2.1 SDTM810 from factor

The SDTM810 form factor is specified by **Figure5-1**.
The figure illustrates a module example application. The hatched area shown in this figure represents the available component volume for the SDTM810's circuitry.

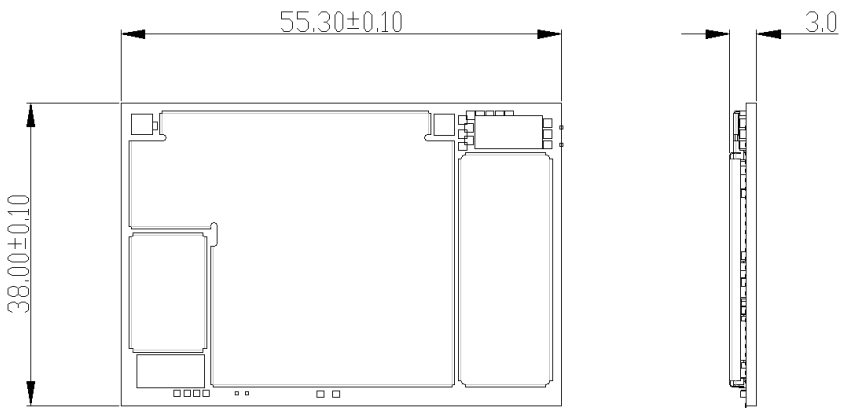


Figure5-1 SDTM810 form factor

5.2.2 SDTM810 PCB details

The following figures (**Figure5-2**) provide the printed circuit board (PCB) details required to

fabricate the PCB. The PCB for this application is expected to be 1.2 mm thick. The steel net thickness is 0.12mm (**Figure5-3**).

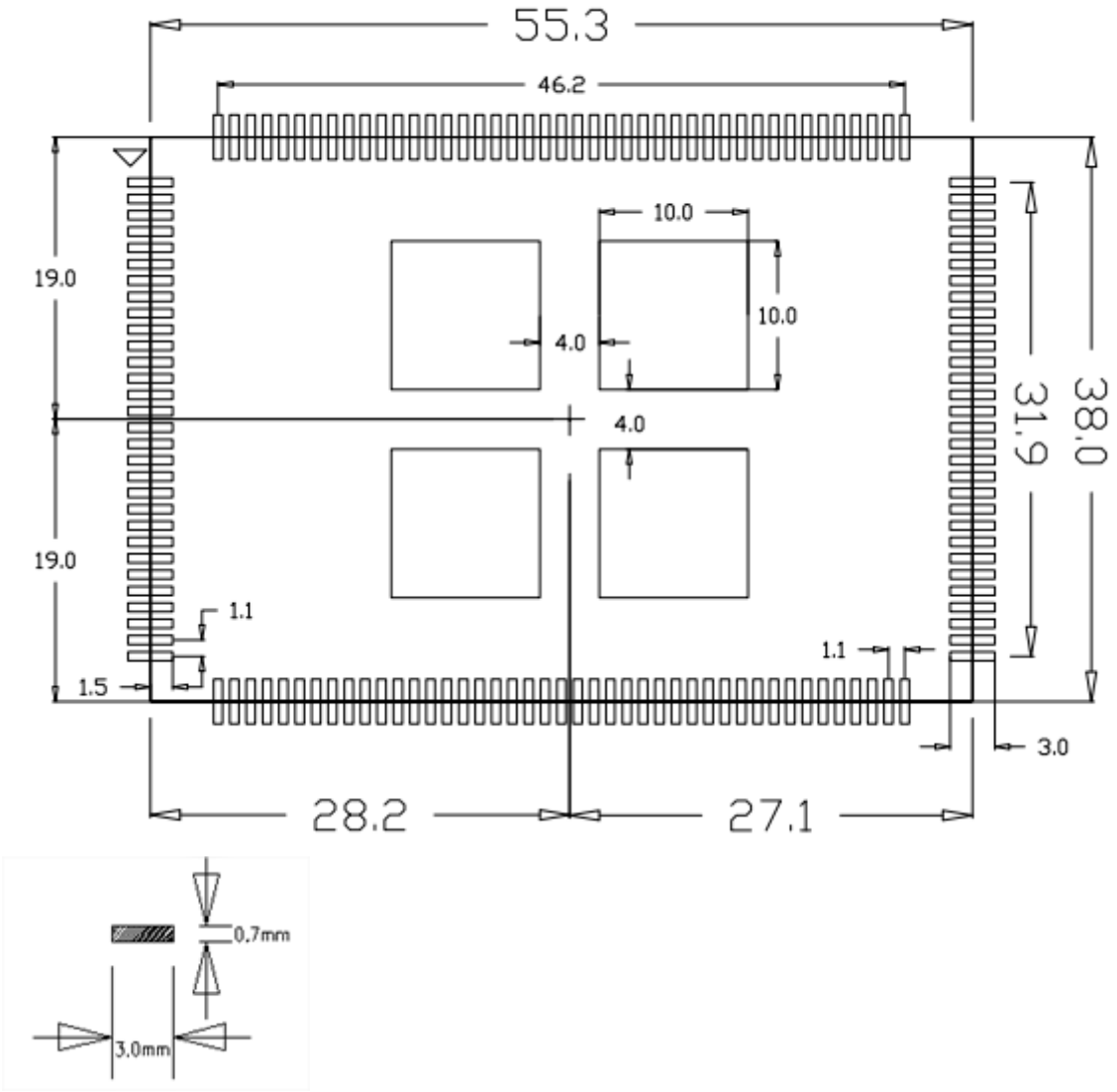


Figure5-2 SDTM810 Pads

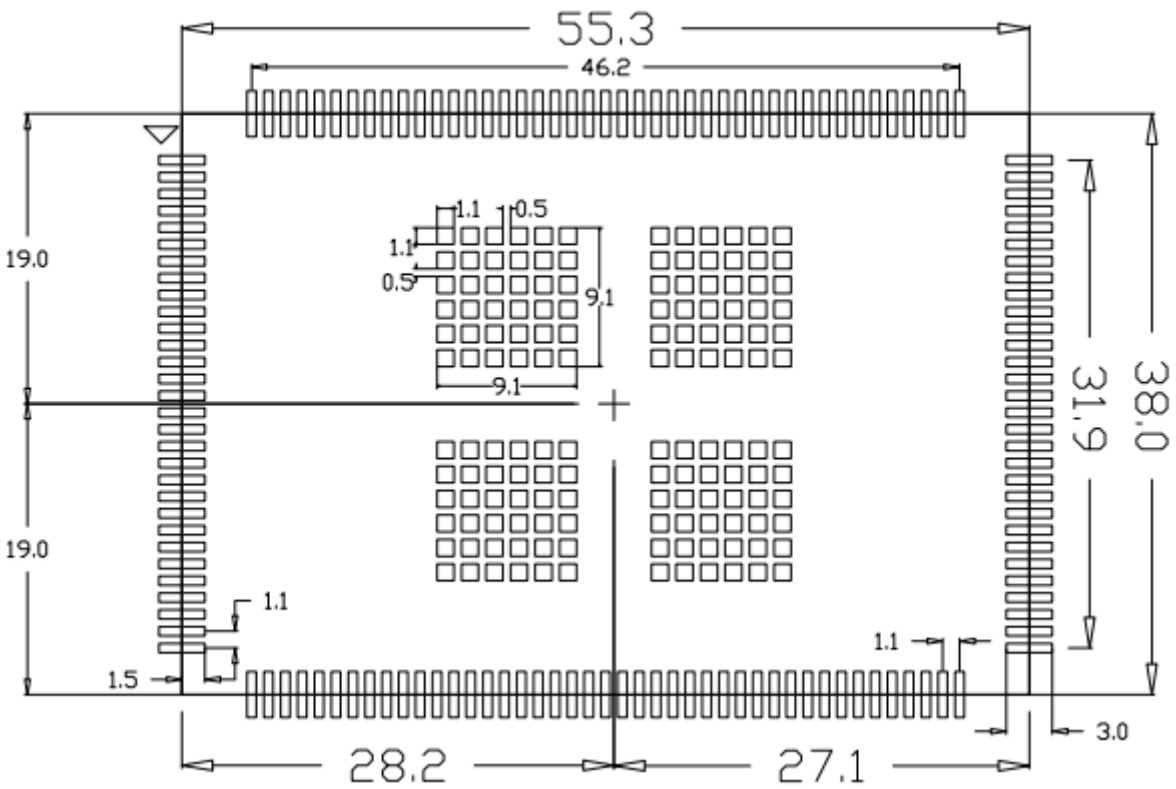


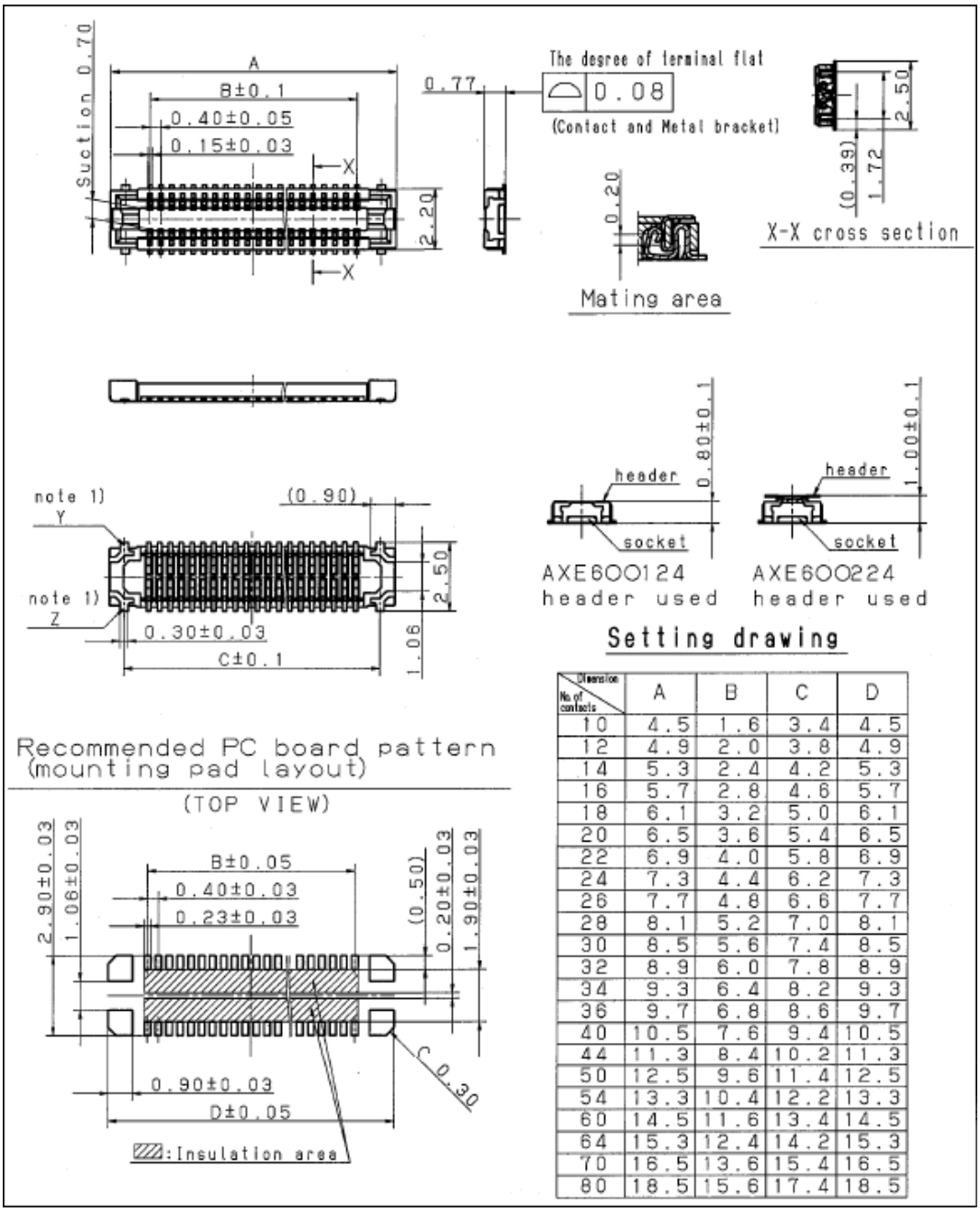
Figure5-3 SDTM810 Steel net

5.3 System BTB connector specifications

The SDTM810 includes two BTB connector where connect more GPIO interface or debug.

5.3.1 BTB connector

The BTB connector is 30-pin card edge type connector. Detailed dimensions should be obtained from the connector manufacturer. **Figure5-4** shows the BTB connector. We use AXE630124 (header). In order to match AXE630124,you can use AXE530127 as socket .



Dimension / No. of contacts	A	B	C	D
10	4.5	1.6	3.4	4.5
12	4.9	2.0	3.8	4.9
14	5.3	2.4	4.2	5.3
16	5.7	2.8	4.6	5.7
18	6.1	3.2	5.0	6.1
20	6.5	3.6	5.4	6.5
22	6.9	4.0	5.8	6.9
24	7.3	4.4	6.2	7.3
26	7.7	4.8	6.6	7.7
28	8.1	5.2	7.0	8.1
30	8.5	5.6	7.4	8.5
32	8.9	6.0	7.8	8.9
34	9.3	6.4	8.2	9.3
36	9.7	6.8	8.6	9.7
40	10.5	7.6	9.4	10.5
44	11.3	8.4	10.2	11.3
50	12.5	9.6	11.4	12.5
54	13.3	10.4	12.2	13.3
60	14.5	11.6	13.4	14.5
64	15.3	12.4	14.2	15.3
70	16.5	13.6	15.4	16.5
80	18.5	15.6	17.4	18.5

Figure5-4 BTB connector

6 RF Specification

TBD

7 Model catalog

TBD