SanDisk®

43nm
8GB (32Gb x 2-die)
16GB (32Gb x 4-die)
32GB (32Gb x 8-die)
4LC 3V NAND Flash Memory Data Sheet

Preliminary Version
Rev 1.3

March 11, 2009

Part Numbers: SDZNMMBHER-008G
SDZNMMCHER-016G
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Proprietary and Confidential

Revision History

Version	Revision	Date	Changes
Preliminary	0.3	01/09/09	Initial release.
Preliminary	1.0	01/14/09	Added Package Marking Spec; minor changes.
Preliminary	1.1	02/10/09	Updated timing diagrams.
Preliminary	1.2	03/09/09	Updated the following sections to clarify the Power On Reset current consumption: • 1.7 Power-On/Off Sequence • 1.8 Power On Reset • 1.14 DC Characteristics Updated the following sections to clarify the parameter value in multi-die package: • 1.2 Features • 1.11 Capacitance • 1.12 Valid Blocks • 1.14 DC Characteristics
Preliminary	1.3	03/11/09	Updated Package Marking Specification.

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1. Device Overview

1.1 Description

The 43nm 8GB / 16GB / 32GB 4LC 3V NAND Flash Memory contains 2, 4, or 8 32Gb NAND Flash Memory dies in a 52-lead 14 x 18 LGA package.

Each 32Gb NAND Flash Memory has two 8568-byte static registers, which allow program and read data to be transferred between the register and the memory cell array in 8568-byte increments. The device is organized as (8192 + 376) bytes × 128 pages × 4096 blocks. A single block unit consists of 1 Mbyte + 47 Kbytes = 8568 bytes x 128 pages.

This serial-type memory device makes use of I/O pins for command inputs, as well as for both address and data input/output. Erase and Program operations are executed automatically, making the device highly suited for applications such as solid-state file storage, image file memory for still cameras, voice recording, and other systems that require high-density non-volatile memory data storage.

1.2 Features

Feature	32Gb (4LC)
Organization:	
Memory Cell Array	8568 x 512K x 8 per die
Number of Registers	8568 x 8 per die
Number of Planes	2 per die
Block Size	(1M + 47K) bytes
Page Size	(8192 + 376) bytes = 8568 bytes
Number of Pages per Block	128
Modes	Read, Multi Page Read, Single Page Program, Auto Page Program, Multi Page Program, Page Copy, Multi Page Copy, Single Block Erase, Multi Block Erase, ID Read, Status Read, Reset
Mode Control	Serial input/output Command control
Number of Valid Blocks	Max 4096 blocks per die; Min 3933 blocks per die
Power Supply	VCC = 2.7V to 3.6V
Access Time	Cell Array to Register: 200 µs max Serial Read Cycle: 25 ns min
Program/Erase Time	Auto Page Program: 1600 µs/page typ. Single Block Erase: 3 ms/block typ.
Operating Current *	Read (30 ns cycle): 50 mA max Program (avg.): 50 mA max Erase (avg.): 50 mA max Standby: 50 µA max
Package	14mm x 18mm x 1.0mm LGA 52-Pin

* Measured per selected active die at VCC = 3.6V, 30 ns Read/Write cycle time.

1.3 Pin Assignment

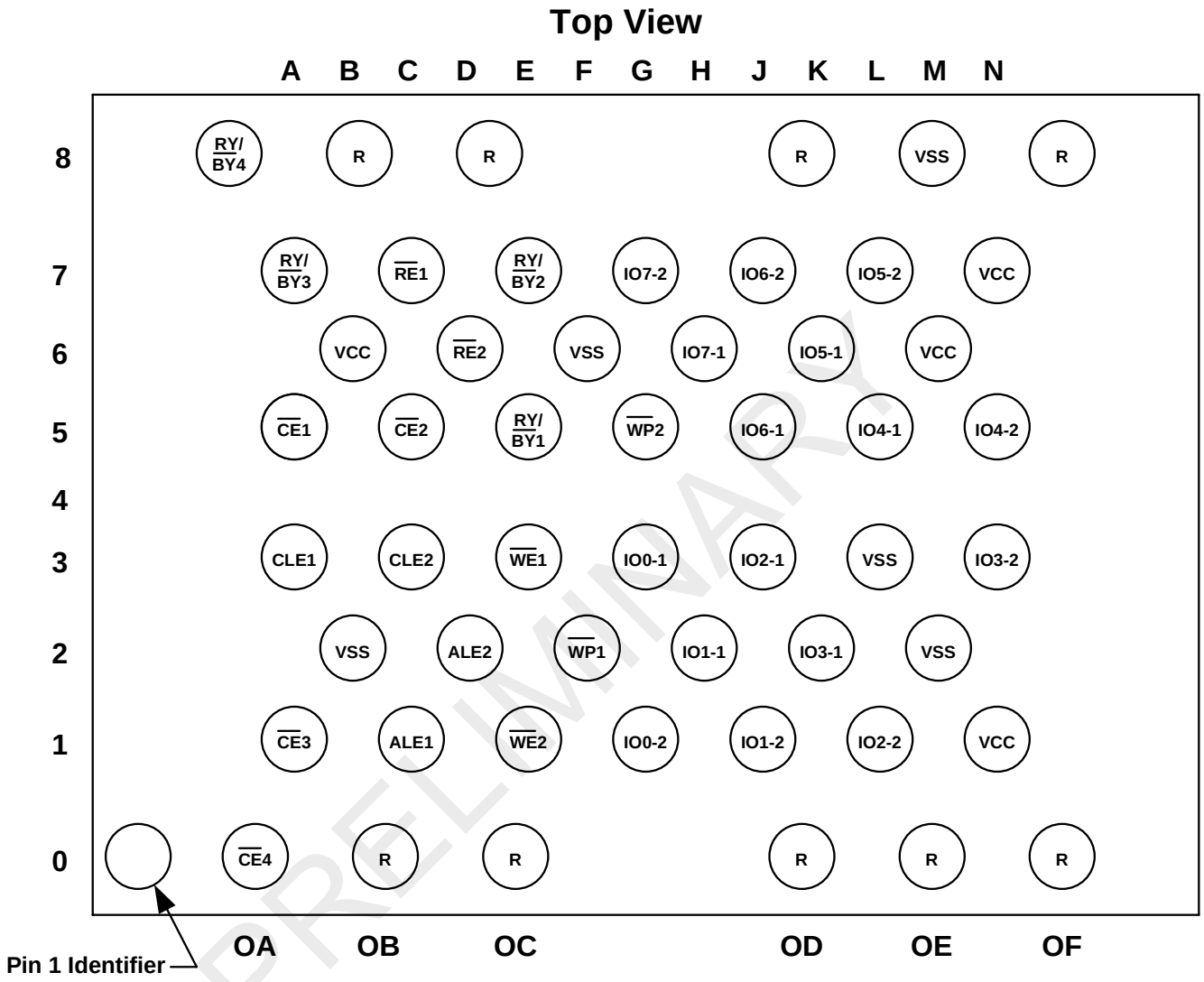
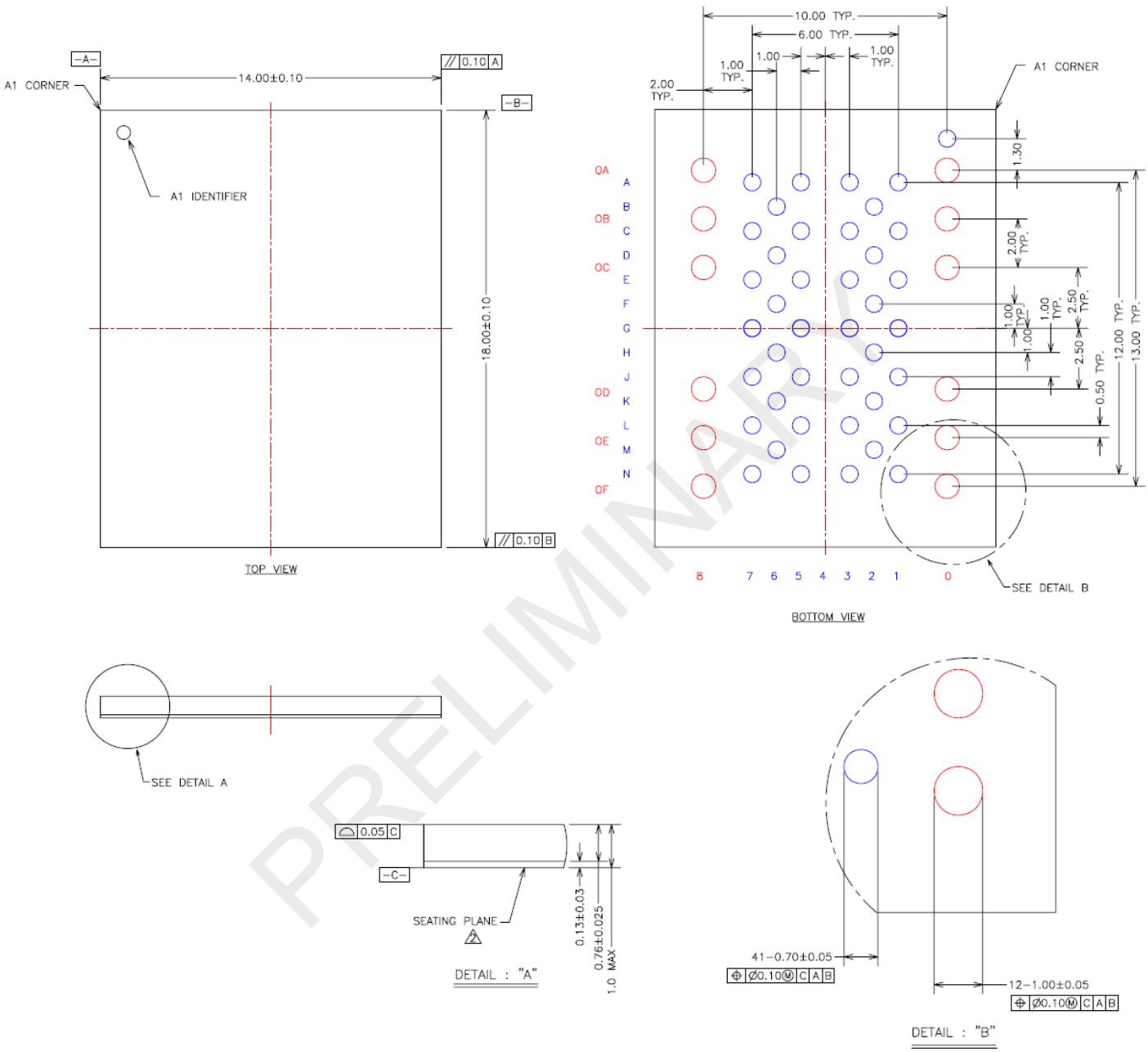


Figure 1: 14 x 18 52-Pin LGA Pinout

1.4 52-Pin LGA Package Outline Drawing



All Dimensions in Millimeters

Figure 2: 52-Pin Package Outline Drawing

1.5 Pin Functions

This serial access memory device makes use of timesharing for input of address information.

Pin Name	Type	Description
$\overline{CE}$	Input	Chip Enable: The device goes into a low-power Standby mode when $\overline{CE}$ goes High while the device is in Ready state. The $\overline{CE}$ signal is ignored when the device is in Busy state (RY/$\overline{BY}$ = L), such as during a Program, Erase, or Read operation, and does not enter Standby mode even if the $\overline{CE}$ input goes High.
$\overline{WE}$	Input	Write Enable: The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.
$\overline{RE}$	Input	Read Enable: The $\overline{RE}$ signal controls serial data output. Data is available tREA after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address = Address + I) on this falling edge.
CLE	Input	Command Latch Enable: The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.
ALE	Input	Address Latch Enable: The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge the $\overline{WE}$ signal while ALE is High.
$\overline{WP}$	Input	Write Protect: The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence, when input signals are invalid.
RY/$\overline{BY}$	Output	Ready/Busy: The RY/$\overline{BY}$ output signal is used to indicate the operating condition of the device. The RY/$\overline{BY}$ signal is in Busy state (RY/$\overline{BY}$ = L) during Program, Erase, and Read operations, and it returns to Ready state (RY/$\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and must be pulled up to Vcc with an appropriate resistor.
VCC	Supply	Power Supply, 2.7 to 3.6V
VSS	Supply	Ground
I/O0 to I/O7	I/O	I/O Ports: The I/O0 to 7 pins are used as a port for transferring address, command, and input/output data to and from the device.
NC		Do Not Connect

There are 4 $\overline{CE}$, 4 RY/$\overline{BY}$, 2 $\overline{RE}$, 2 CLE, 2 ALE, 2 $\overline{WE}$, and 2 $\overline{WP}$ pins. There are two 8-bit-wide data I/O buses, with $\overline{CE}$1 and $\overline{CE}$3 mapped to the I/O-1 bus, and $\overline{CE}$2 and $\overline{CE}$4 mapped to the I/O-2 bus, per the ONFI 2.0 specification. See the "Pin Decoding Tables" section for pin decoding information for 2, 4, and 8-die packages.

1.6 Pin Decoding Tables

Pin Decoding for 8-Die Package with 4 $\overline{CE}$ Pins

Pad Name	NAND Flash Memory Device							
	#1	#2	#3	#4	#5	#6	#7	#8
$\overline{CE}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	$\overline{CE4}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	$\overline{CE4}$
RY/$\overline{BY}$	RY/$\overline{BY1}$	RY/$\overline{BY2}$	RY/$\overline{BY3}$	RY/$\overline{BY4}$	RY/$\overline{BY1}$	RY/$\overline{BY2}$	RY/$\overline{BY3}$	RY/$\overline{BY4}$
$\overline{RE}$	$\overline{RE1}$	$\overline{RE2}$	$\overline{RE1}$	$\overline{RE2}$	$\overline{RE1}$	$\overline{RE2}$	$\overline{RE1}$	$\overline{RE2}$
CLE	CLE1	CLE2	CLE1	CLE2	CLE1	CLE2	CLE1	CLE2
ALE	ALE1	ALE2	ALE1	ALE2	ALE1	ALE2	ALE1	ALE2
$\overline{WE}$	$\overline{WE1}$	$\overline{WE2}$	$\overline{WE1}$	$\overline{WE2}$	$\overline{WE1}$	$\overline{WE2}$	$\overline{WE1}$	$\overline{WE2}$
$\overline{WP}$	$\overline{WP1}$	$\overline{WP2}$	$\overline{WP1}$	$\overline{WP2}$	$\overline{WP1}$	$\overline{WP2}$	$\overline{WP1}$	$\overline{WP2}$
IO0	IO0-1	IO0-2	IO0-1	IO0-2	IO0-1	IO0-2	IO0-1	IO0-2
IO1	IO1-1	IO1-2	IO1-1	IO1-2	IO1-1	IO1-2	IO1-1	IO1-2
IO2	IO2-1	IO2-2	IO2-1	IO2-2	IO2-1	IO2-2	IO2-1	IO2-2
IO3	IO3-1	IO3-2	IO3-1	IO3-2	IO3-1	IO3-2	IO3-1	IO3-2
IO4	IO4-1	IO4-2	IO4-1	IO4-2	IO4-1	IO4-2	IO4-1	IO4-2
IO5	IO5-1	IO5-2	IO5-1	IO5-2	IO5-1	IO5-2	IO5-1	IO5-2
IO6	IO6-1	IO6-2	IO6-1	IO6-2	IO6-1	IO6-2	IO6-1	IO6-2
IO7	IO7-1	IO7-2	IO7-1	IO7-2	IO7-1	IO7-2	IO7-1	IO7-2

Pin Decoding for 4-Die Package with 4 $\overline{CE}$ Pins

Pad Name	NAND Flash Memory Device			
	#1	#2	#3	#4
$\overline{CE}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	$\overline{CE4}$
RY/$\overline{BY}$	RY/$\overline{BY1}$	RY/$\overline{BY2}$	RY/$\overline{BY3}$	RY/$\overline{BY4}$
$\overline{RE}$	$\overline{RE1}$	$\overline{RE2}$	$\overline{RE1}$	$\overline{RE2}$
CLE	CLE1	CLE2	CLE1	CLE2
ALE	ALE1	ALE2	ALE1	ALE2
$\overline{WE}$	$\overline{WE1}$	$\overline{WE2}$	$\overline{WE1}$	$\overline{WE2}$
$\overline{WP}$	$\overline{WP1}$	$\overline{WP2}$	$\overline{WP1}$	$\overline{WP2}$
IO0	IO0-1	IO0-2	IO0-1	IO0-2
IO1	IO1-1	IO1-2	IO1-1	IO1-2
IO2	IO2-1	IO2-2	IO2-1	IO2-2
IO3	IO3-1	IO3-2	IO3-1	IO3-2
IO4	IO4-1	IO4-2	IO4-1	IO4-2
IO5	IO5-1	IO5-2	IO5-1	IO5-2
IO6	IO6-1	IO6-2	IO6-1	IO6-2
IO7	IO7-1	IO7-2	IO7-1	IO7-2

Pin Decoding for 2-Die Package with 2 $\overline{CE}$ Pins

Pad Name	NAND Flash Memory Device	
	#1	#2
$\overline{CE}$	$\overline{CE1}$	$\overline{CE2}$
RY/$\overline{BY}$	RY/$\overline{BY1}$	RY/$\overline{BY2}$
$\overline{RE}$	$\overline{RE1}$	$\overline{RE2}$
CLE	CLE1	CLE2
ALE	ALE1	ALE2
$\overline{WE}$	$\overline{WE1}$	$\overline{WE2}$
$\overline{WP}$	$\overline{WP1}$	$\overline{WP2}$
IO0	IO0-1	IO0-2
IO1	IO1-1	IO1-2
IO2	IO2-1	IO2-2
IO3	IO3-1	IO3-2
IO4	IO4-1	IO4-2
IO5	IO5-1	IO5-2
IO6	IO6-1	IO6-2
IO7	IO7-1	IO7-2

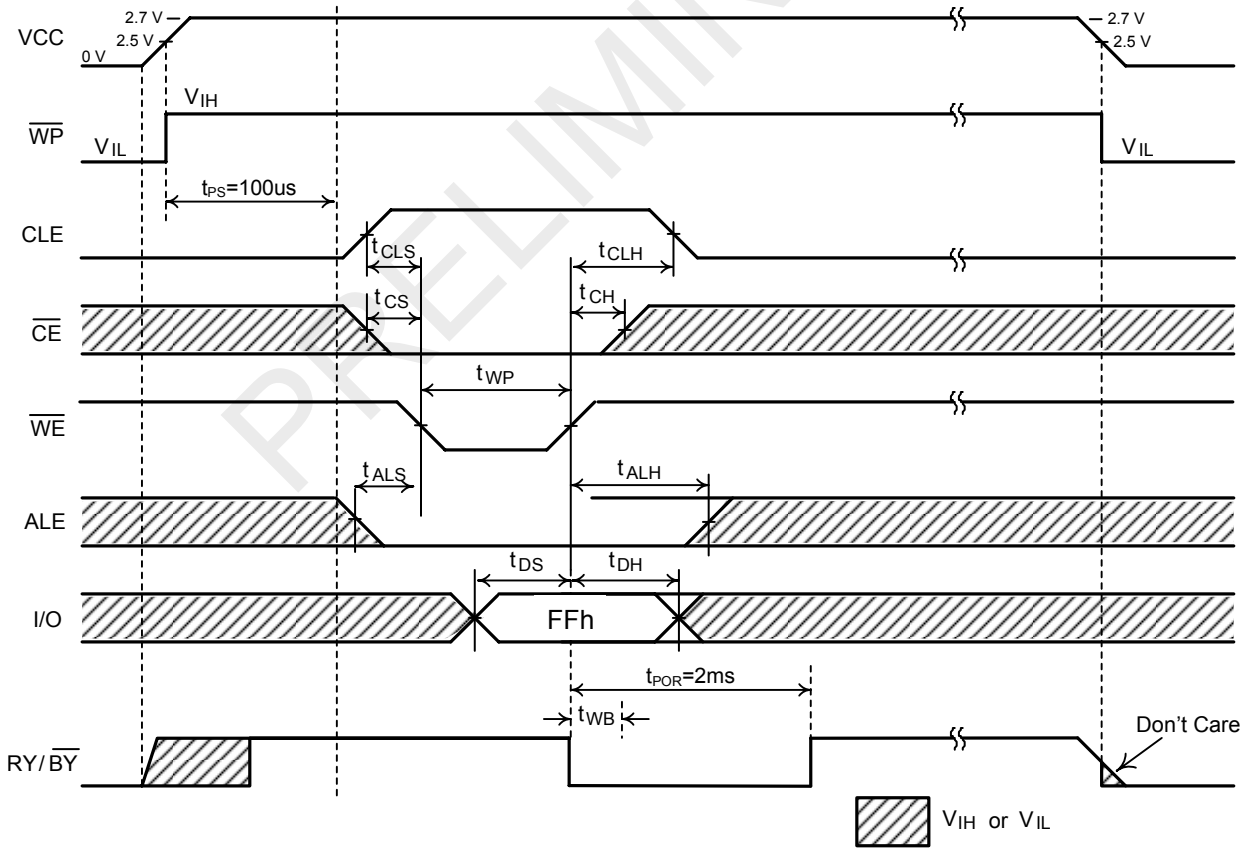
1.7 Power-On/Off Sequence

The device is configured such that it does NOT go into automatic self initialization during power on. It is highly recommended that the Write Protect signal should go high during the initial power-on and power-off sequence (as shown in the diagram below) for protecting against data corruption.

1.8 Power On Reset

Since some input signals might not be stable at power on, performing an FFh Reset after power up is necessary. During the FFh Reset Busy period, each selected die in the device consumes a maximum current of 50mA (I_{CCO0}). Only the selected die is reset by the FFh command.

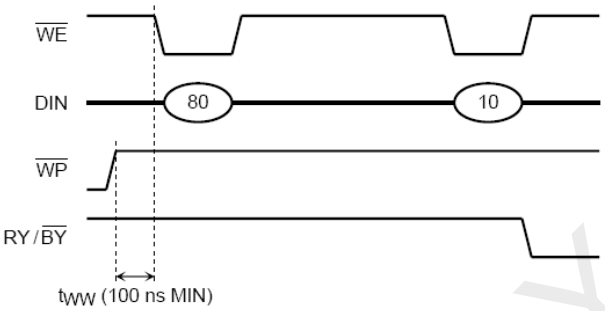
For the 2-die device with 2 Chip Enable control pins and the 4-die device with 4 Chip Enable control pins, one die is selected by each Chip Enable control pin. For the 8-die device with 4 Chip Enable control pins, two die are selected by each Chip Enable control pin. The maximum current consumed during the Reset Busy period is 50mA per die selected by the Chip Enable control pin(s). Therefore, for 2-die and 4-die devices, the maximum current consumed during the Reset Busy period is 50mA when one Chip Enable control pin is asserted; and for 8-die devices, the maximum current consumed during the Reset Busy period is 100mA when one Chip Enable control pin is asserted.



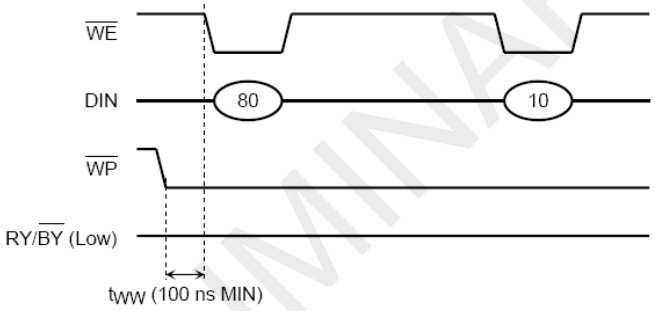
1.9 Write Protect Signal

Erase and Program operations are automatically reset when the Write Protect signal goes Low. The operations are enabled and disabled, as follows:

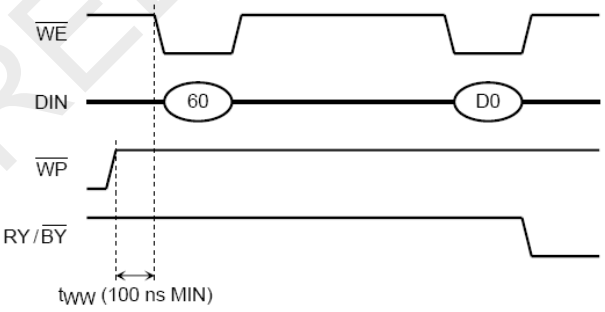
Enable Programming



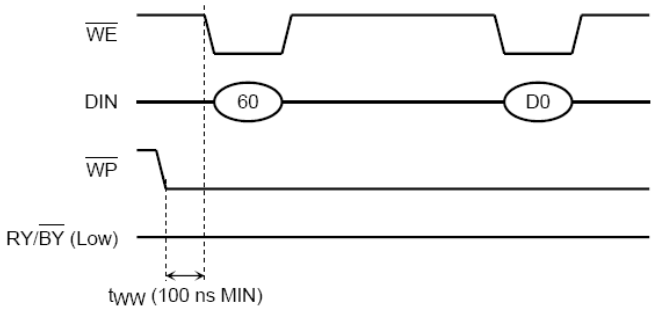
Disable Programming



Enable Erasing



Disable Erasing



1.10 Absolute Maximum Ratings

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	–0.6 to 4.6	V
V_{IN}	Input Voltage	–0.6 to 4.6	V
$V_{I/O}$	Input/Output Voltage	–0.6 to V_{CC} + 0.3 (≤ 4.6)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	–55 to 150	°C
T_{OPR}	Operating Temperature	0 to 70	°C

1.11 Capacitance

(Ta = 25° C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
C_{IN} *	Input	V_{IN} = 0 V	---	5	10	pF
C_{OUT} *	Output	V_{OUT} = 0 V	---	5	10	pF

* This parameter is per die, is periodically sampled, and is not tested for every device.

1.12 Valid Blocks

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks per Die	3933	---	4096	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (6) toward the end of this document.

The first block (Block 0) is guaranteed to be a valid block at the time of shipment.

The specification for the minimum number of valid blocks is applicable over the device lifetime.

1.13 Recommended DC Operating Conditions

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	---	3.6	V
V_{iH}	High-Level Input Voltage 2.7 V ≤ V_{CC} ≤ 3.6 V	0.8 x VCC	---	VCC + 0.3	V
V_{iL}	Low-Level Input Voltage 2.7 V ≤ V_{CC} ≤ 3.6 V	–0.3 *	---	0.2 x VCC	V

* –2 V (pulse width less than 20 ns)

1.14 DC Characteristics

(Ta = 0 to 70°C, VCC = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}			±10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}			±10	µA
I_{CCO0} *	Power On Reset Current	During FFh command input after Power On			50	mA
I_{CCO1} *	Serial Read Current	$\overline{CE}$ = V_{IL} , I_{OUT} = 0 mA, tcycle = 30 ns			50	mA
I_{CCO2} *	Programming Current	---			50	mA
I_{CCO3} *	Erasing Current	---			50	mA
I_{CCS} **	Standby Current	$\overline{CE}$ = V_{CC} – 0.2 V, $\overline{WP}$ = 0 V/V_{CC}			50	µA
V_{OH}	High-Level Output Voltage	I_{OH} = – 0.4 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	2.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 2.1 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)			0.4	V
I_{OL} ($RY/\overline{BY}$)	Output Current of $RY/\overline{BY}$ Pin	V_{OL} = 0.4 V (2.7 V ≤ V_{CC} ≤ 3.6 V)		8		mA

* per selected active die in the package

** per die in the package

1.15 AC Characteristics and Recommended Operating Conditions

(Ta = 0 to 70°C, VCC = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CLS}	CLE Setup Time	0	—	ns
t_{CLS2}	CLE Setup Time	30	—	ns
t_{CLH}	CLE Hold Time	5	—	ns
t_{CS}	$\overline{CE}$ Setup Time	8	—	ns
t_{CS2}	$\overline{CE}$ Setup Time	20	—	ns
t_{CH}	$\overline{CE}$ Hold Time	5	—	ns
t_{WP}	Write Pulse Width	12	—	ns
t_{ALS}	ALE Setup Time	0	—	ns
t_{ALH}	ALE Hold Time	5	—	ns
t_{DS}	Data Setup Time	10	—	ns
t_{DH}	Data Hold Time	5	—	ns
t_{WC}	Write Cycle Time	25	—	ns
t_{WH}	$\overline{WE}$ High Hold Time	10	—	ns
t_{WHW} *	$\overline{WE}$ High Hold Time from final address to first data	80	—	ns
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns
t_{RW}	Ready to $\overline{WE}$ Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	12	—	ns
t_{RC}	Read Cycle Time	25	—	ns
t_{REA}	$\overline{RE}$ Access Time	—	20	ns
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low	10	—	ns
t_{CLR}	CLE Low to $\overline{RE}$ Low	10	—	ns
t_{AR}	ALE Low to $\overline{RE}$ Low	10	—	ns
t_{RHOH}	Data Output Hold Time from $\overline{RE}$ High	30	—	ns
t_{RLOH}	Data Output Hold Time from $\overline{RE}$ Low	5	—	ns
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	60	ns
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	30	ns
t_{CLHZ}	CLE High to Output High Impedance	—	30	ns
t_{REH}	$\overline{RE}$ High Hold Time	10	—	ns
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	120	—	ns
t_{R}	Memory Cell Array to Starting Address	—	200	µs
$t_{DCBSYR1}$	Data Cache Busy in Read Cache (following 31h and 3Fh)	—	200	µs
$t_{DCBSYR2}$	Data Cache Busy in Page Copy (following 3Ah)	—	205	µs
t_{WB}	$\overline{WE}$ High to Busy	—	100	ns
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	10/10/30/500	µs

* t_{WHW} is the time from the $\overline{WE}$ rising edge of the final address cycle to the $\overline{WE}$ falling edge of the first data cycle.

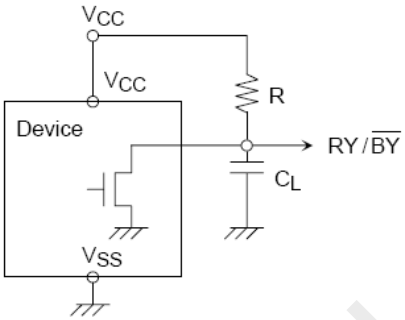
1.16 AC Test Conditions

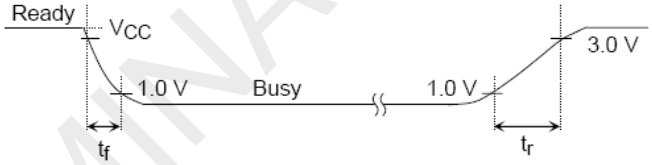
PARAMETER	CONDITION
	2.7 V ≤ V_{CC} ≤ 3.6 V
Input level	0 V to V_{CC}
Input pulse rise and fall time	3ns
Input comparison level	1/2 V_{CC}
Output data comparison level	1/2 V_{CC}
Output load	C_L (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.

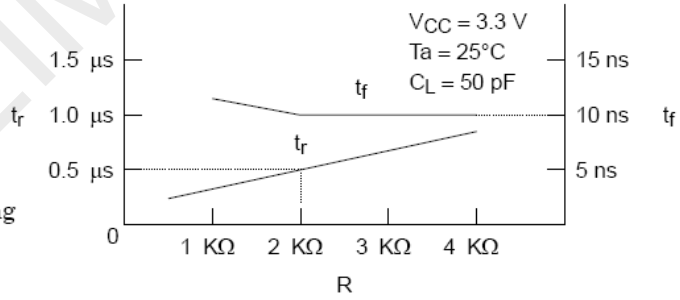
RY / $\overline{BY}$: Termination for the Ready/Busy Pin (RY/$\overline{BY}$)

A pull-up resistor must be used for termination, because the RY/$\overline{BY}$ buffer consists of an open drain circuit.





This data might vary from device to device. Using this data as a reference when selecting a resistor value is recommended.



1.17 Programming and Erasing Characteristics

(Ta = 0 to 70°C, VCC = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	1600	3000	µs	
$t_{DCBSYW1}$	Data Cache Busy Time in Write Cache (following 11h)	—	—	5	µs	
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)	—	—	3000	µs	(2)
N	Number of Partial Program Cycles in the Same Page	—	—	0		(1)
t_{BERASE}	Block Erasing Time	—	3	10	ms	

(1) Partial page programming is not supported.

(2) $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

2. Address Assignment

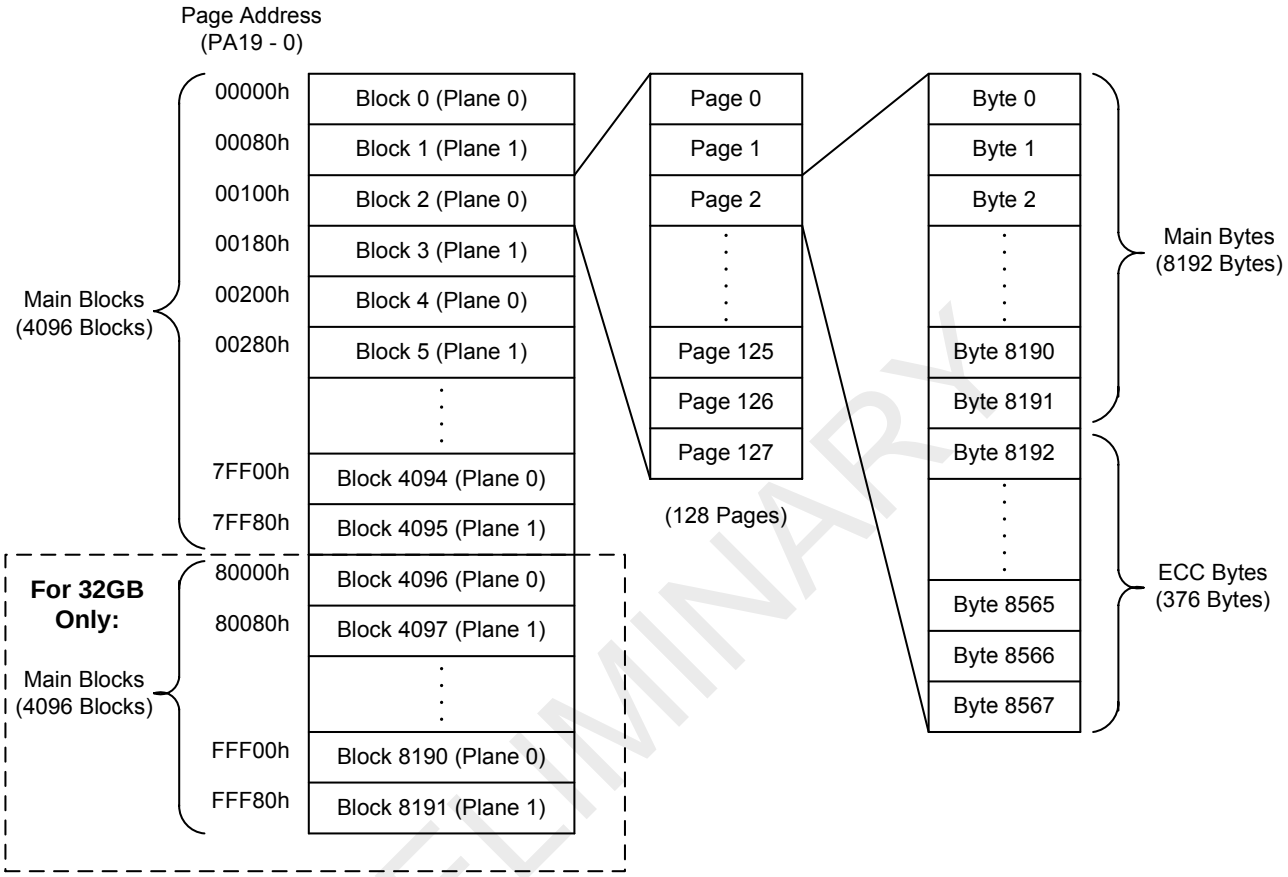


Table 1: Addressing

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First Cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second Cycle	L	L	CA13	CA12	CA11	CA10	CA9	CA8
Third Cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth Cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
Fifth Cycle	L	L	L	L	PA19	PA18	PA17	PA16

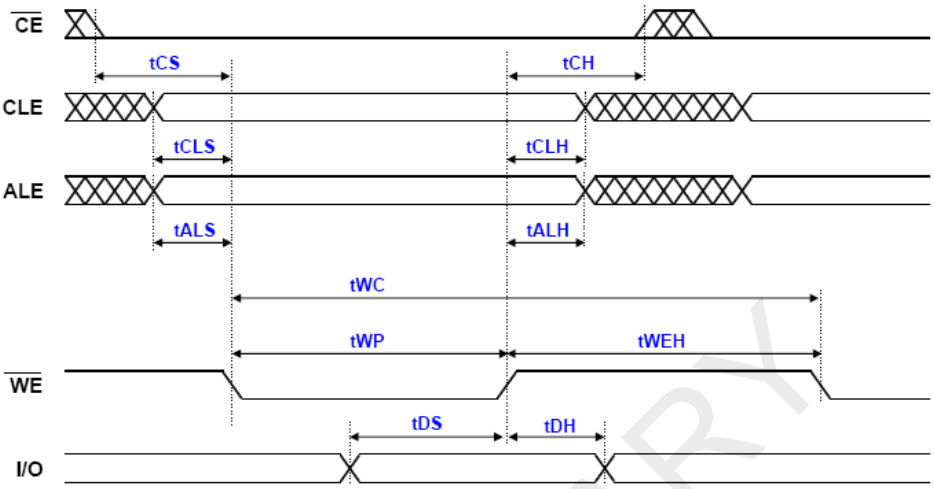
CA0 to CA13: Column Address

PA0 to PA6: Page Address

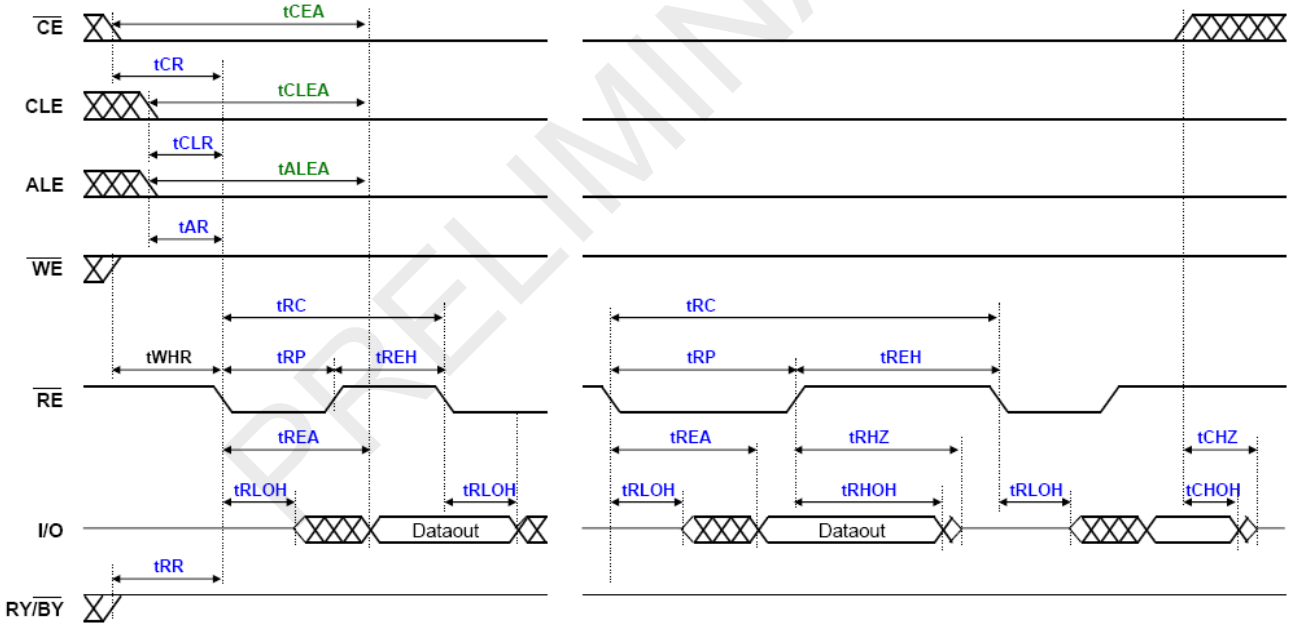
PA7 to PA19: Block Address

3. Timing Diagrams

3.1 Write Timing



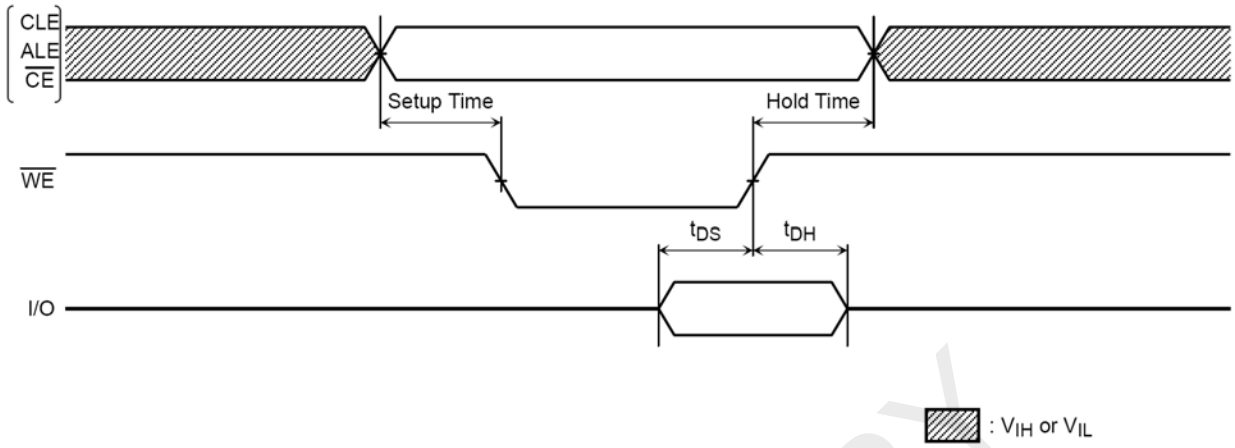
3.2 Read Timing



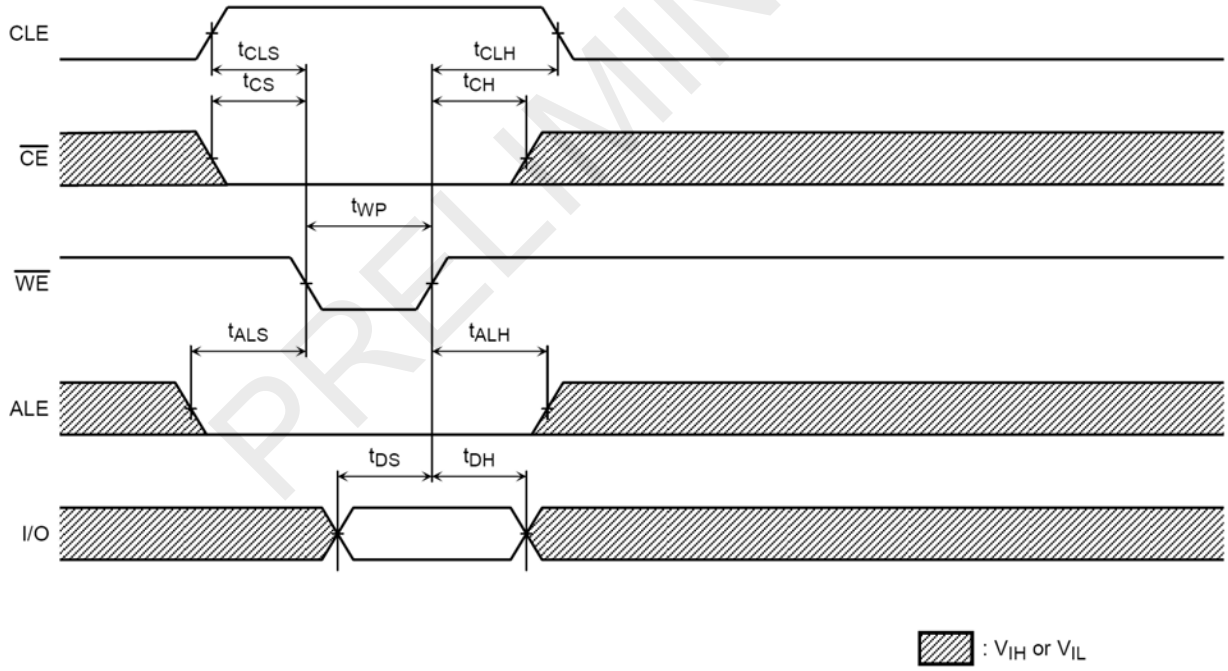
Notes:

1. Hold time from $\overline{RE}$ rising edge is determined by the shorter one of either tRHOH or tREH + tRLOH.
2. When tREH is long, output buffers are disabled by $\overline{RE}$=High, and the hold time of data output depends on tRHOH (30 ns MIN). On this condition, waveforms look like normal serial read mode. (For instance, when tREH = 30ns, it is tRHOH = 30ns.)
3. When tREH is short, output buffers are not disabled by $\overline{RE}$=High, and the hold time of data output depends on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE, ALE, $\overline{CE}$, or the falling edge of $\overline{WE}$, and waveforms look like Extended Data Output Mode. (For instance, when tREH = 10ns, it is tRHOH = tREH + tRLOH = 15ns.)

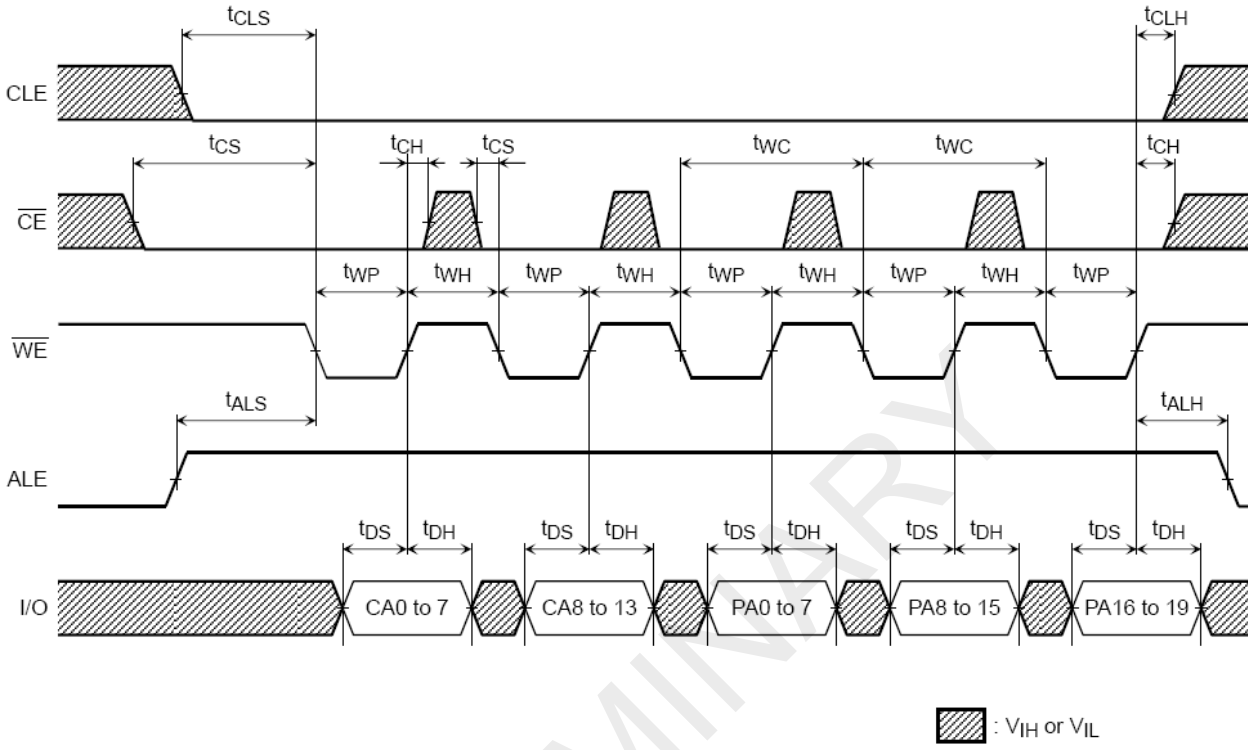
3.3 Latch Timing for Command/Address/Data



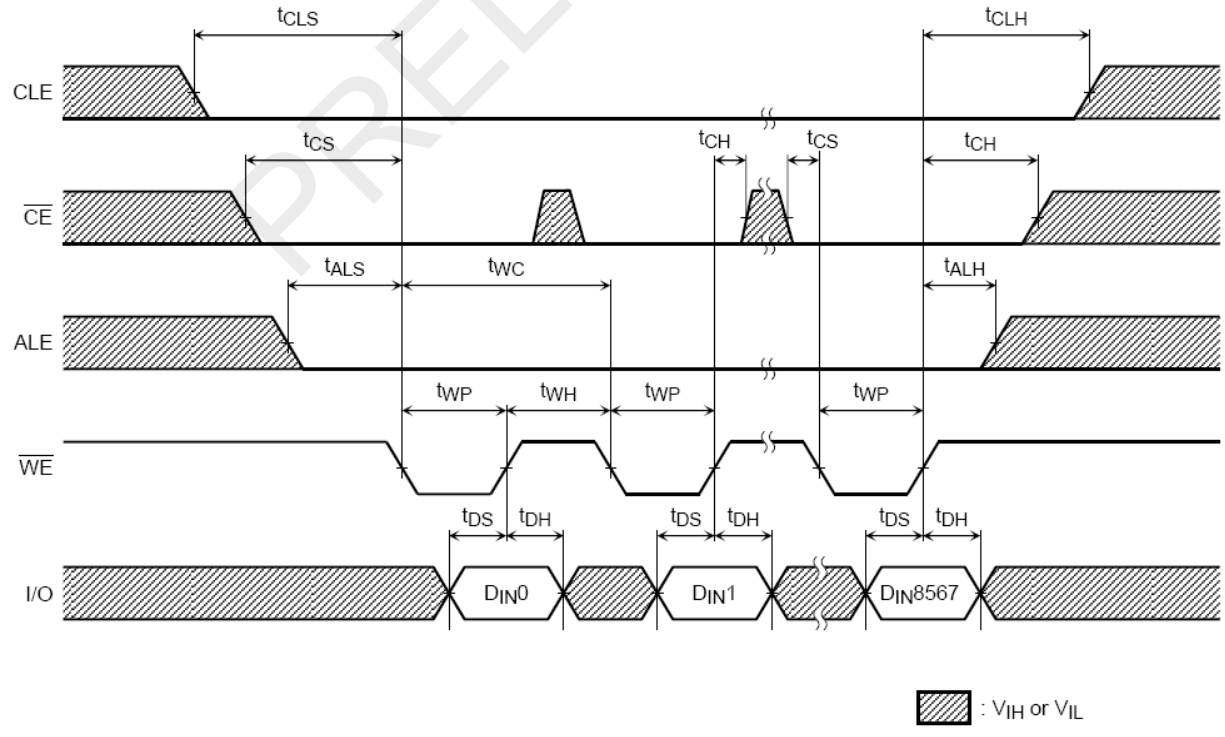
3.4 Command Input Cycle Timing



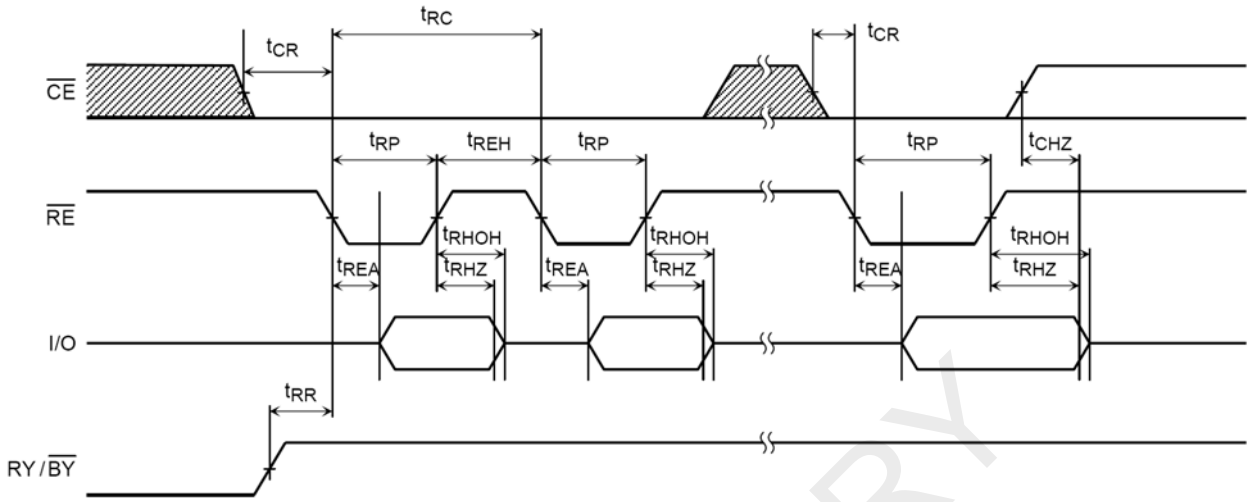
3.5 Address Input Cycle Timing



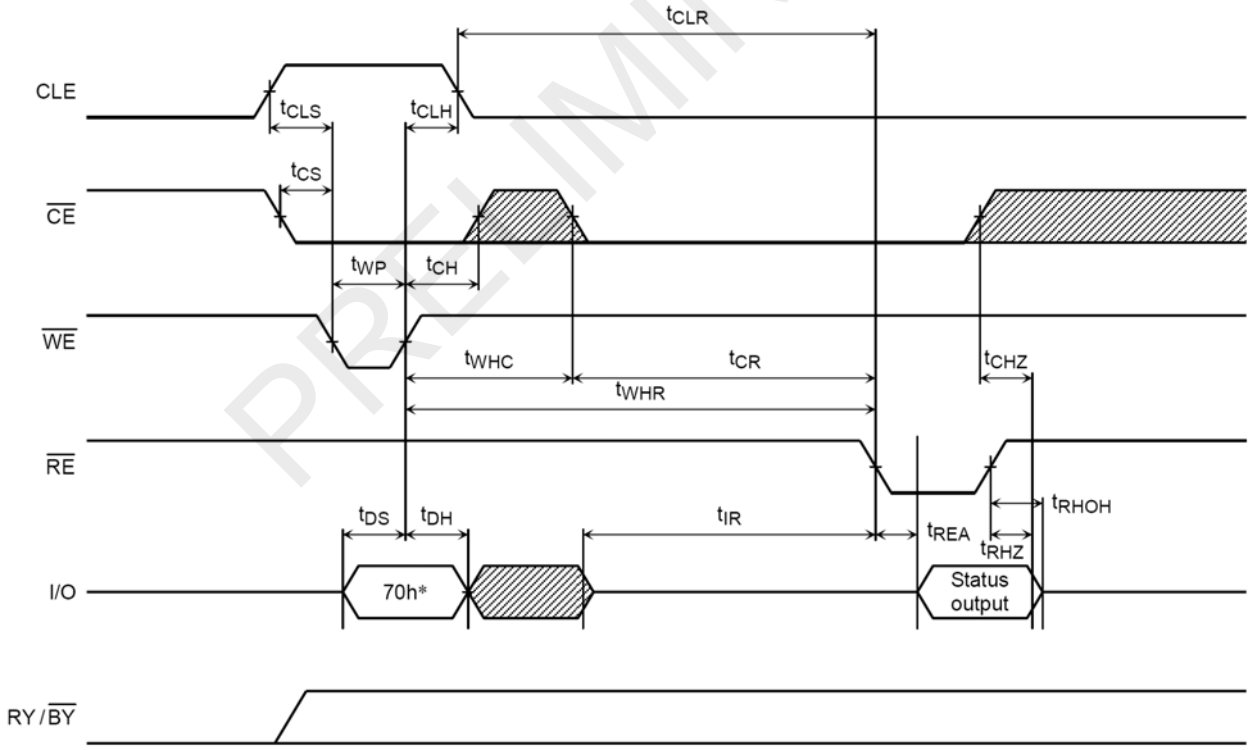
3.6 Data Input Cycle Timing



3.7 Serial Read Cycle Timing



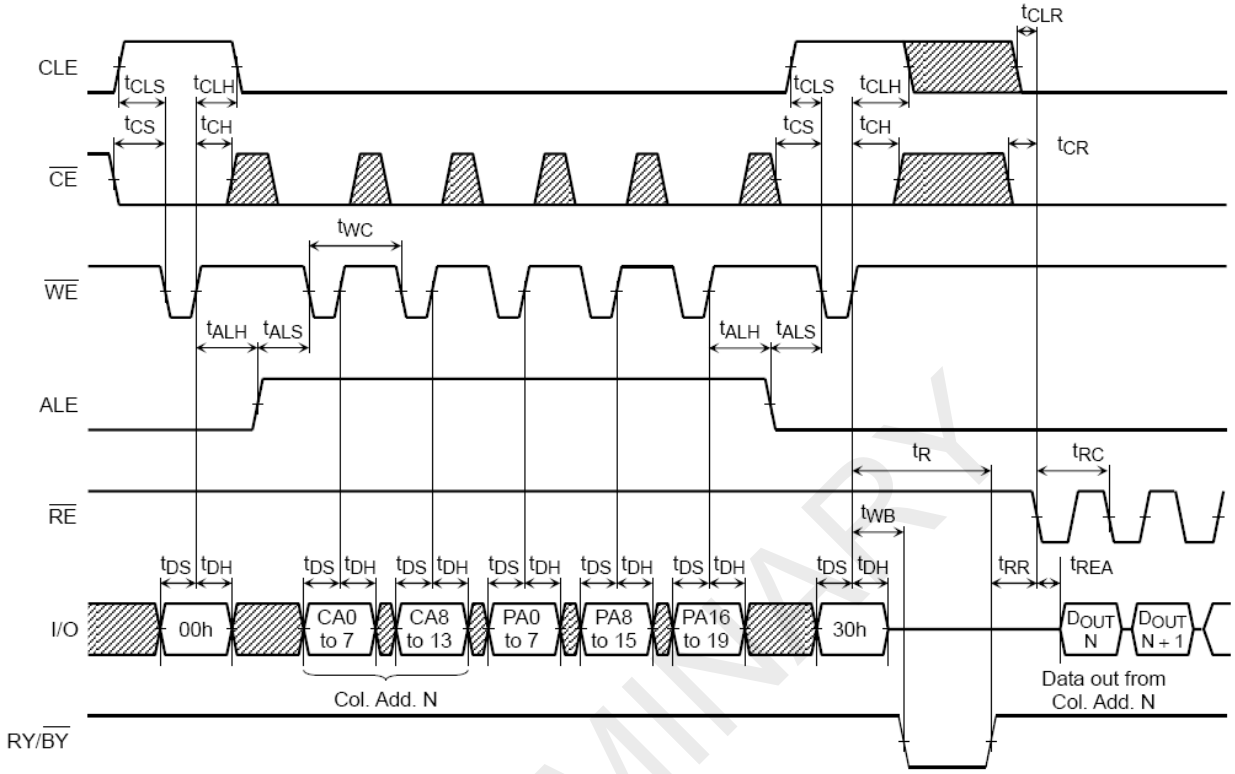
3.8 Status Read Cycle Timing



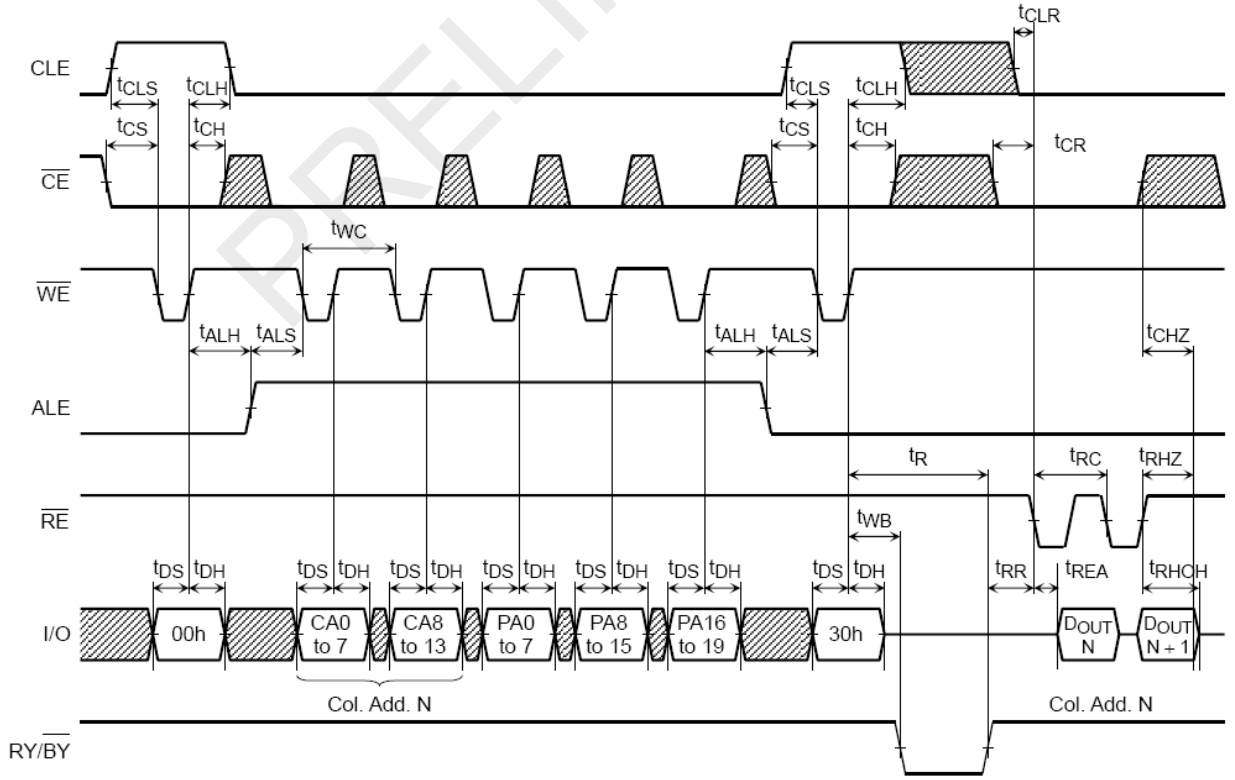
*: 70h represents the hexadecimal number

: V_{IH} or V_{IL}

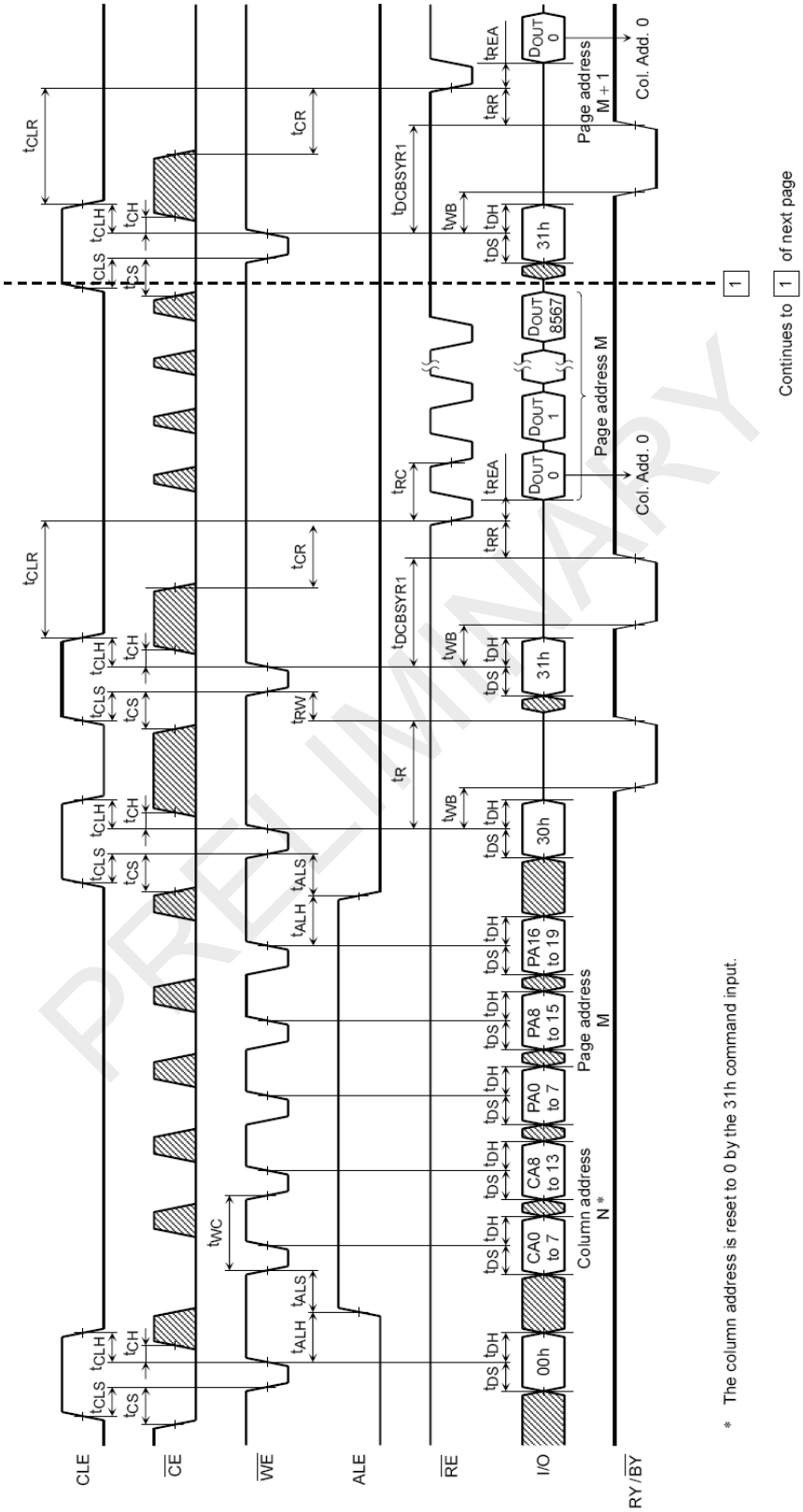
3.9 Read Cycle Timing



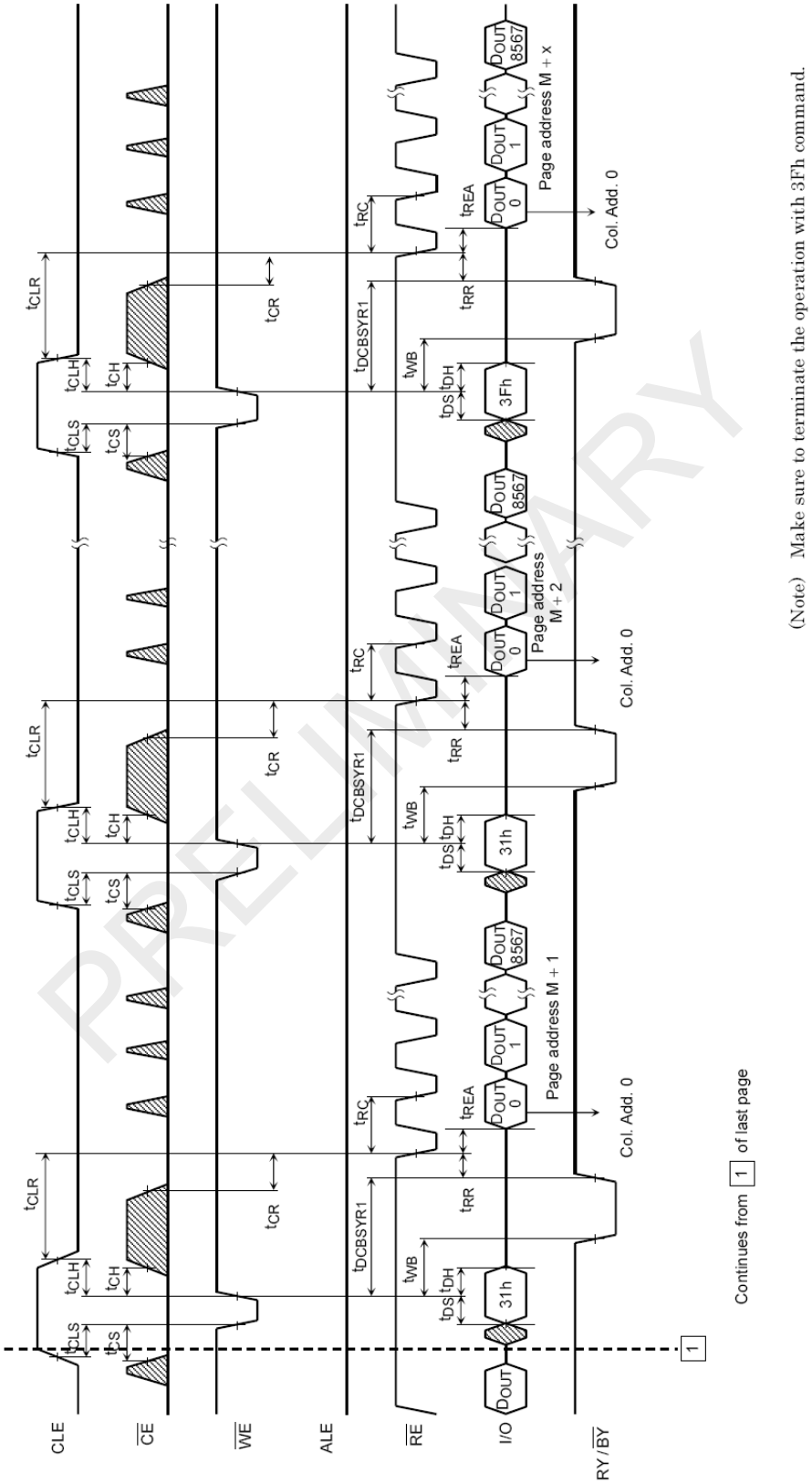
3.10 Read Cycle Timing: When Interrupted by Command Enable



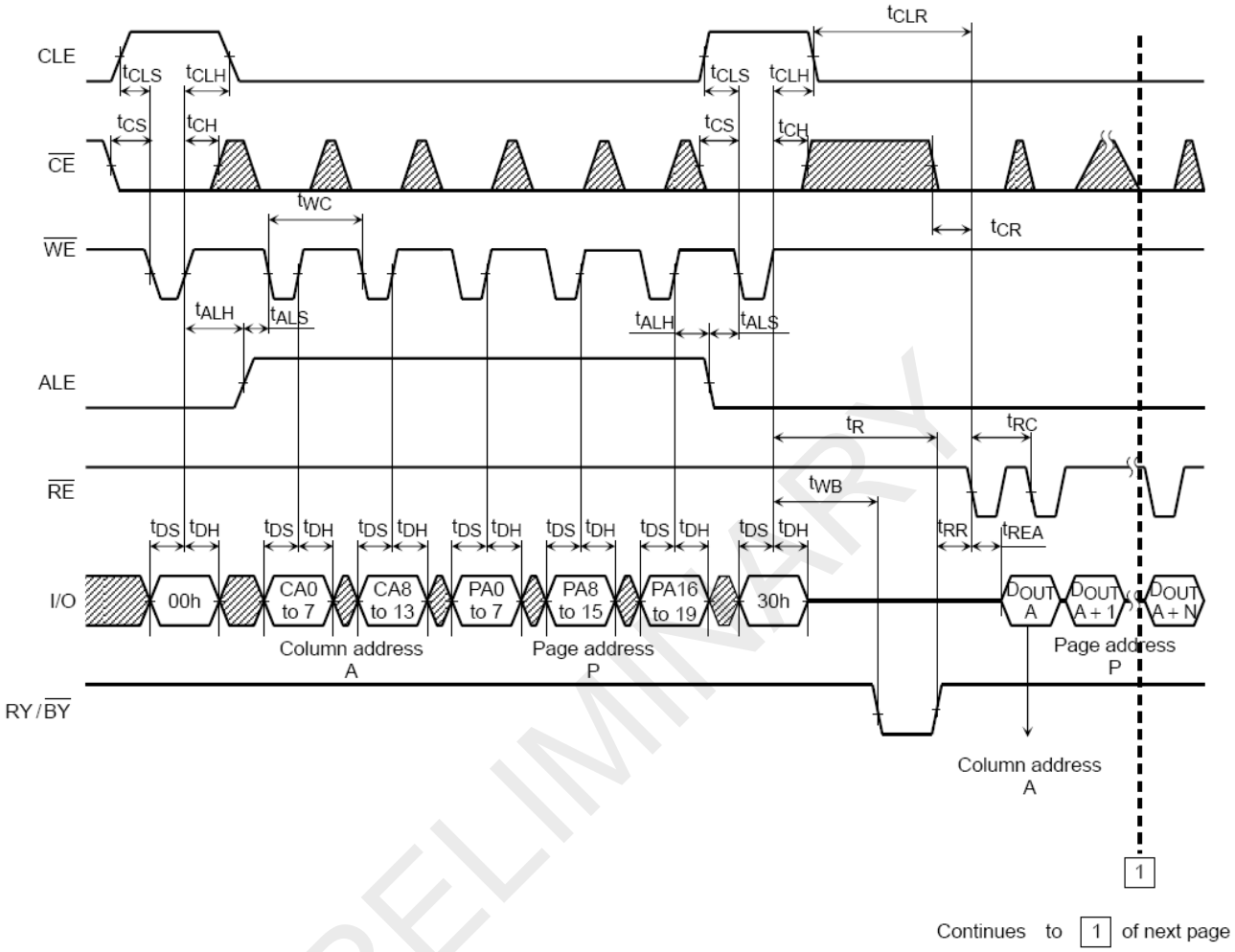
3.11 Read Cycle with Data Cache Timing (1/2)



3.12 Read Cycle with Data Cache Timing (2/2)

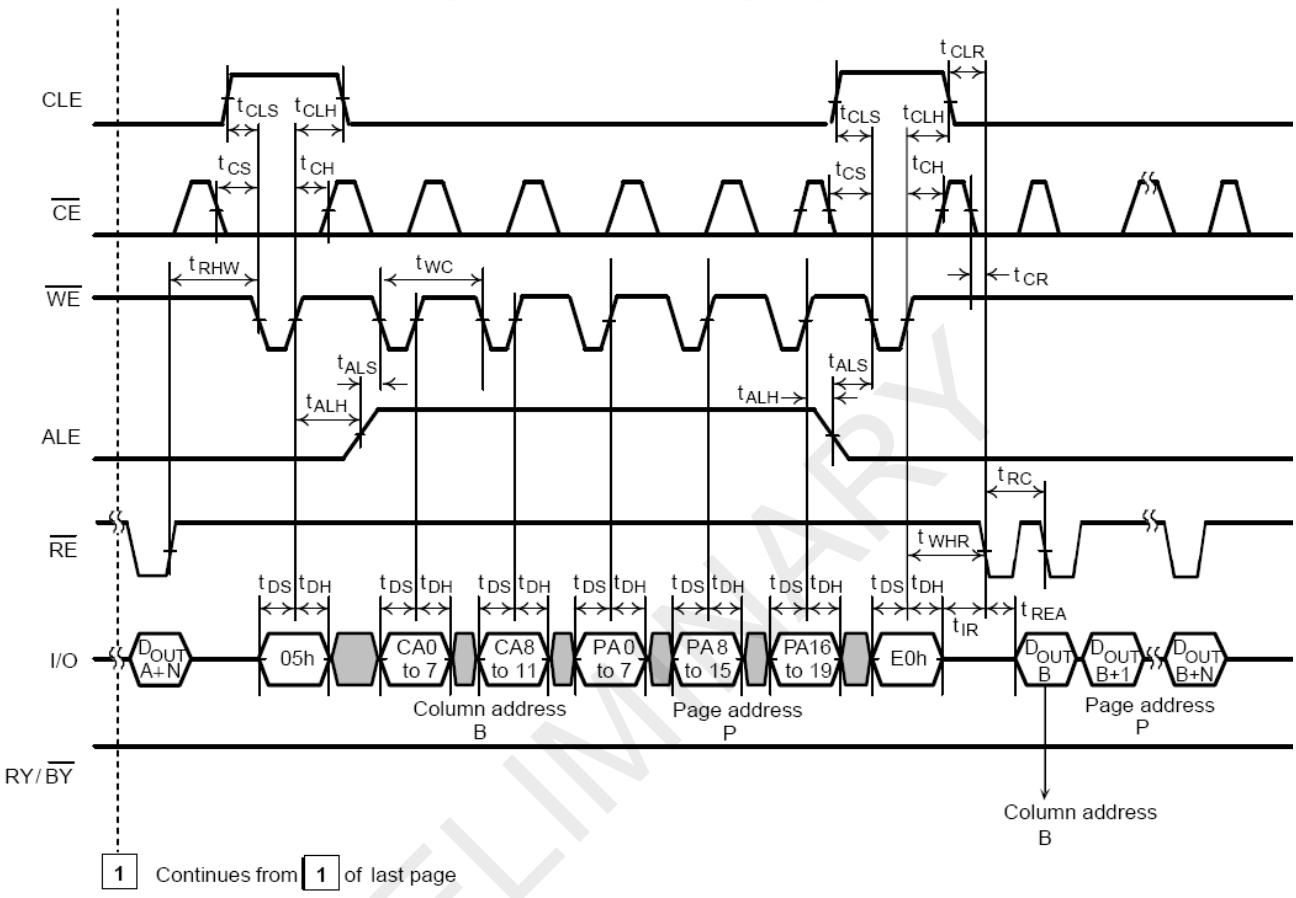


3.13 Column Address Change in Read Cycle Timing (1/2)

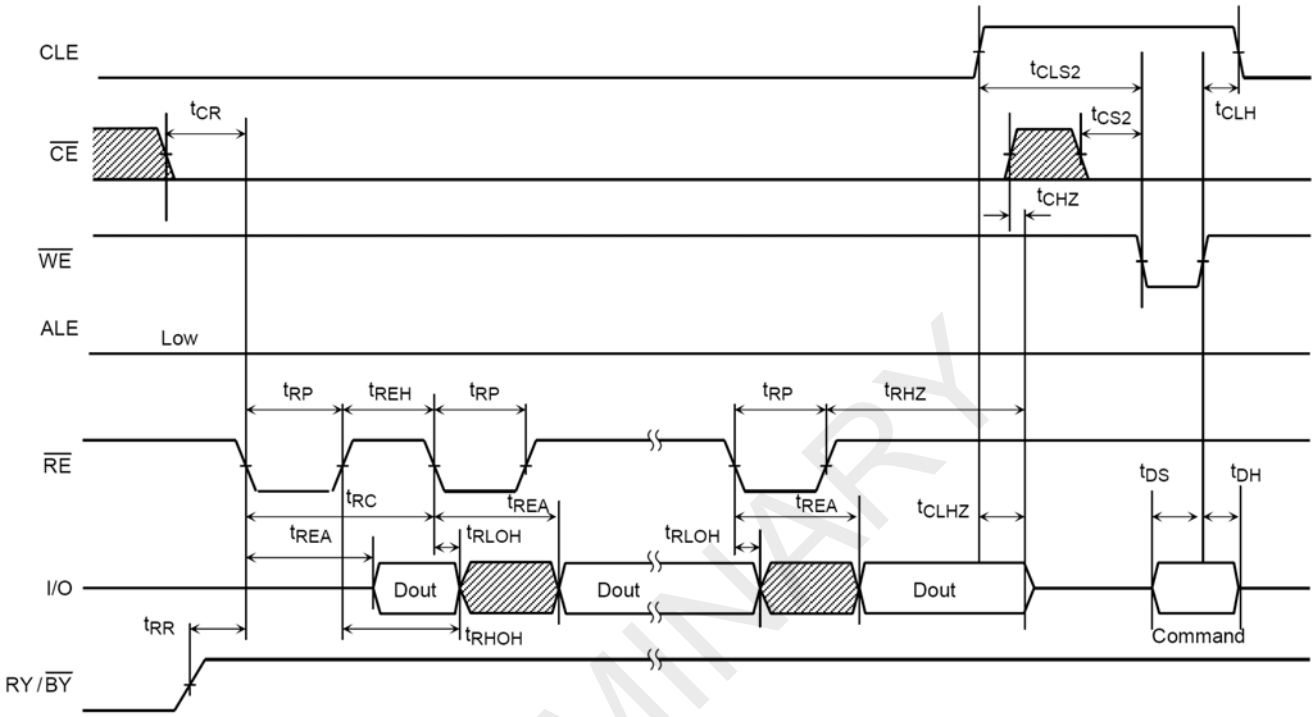


3.14 Column Address Change in Read Cycle Timing (2/2)

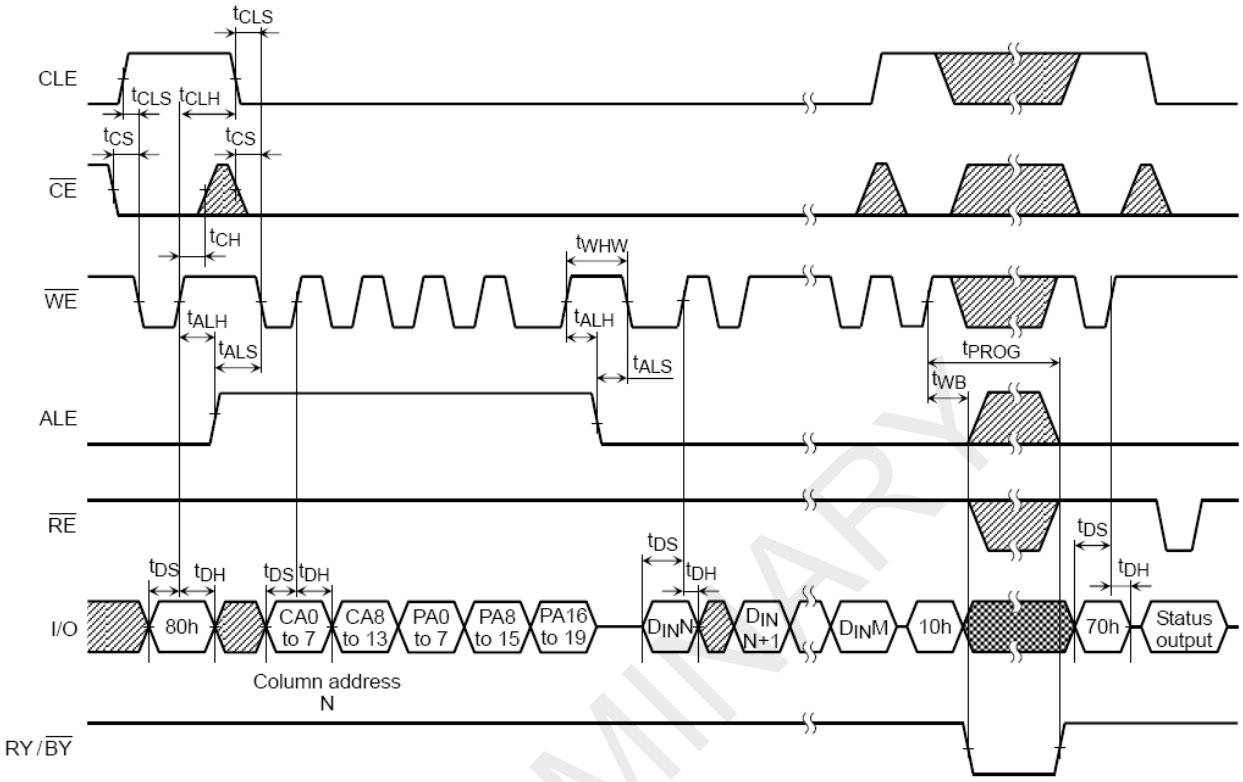
Column Address Change in Read Cycle Timing Diagram (2/2)



3.15 Data Output Timing



3.16 Single Page Program Operation Timing

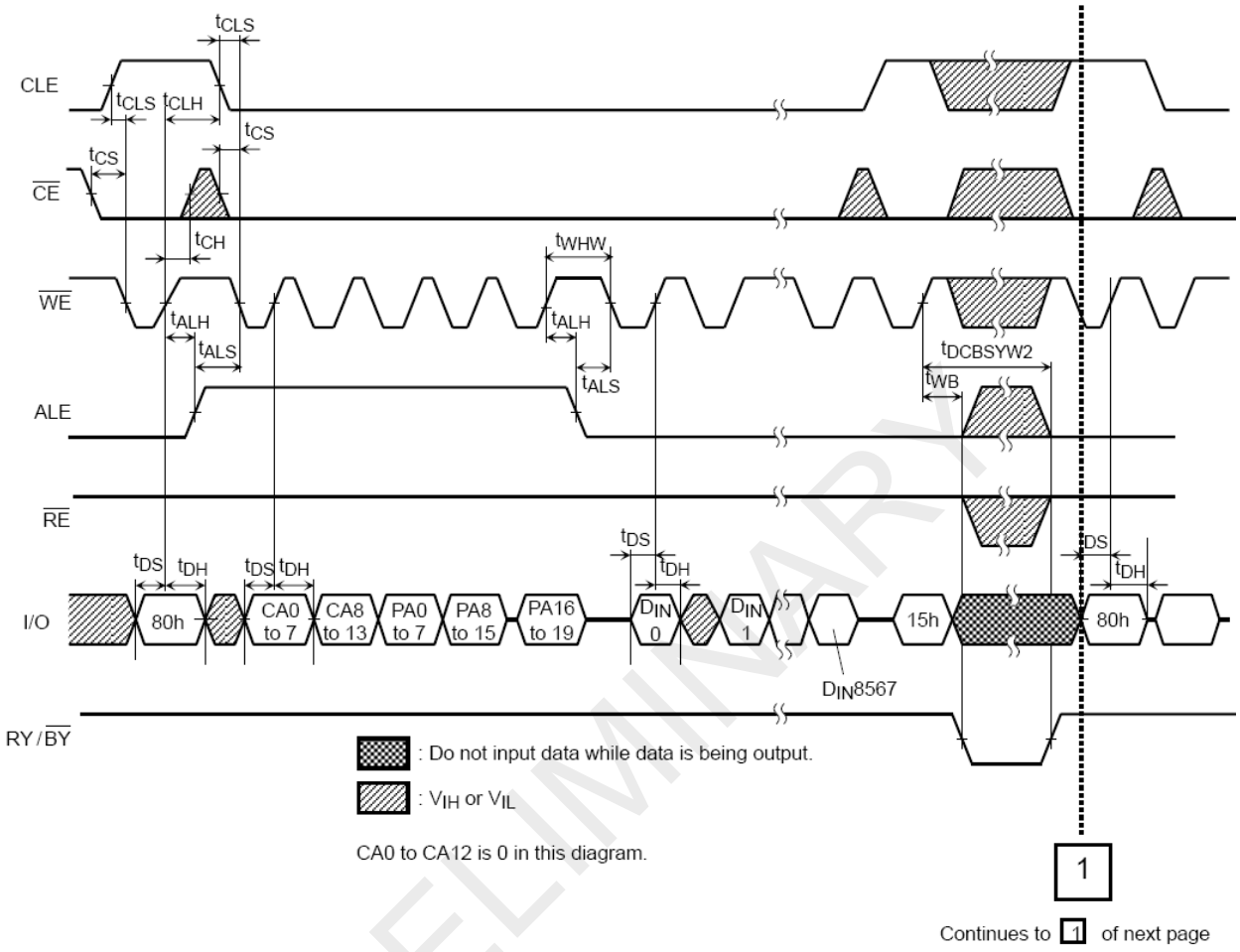


: Do not input data while data is being output.

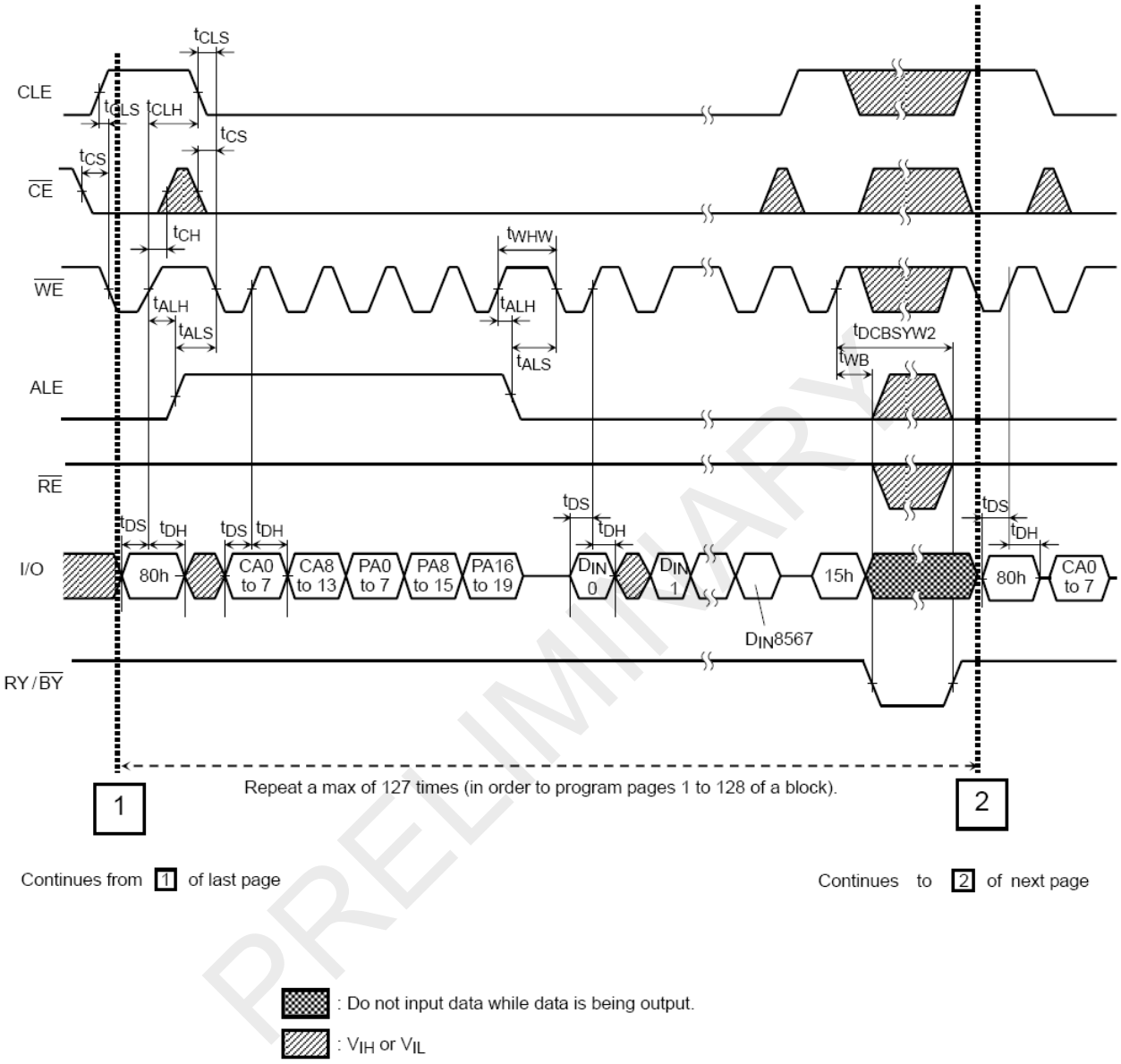
: V_{IH} or V_{IL}

*) M: up to 8567

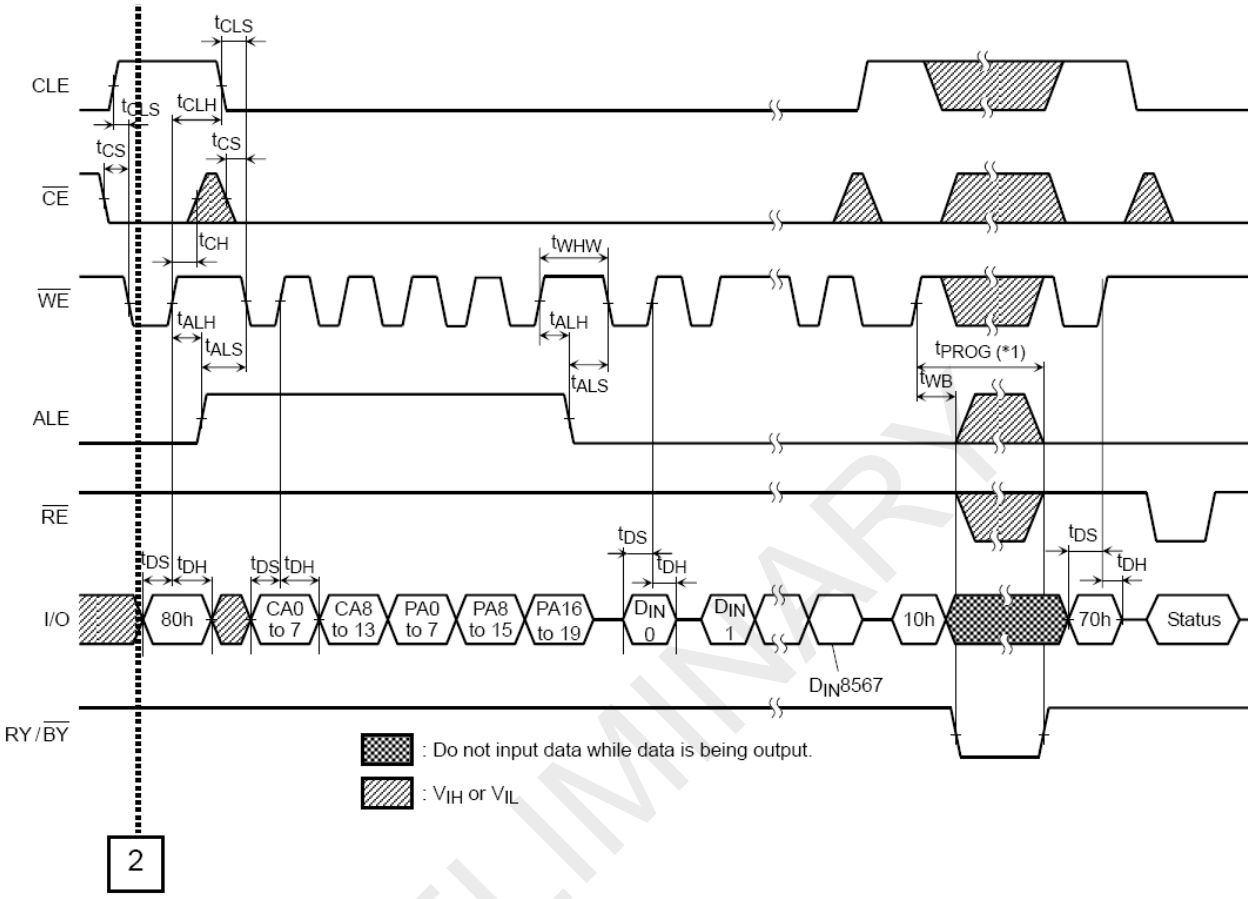
3.17 Auto Page Program with Data Cache Operation Timing (1/3)



3.18 Auto Page Program with Data Cache Operation Timing (2/3)



3.19 Auto Page Program with Data Cache Operation Timing (3/3)



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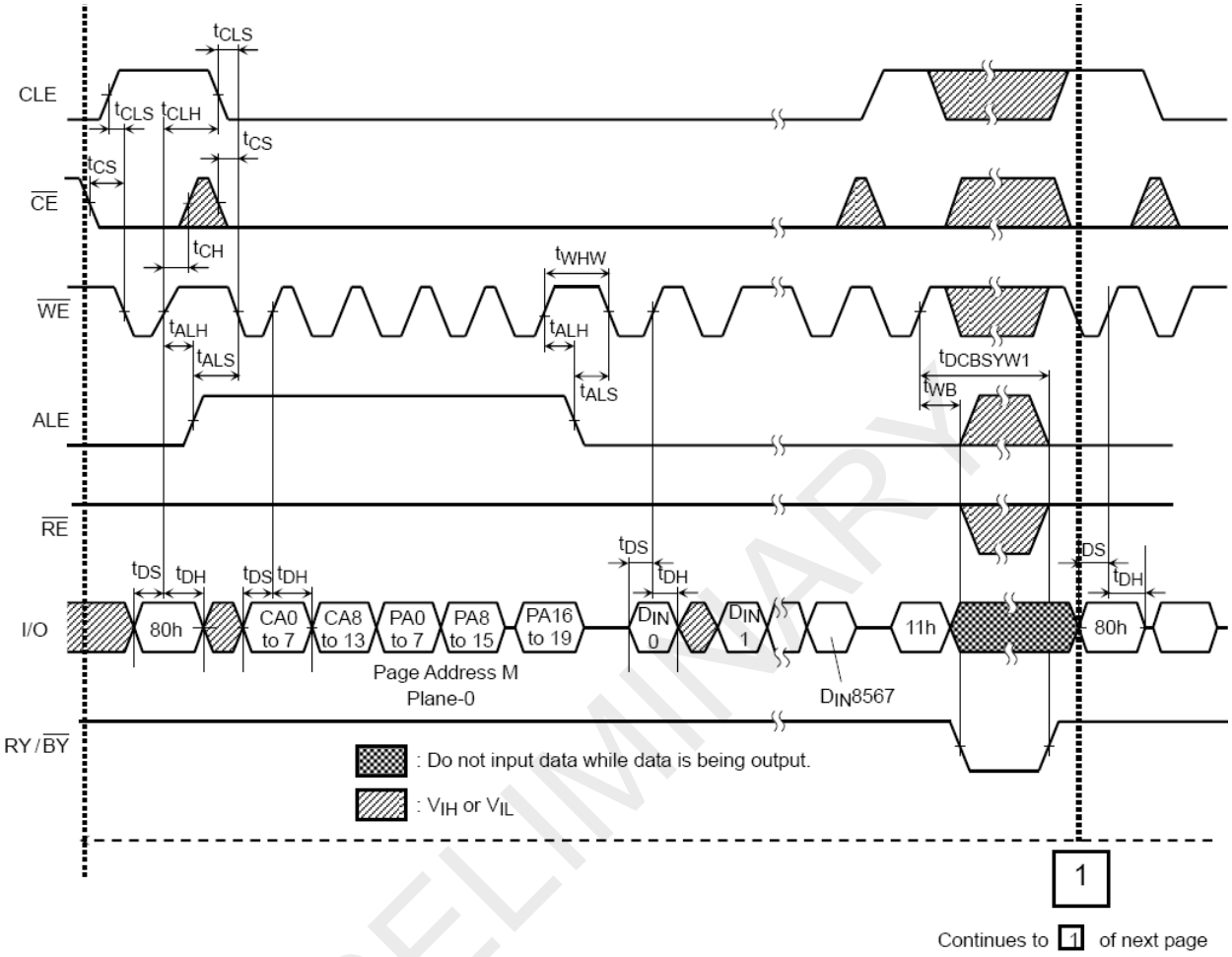
(*1) t_{PROG}: Since the last page programming by the 10h command is initiated after the previous cache program, the t_{PROG} during cache programming is given by the following equation.

tPROG = tPROG of the last page + tPROG of the previous page - A

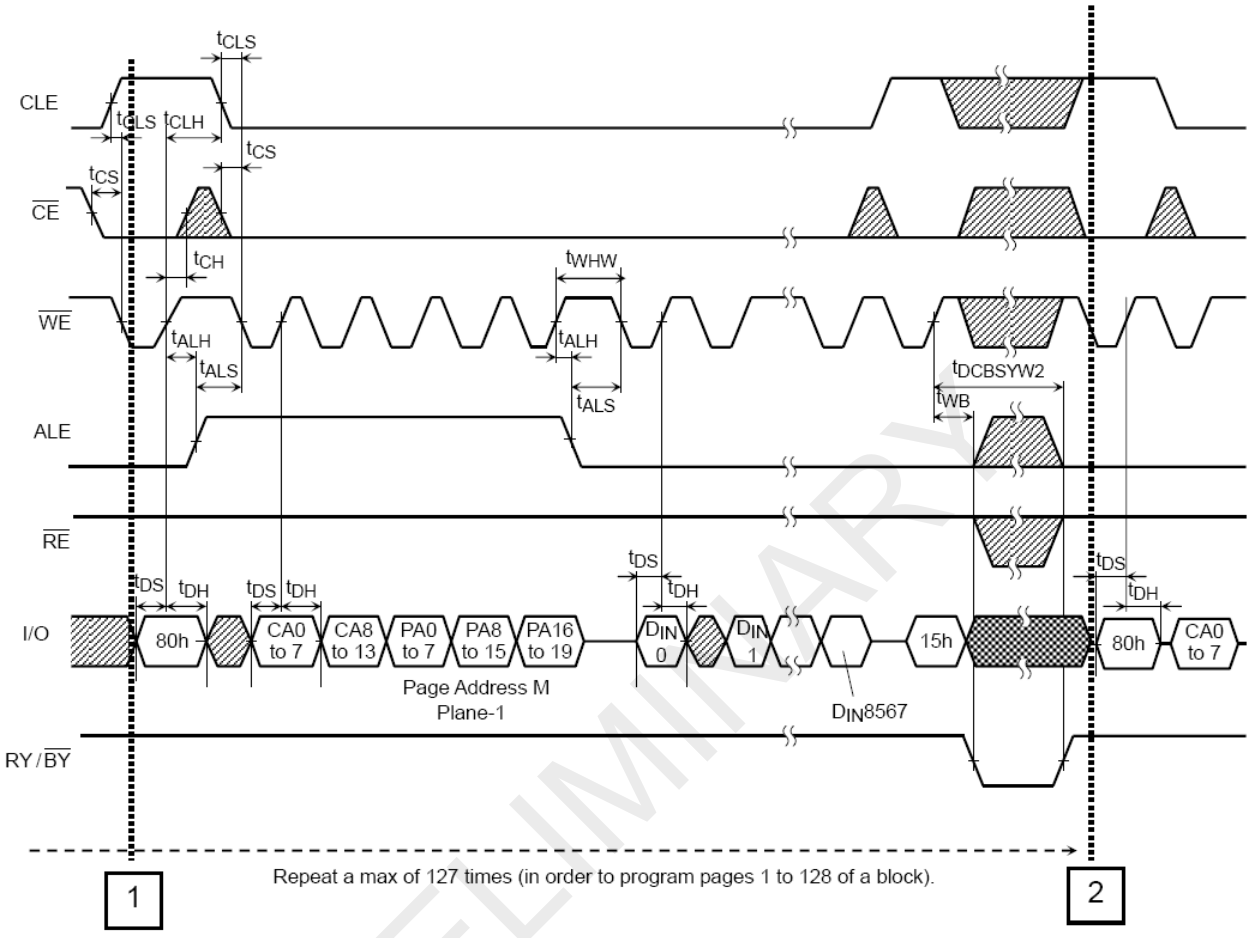
A = (command input cycle + address input cycle + data input cycle time of the last page)

If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

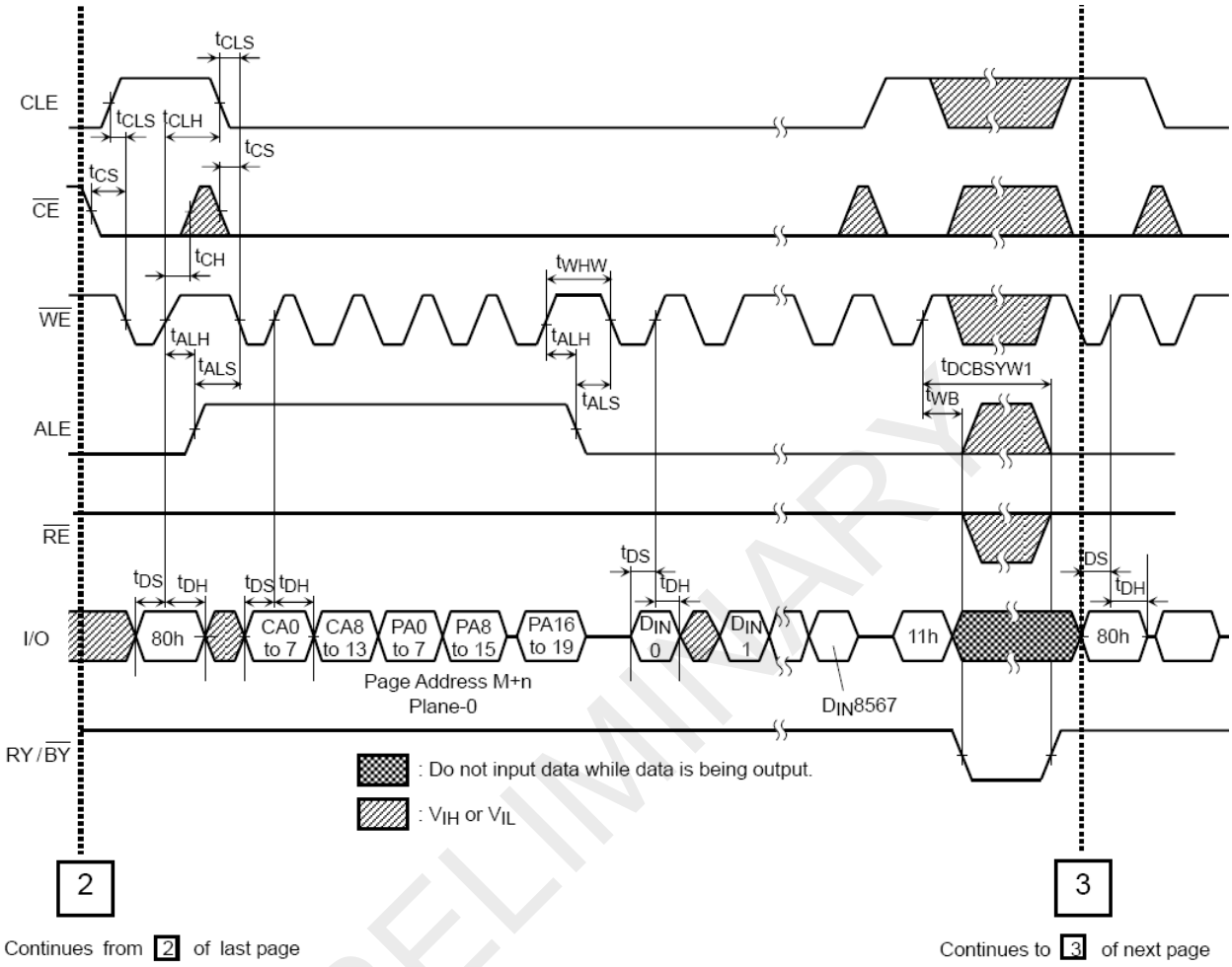
3.20 Multi Page Program with Data Cache Operation Timing (1/4)



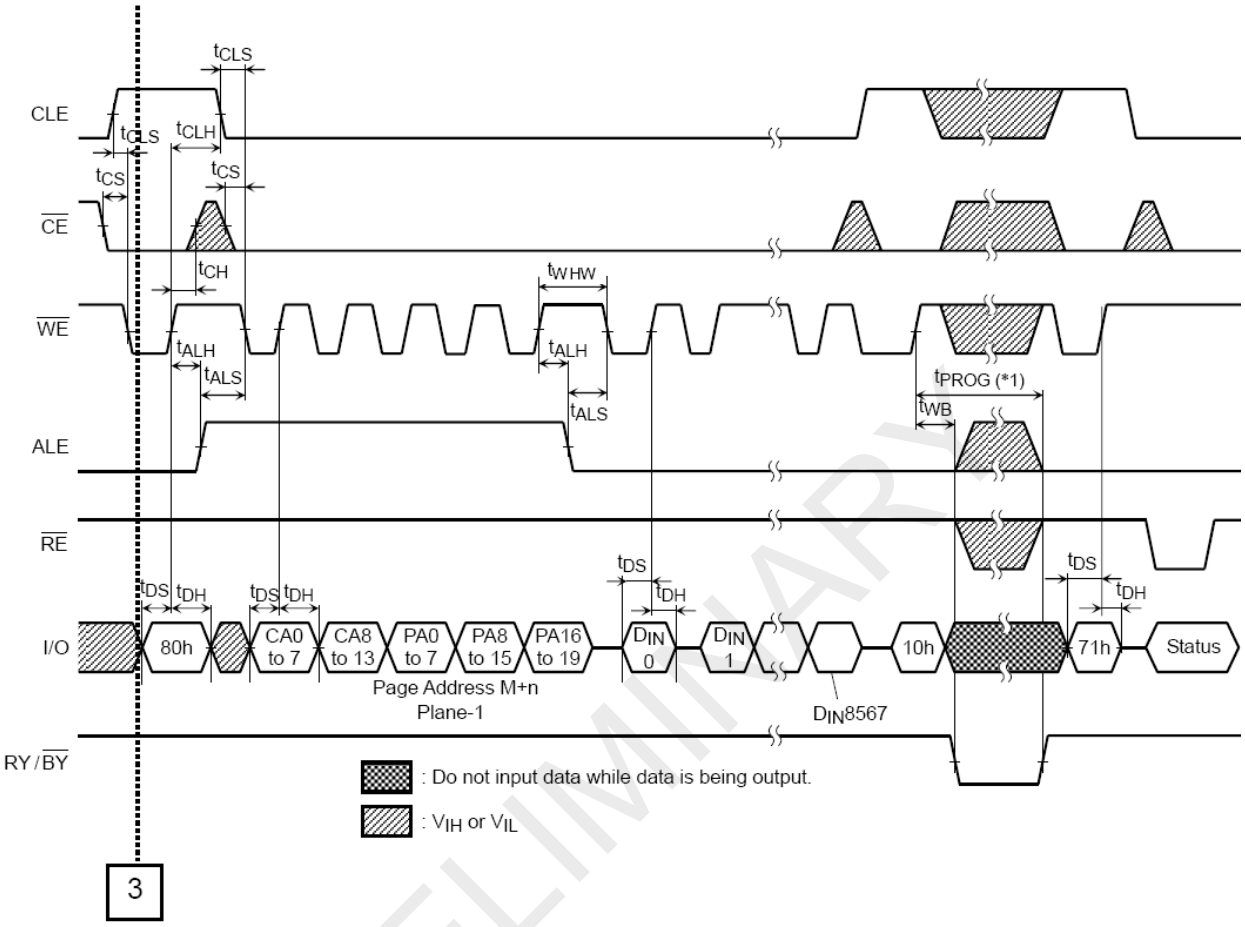
3.21 Multi Page Program with Data Cache Operation Timing (2/4)



3.22 Multi Page Program with Data Cache Operation Timing (3/4)



3.23 Multi Page Program with Data Cache Operation Timing (4/4)



Continued from 3 of last page

(*1) t_{PROG}: Since the last page programming by the 10h command is initiated after the previous cache program, the t_{PROG} during cache programming is given by the following equation.

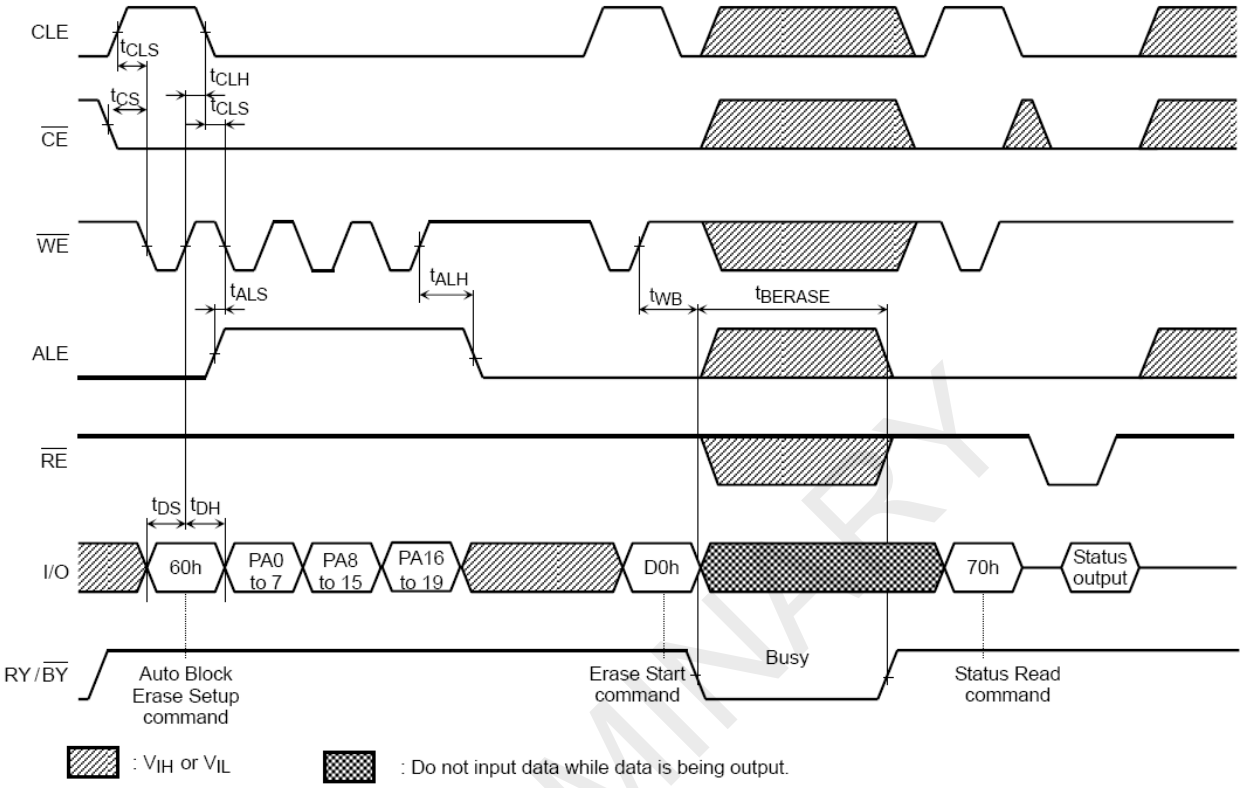
tPROG = tPROG of the last page + tPROG of the previous page - A

A = (command input cycle + address input cycle + data input cycle time of the last page)

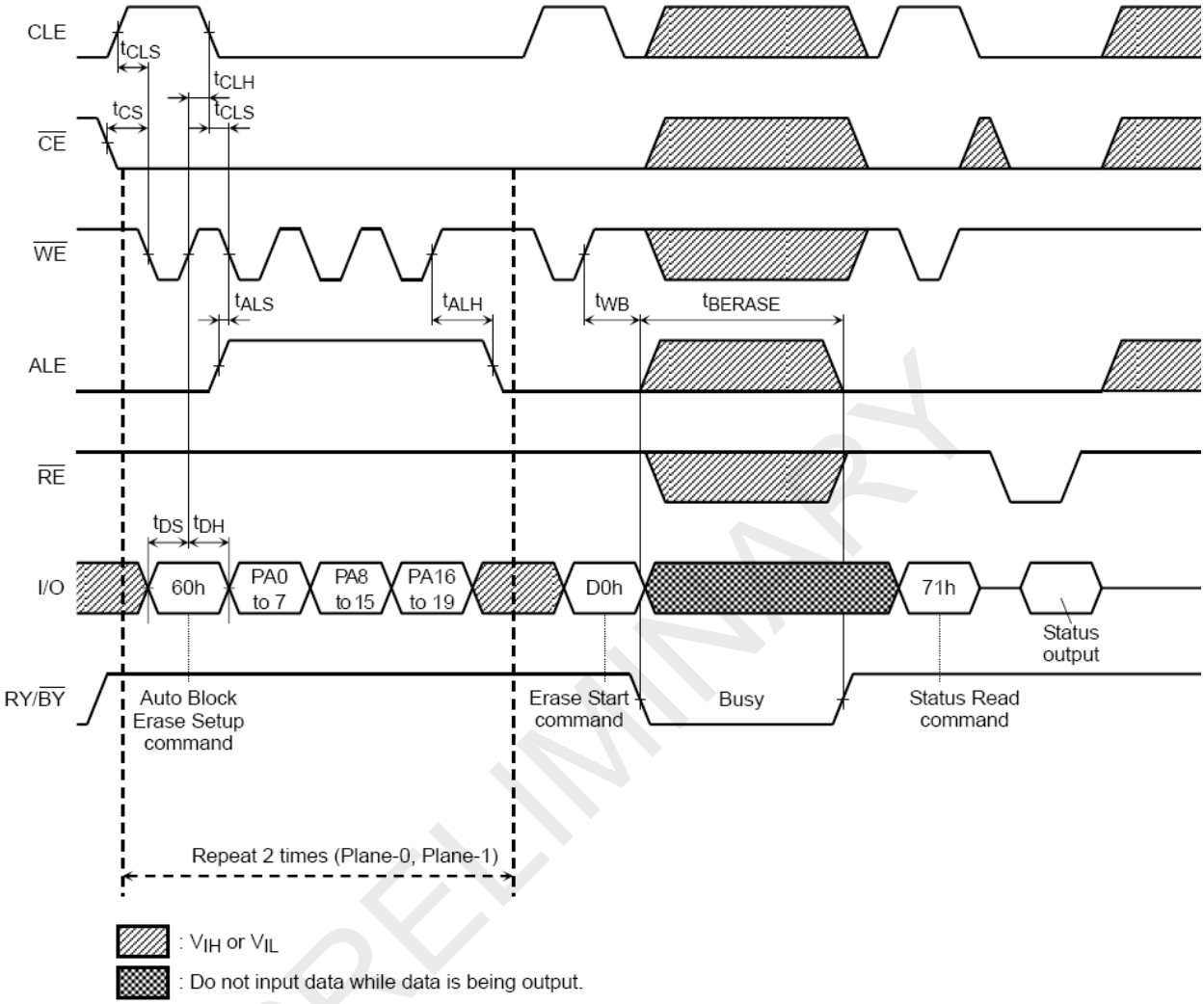
If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

(Note) Make sure to terminate the operation with an 80h-10h command sequence.
If the operation is terminated by an 80h-15h command sequence, monitor I/O5 (Ready / Busy) by issuing a Status Read command (70h), and make sure the previous page program operation has completed. If the page program operation has completed, issue an FFh reset before the next operation.

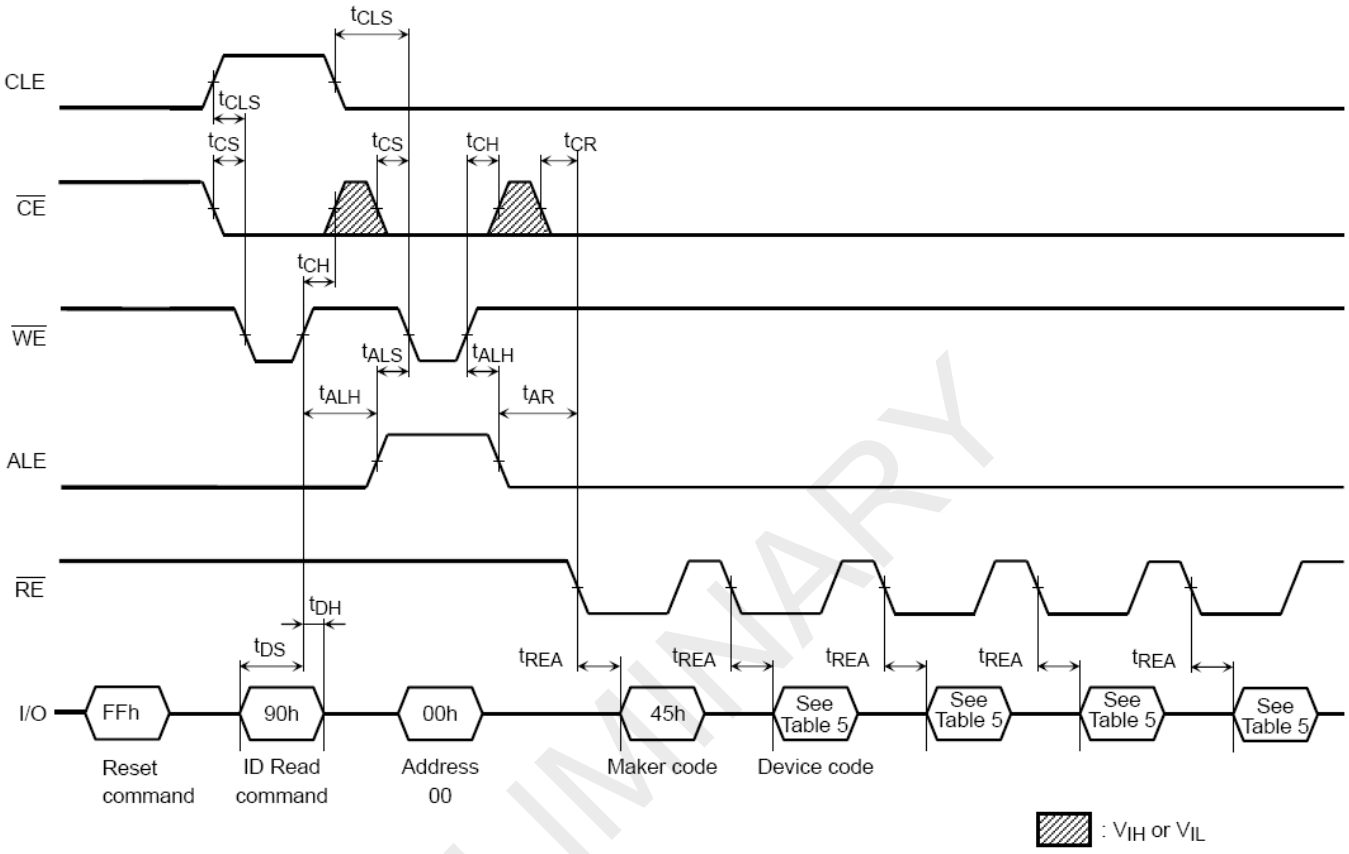
3.24 Single Block Erase Timing



3.25 Multi Block Erase Timing



3.26 ID Read Operation Timing



4. Operation Mode: Logic and Command Tables

4.1 Logic Table

Operation modes such as Program, Erase, Read, and Reset are controlled by command operations shown in Table 3. Address input, command input, and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L		H	*
Data Input	L	L	L		H	H
Address input	L	H	L		H	*
Serial Data Output	L	L	L	H		*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to the "Write Protect Signal" section for details regarding Program and Erase operations when the $\overline{WP}$ signal goes Low.

*2: If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read commands can be input during Read (Busy).

4.2 Command Table

Table 3: Command Table (HEX)

Command	First Cycle	Second Cycle	Third Cycle	Acceptable while Busy
Auto Page Program with Data Cache (See note 1.)	80	15	–	
Column Address Change in Serial Data Output	05	E0	–	
Column Address in Serial Data Input	85	–	–	
ID Read	90	–	–	
Multi Block Erase	60	60	D0	
Multi Page Program	80	11	–	
Multi Page Read	60	60	30	
Multi Page Read during Multi Page Copy (2)	60	60	3A	
Read for Page Copy (2)	00	3A	–	
Read Start for Last Page in Read cycle with Data Cache	3F	–	–	
Read with Data Cache	31	–	–	
Reset	FF	–	–	O
Serial Data Input	80	–	–	
Single Block Erase	60	D0	–	
Single Page Program	80	10	–	
Single Page Program during Multi Page Copy (2) (See note 1.)	8C	11	–	
Single Page Program for last page during Page Copy (2) (See note 1.)	8C	10	–	
Single Page Program with Data Cache during Page Copy (2) (See note 1.)	8C	15	–	
Single Page Read	00	30	–	
Status Read	70	–	–	O
Status Read for Multi Page Program or Multi Block Erase	71	–	–	O

Notes: **1. Input of a command other than those specified in Table 3 is prohibited. Stored data can be corrupted if an unknown command is entered during the command cycle.**

2. During the Busy state, do not input any command except 70h(71h) and FFh.

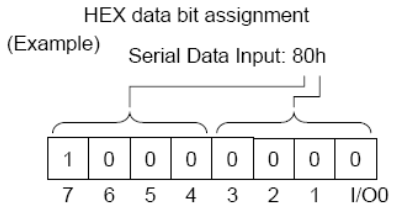


Table 4 shows the operation states for Read mode, when tREH is long.

Table 4. Read Mode Operation States

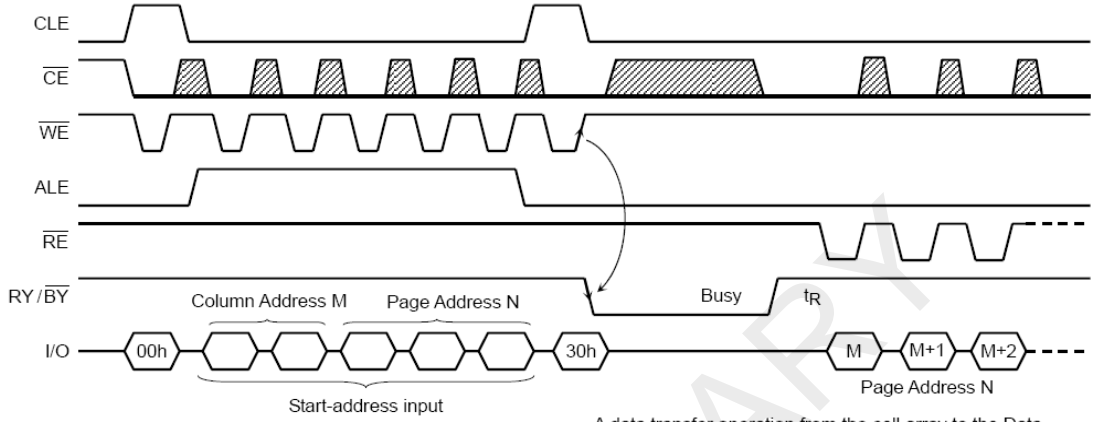
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O0 to I/O7	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

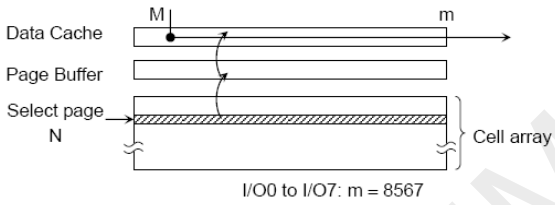
H: V_{IH}, L: V_{IL}

5. Device Operation

5.1 Read Mode

Read mode is set when the "00h" and "30h" commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. Refer to the figures below for the sequence and the block diagram (Refer to the detailed timing chart.).

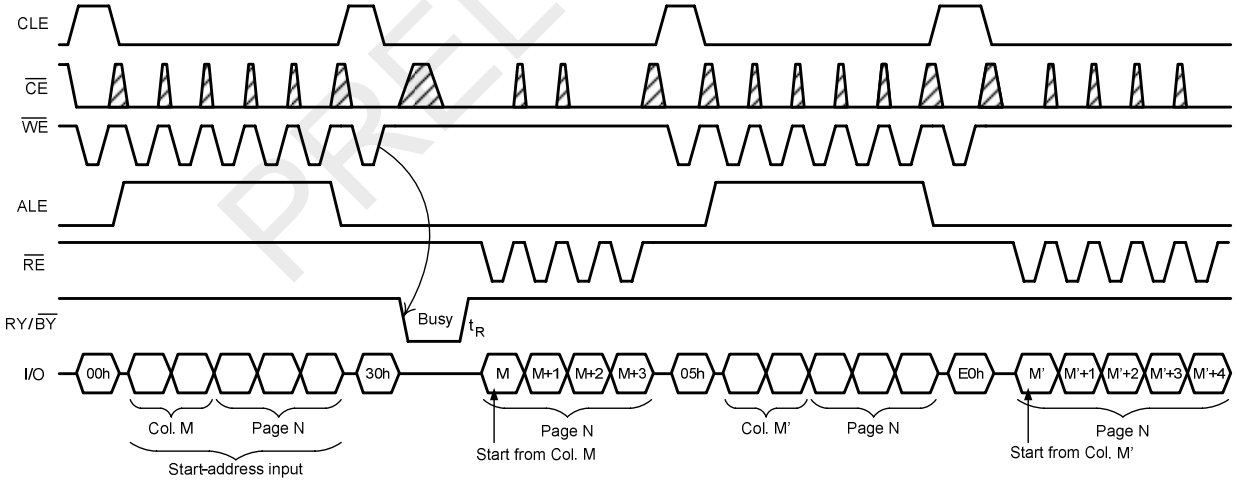


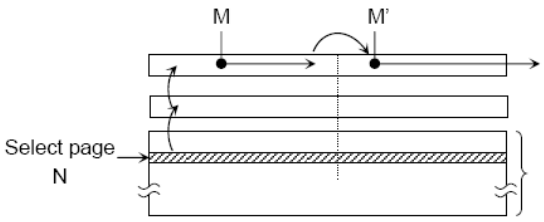


A data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

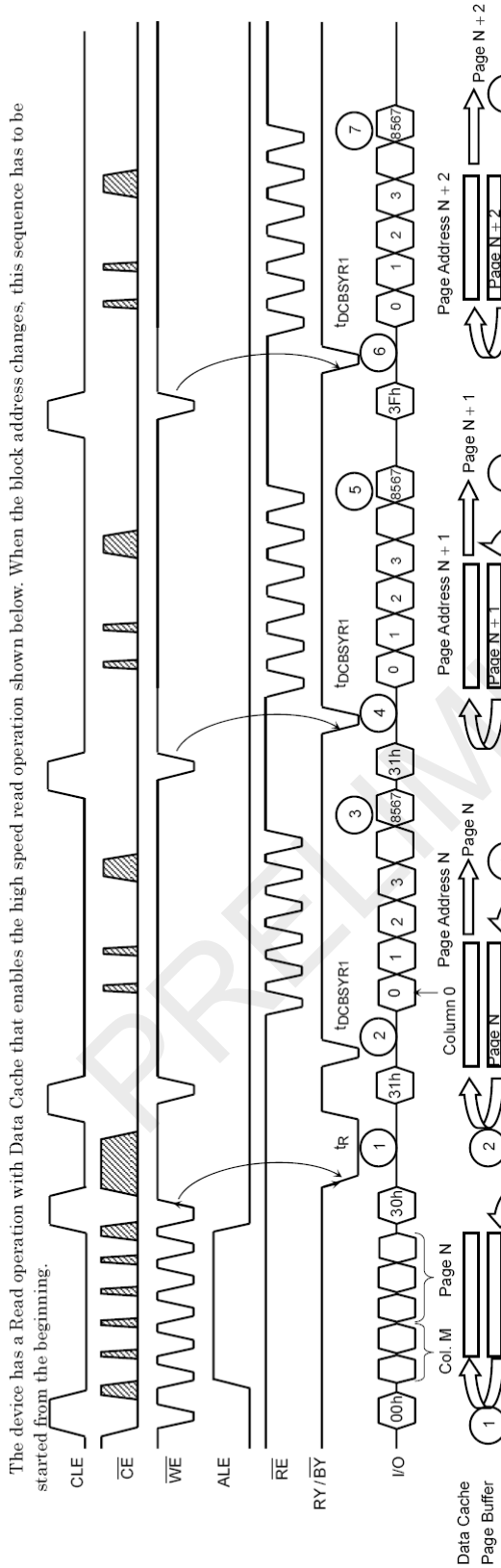
5.2 Random Column Address Change in Read Cycle





During the serial data output from the Data Cache, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.

5.3 Read Operation with Read Cache



The device has a Read operation with Data Cache that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning.

If the 31h command is issued to the device, the data content of the next page is transferred to the Page Buffer during serial data out from the Data Cache, and therefore the tR (Data transfer from memory cell to data register) will be reduced.

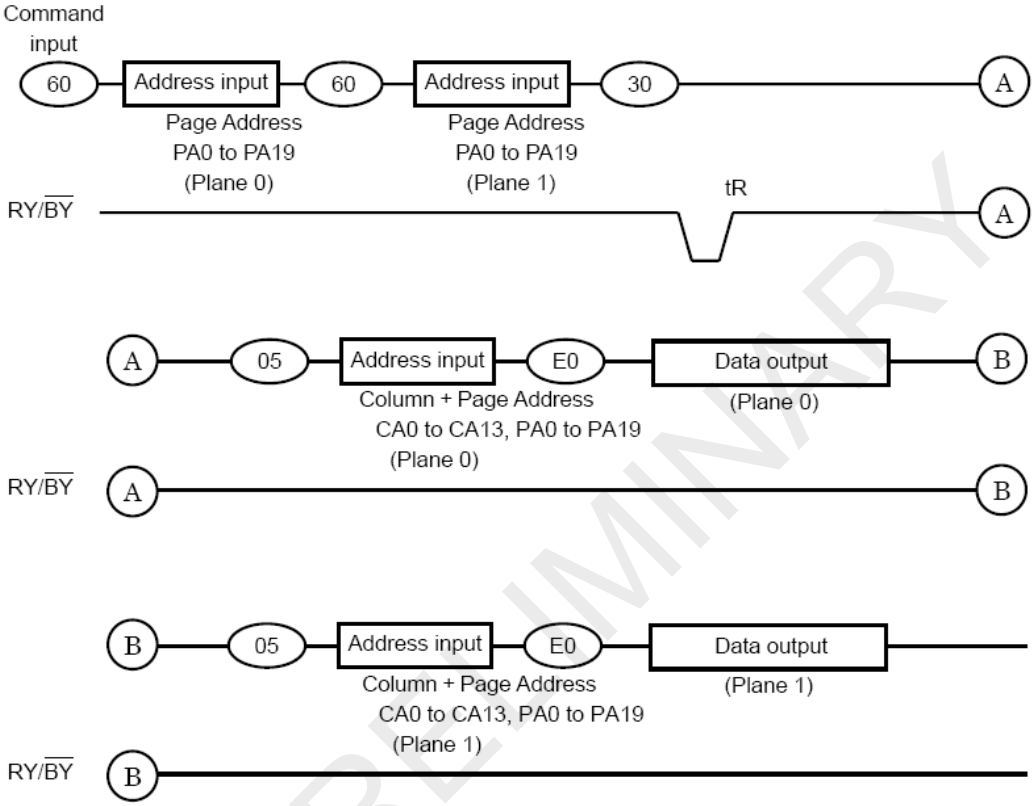
1 Normal read. Data is transferred from Page N to Data Cache through Page Buffer. During this time period, the device outputs Busy state for tR max.
2 After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to Data Cache from Page Buffer again. This data transfer takes tDCBSYR1 max and the completion of this time period can be detected by Ready/Busy signal.
3 Data of Page N + 1 is transferred to Page Buffer from cell while the data of Page N in Data cache can be read out by /RE clock simultaneously.
4 The 31h command makes data of Page N + 1 transfer to Data Cache from Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.
5 Data of Page N + 2 is transferred to Page Buffer from cell while the data of Page N + 1 in Data cache can be read out by /RE clock simultaneously
6 The 3Fh command makes the data of Page N + 2 transfer to the Data Cache from the Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.
7 Data of Page N + 2 in Data Cache can be read out, but since the 3Fh command does not transfer the data from the memory cell to Page Buffer, the device can accept new command input immediately after the completion of serial data out.

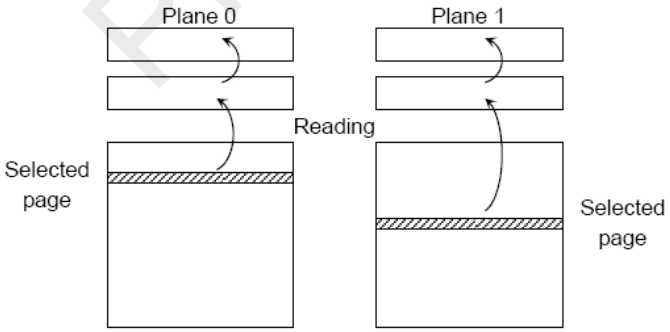
5.4 Multi Page Read Operation

The device has a Multi Page Read operation and Multi Page Read with Data Cache operation..

(1) Multi Page Read without Data Cache

The sequence of command and address input is shown below.
Same page address (PA0 to PA6) within each Plane must be selected.



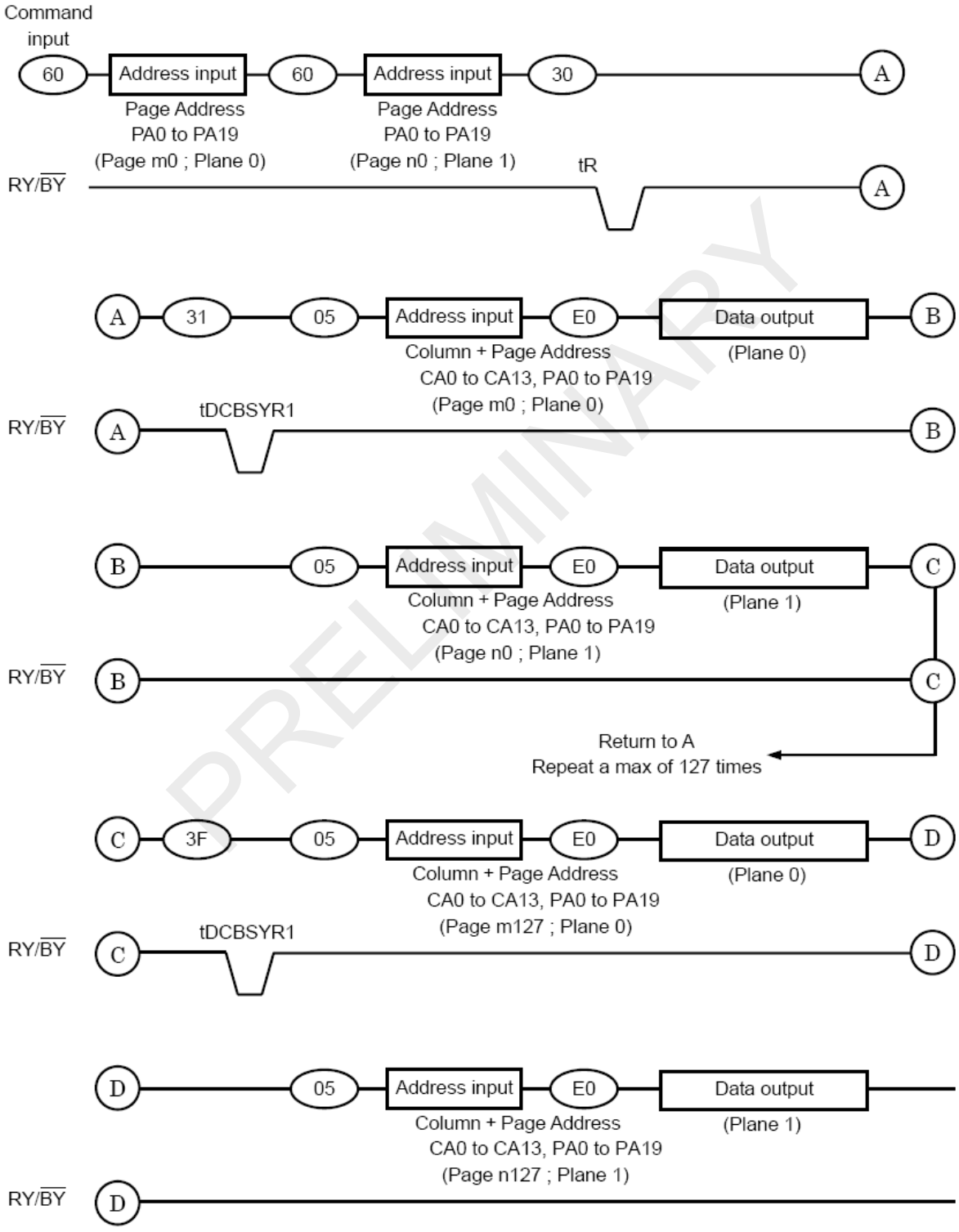


The data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the 2 Planes address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

(2) Multi Page Read with Data Cache

When the block address changes (increments) this sequence must be started from the beginning.
The sequence of command and address input is shown below.
Same page address (PA0 to PA6) within each Plane must be selected.



(3) Notes

(a) Internal addressing in relation to the Planes

When using a Multi Page Read operation, internal addressing should be considered in relation to the Plane.

- The device consists of 2 Planes.
- Each Plane consists of 2048 erase blocks.
- The allocation rule is as follows:
  Plane 0: Block 0, Block 2, Block 4, Block 6, ···, Block 4094
  Plane 1: Block 1, Block 3, Block 5, Block 7, ···, Block 4095

- For 32GB with 4 $\overline{CE}$ control pins, each Plane has 4096 erase blocks:
  Plane 0: Block 0, Block 2, Block 4, Block 6,···, Block 8190
  Plane 1: Block 1, Block 3, Block 5, Block 7,···, Block 8191

(b) Address input restriction for the Multi Page Read operation

The following restrictions exist when using Multi Page Read;

(Restriction)
A maximum of one block should be selected from each Plane.
The same page address (PA0 to PA6) within each Plane must be selected.
For example;
(60) [Plane 0, Page Address 0x00000] (60) [Plane 1, Page Address 0x00000] (30)
(60) [Plane 0, Page Address 0x00001] (60) [Plane 1, Page Address 0x00001] (30)

(Acceptance)
There is no order limitation on the Plane for the address input.
An address from either Plane can be entered first.
For example, either one of the following operations is accepted;
(60) [Plane 0] (60) [Plane 1] (30)
(60) [Plane 1] (60) [Plane 0] (30)

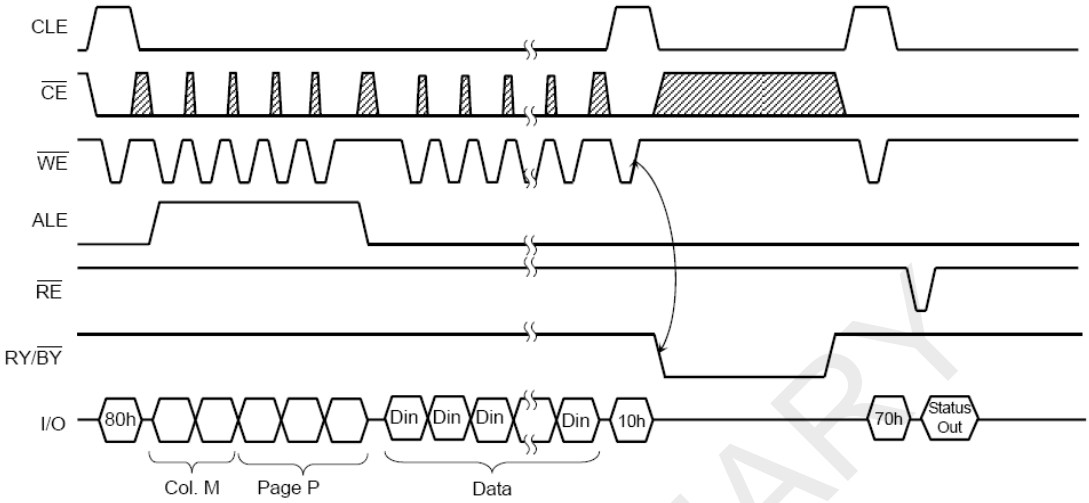
Any valid block address from each Plane can be entered. The selected block addresses from the two Planes do not need to be related.

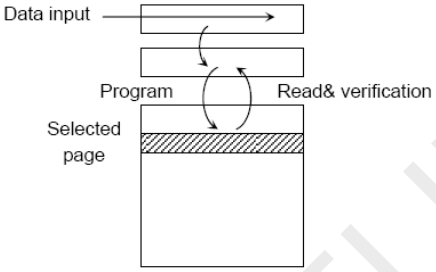
(c) $\overline{WP}$ signal

Make sure $\overline{WP}$ is held to High when a Multi Page Read operation is performed.

5.5 Single Page Program Operation

The device carries out an automatic Single Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address, and data input is shown below. (Refer to the detailed timing chart.)



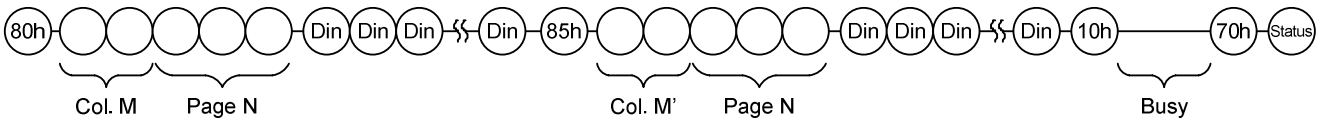


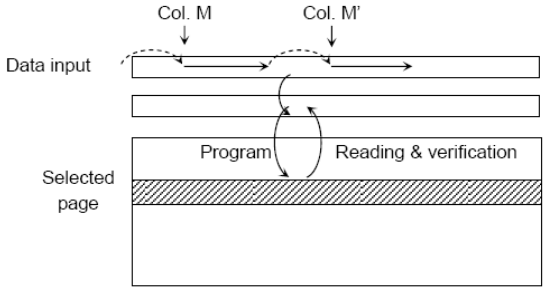
The data is transferred (programmed) from the Data Cache via the Page Buffer to the selected page on the rising edge of $\overline{WE}$ following input of the "10h" command. After programming, the programmed data is transferred back to the Page Buffer to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

5.6 Random Column Address Change in Single Page Program Operation

The column address can be changed by the 85h command during the data input sequence of the Single Page Program operation.

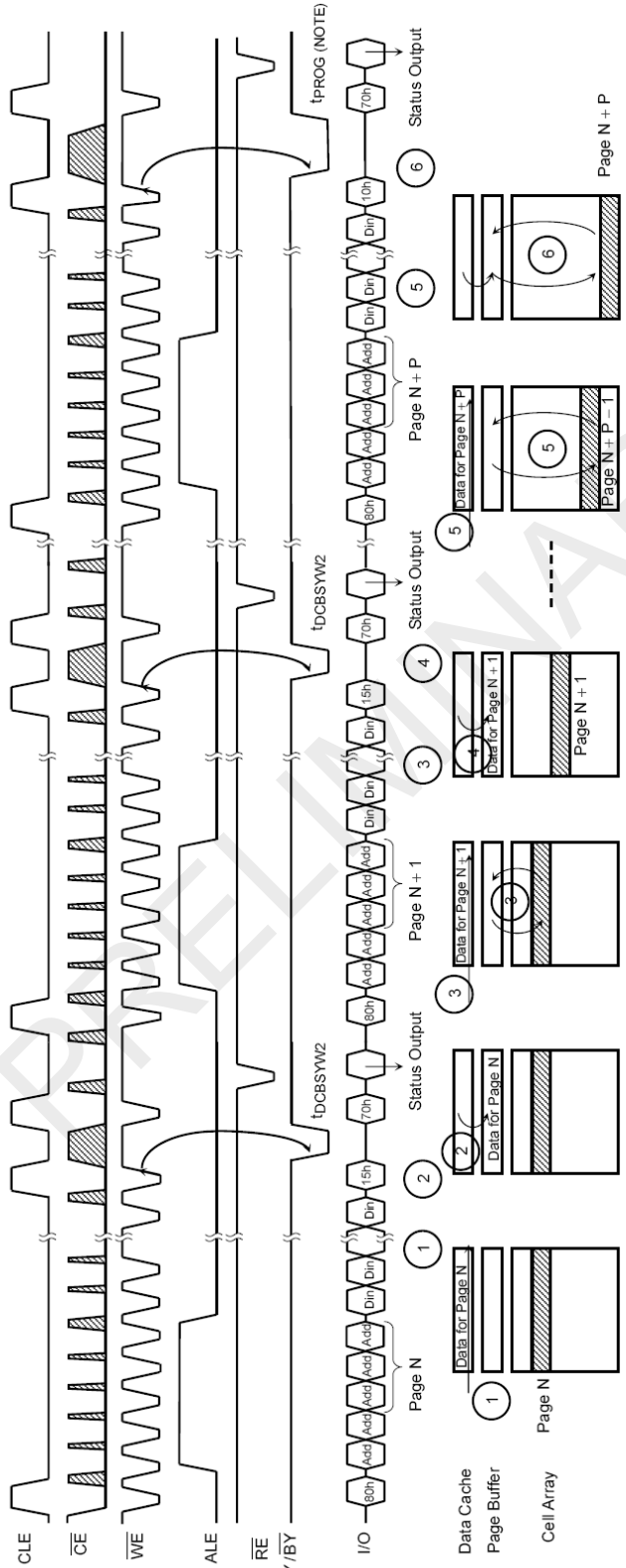
Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.





5.7 Auto Page Program with Data Cache Operation

The device has an Auto Page Program with Data Cache operation enabling the high speed program operation shown below. When the block address changes this sequenced has to be started from the beginning.



Issuing the 15h command to the device after serial data input initiates the program operation with Data Cache

1 Data for Page N is input to Data Cache.
2 Data is transferred to the Page Buffer by the 15h command. During the transfer the Ready/Busy outputs Busy State ($t_{DCBSYW2}$).
3 Data is programmed to the selected page while the data for page N + 1 is input to the Data Cache.
4 By the 15h command, the data in the Data Cache is transferred to the Page Buffer after the programming of page N is completed. The device output busy state from the 15h command until the Data Cache becomes empty. The duration of this period depends on timing between the internal programming of page N and serial data input for Page N + 1 ($t_{DCBSYW2}$).
5 Data for Page N + P is input to the Data Cache while the data of the Page N + P – 1 is being programmed.
6 The programming with Data Cache is terminated by the 10h command. When the device becomes Ready, it shows that the internal programming of the Page N + P is completed.

NOTE: Since the last page programming by the 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following;

$t_{PROG} = t_{PROG}$ for the last page + t_{PROG} of the previous page – (command input cycle + address input cycle + data input cycle time of the previous page)

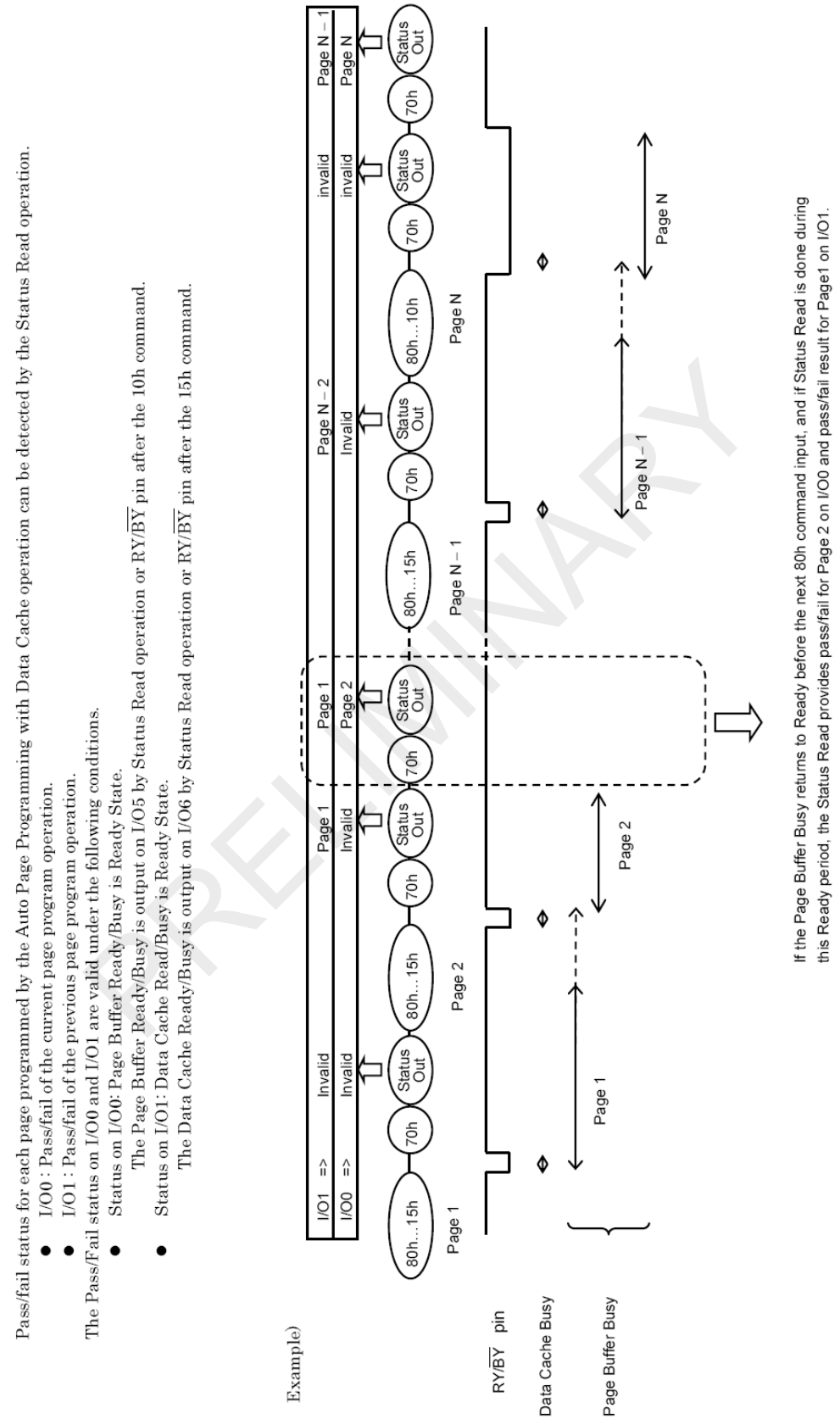
Pass/fail status for each page programmed by the Auto Page Programming with Data Cache operation can be detected by the Status Read operation.

- I/O0 : Pass/fail of the current page program operation.
- I/O1 : Pass/fail of the previous page program operation.

The Pass/Fail status on I/O0 and I/O1 are valid under the following conditions.

- Status on I/O0: Page Buffer Ready/Busy is Ready State.
  The Page Buffer Ready/Busy is output on I/O5 by Status Read operation or RY/$\overline{BY}$ pin after the 10h command.
- Status on I/O1: Data Cache Read/Busy is Ready State.
  The Data Cache Ready/Busy is output on I/O6 by Status Read operation or RY/$\overline{BY}$ pin after the 15h command.

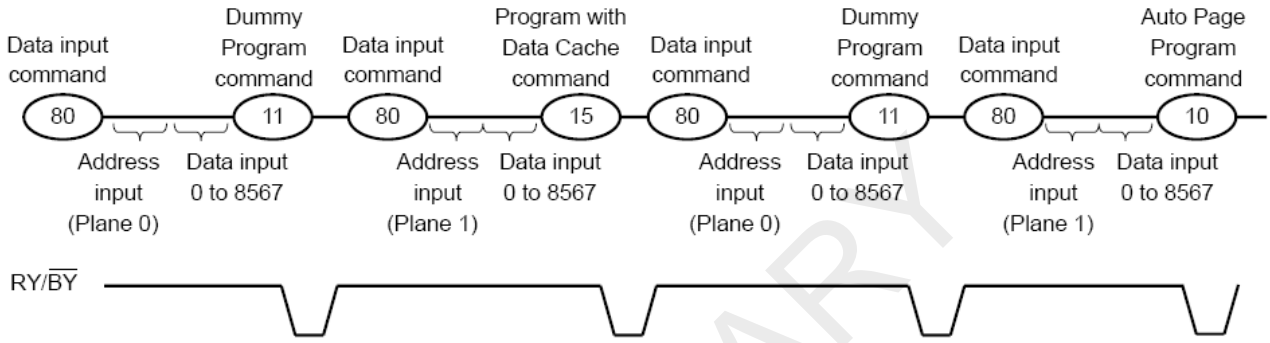
Example)



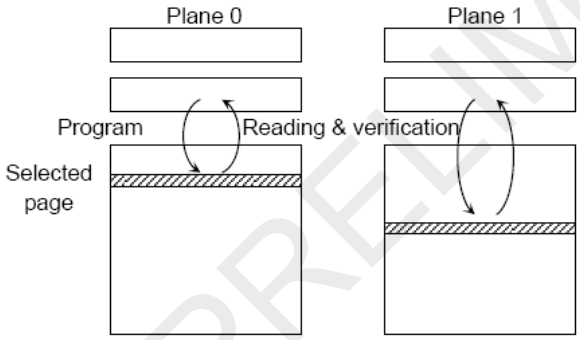
5.8 Multi Page Program with Data Cache Operation

The device has a Multi Page Program with Data Cache operation, which enables even higher speed program operation compared to Auto Page Program with Data Cache, as shown below. When the block address changes (increments), this sequence must be started from the beginning.

The sequence of command, address, and data input is shown below. (Refer to the detailed timing chart.)



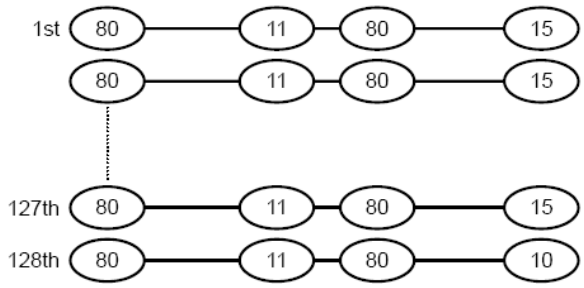
After a "15h" or "10h" Program command is input to the device, physical programing starts, as follows. For details about Single Program with Data Cache, refer to the "Single Page Program with Data Cache" section.



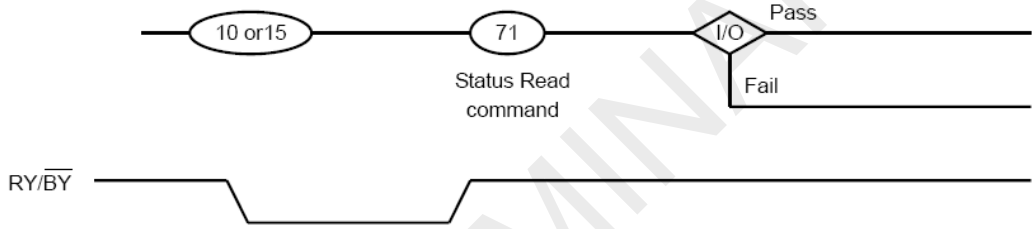
The data is transferred (programmed) from the page buffer to the selected page on the rising edge of $\overline{WE}$, following input of the "15h" or "10h" command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved, or until the maximum loop number set in the device is reached.

Starting the above operation from the first page of the selected erase blocks, and then repeating the operation a total of 128 times with the page address incrementing in the blocks, after inputting the last page of the data blocks, the "10h" command executes final programming. Make sure to terminate with an 80h-10h command sequence.

In this full sequence, the command sequence is as follows:



After the "15h" or "10h" command, the results of the above operation are shown using the "71h" Status Read command.



The 71h command Status description is provided below.

	STATUS	OUTPUT	
I/O0	Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
I/O1	Plane 0 Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
I/O2	Plane 1 Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
I/O3	Plane 0 Chip Status2 : Pass/Fail	Pass: 0	Fail: 1
I/O4	Plane 1 Chip Status2 : Pass/Fail	Pass: 0	Fail: 1
I/O5	Ready/Busy	Ready: 1	Busy: 0
I/O6	Data Cache Ready/Busy	Ready: 1	Busy: 0
I/O7	Write Protect	Protect: 0	Not Protect: 1

I/O0 describes Pass/Fail condition of Plane 0 and 1 (OR data of I/O1 and I/O2). If one of the Planes fails during a multi page program operation, it shows "Fail".

I/O1 to 4 show the Pass/Fail condition of each Plane. For details on "Chip Status1" and "Chip Status2", refer to the "Status Read" section.

Internal Addressing in Relation to the Planes

To use the Multi Page Program operation, the internal addressing should be considered in relation to the Plane.

- The device consists of 2 Planes.
- Each Plane consists of 2048 erase blocks.
- The allocation rule is as follows:
  Plane 0: Block 0, Block 2, Block 4, Block 6, ···, Block 4094
  Plane 1: Block 1, Block 3, Block 5, Block 7, ···, Block 4095
- For 32GB with 4 $\overline{CE}$ control pins, each Plane has 4096 erase blocks:
  Plane 0: Block 0, Block 2, Block 4, Block 6,···, Block 8190
  Plane 1: Block 1, Block 3, Block 5, Block 7,···, Block 8191

Address Input Restriction for Multi Page Program w/ Data Cache Operation

Restrictions when using Multi Page Program with Data Cache are as follows;

(Restriction)
Maximum one block should be selected from each Plane.
Same page address (PA0 to PA6) within each Plane must be selected.
For example;
(80) [Plane 0, Page Address 0x00000] (11) (80) [Plane 1, Page Address 0x00000] (15 or 10)
(80) [Plane 0, Page Address 0x00001] (11) (80) [Plane 1, Page Address 0x00001] (15 or 10)

(Acceptance)
There is no order limitation on the Plane for the address input. An address from either Plane can be entered first. For example, the following operation is accepted:
(80) [Plane 0] (11) (80) [Plane 1] (15 or 10)
(80) [Plane 1] (11) (80) [Plane 0] (15 or 10)

Any valid block address from each Plane can be entered. The selected block addresses from the two Planes do not need to be related.

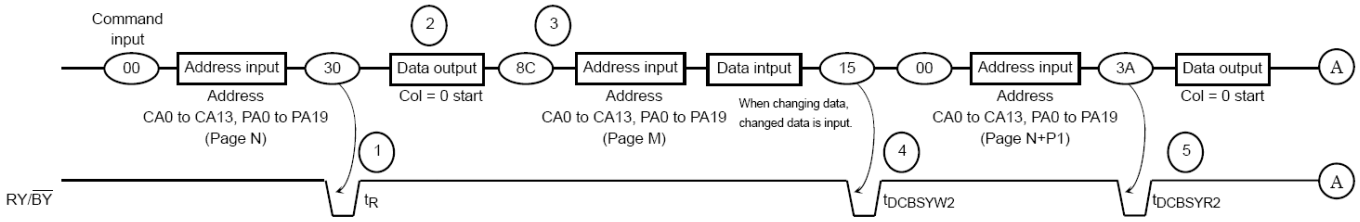
Operating Restriction During Multi Page Program w/ Data Cache Operation

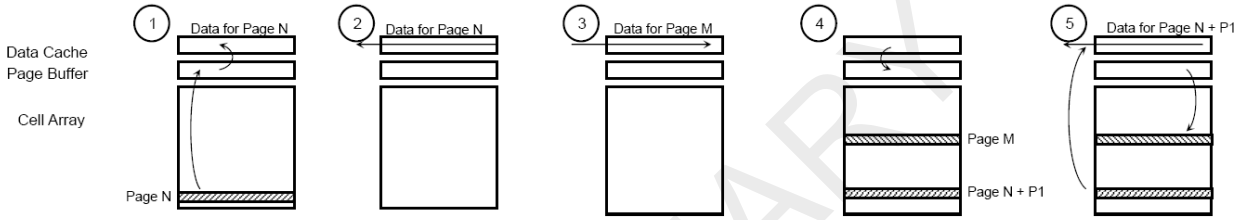
(Restriction)
The operation must be terminated with a "10h" command.
Once the operation is started, no commands other than the commands shown in the timing diagram are allowed to be input, except for a Status Read or a Reset command. If an FF reset command is input before a write operation to page B is complete, it can cause damage to data; not only to the programmed page, but also to the adjacent page A. Regarding page A and B, see the table below:

Page A	Page B	Page A	Page B
0	2	⋮	⋮
1	4	⋮	⋮
3	6	⋮	⋮
5	8	97	100
7	10	99	102
9	12	101	104
11	14	103	106
13	16	105	108
15	18	107	110
17	20	109	112
19	22	111	114
21	24	113	116
23	26	115	118
25	28	117	120
27	30	119	122
⋮	⋮	121	124
⋮	⋮	123	126
⋮	⋮	125	127

5.9 Page Copy (2)

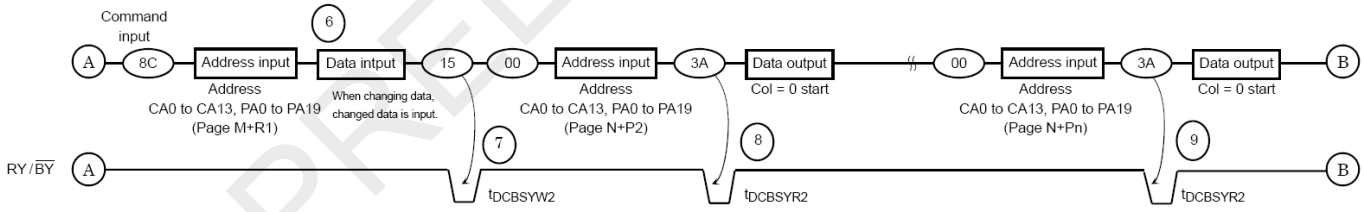
By using Page Copy (2), data in a page can be copied to another page after the data has been read out.
When the block address changes (increments) this sequenced has to be started from the beginning.

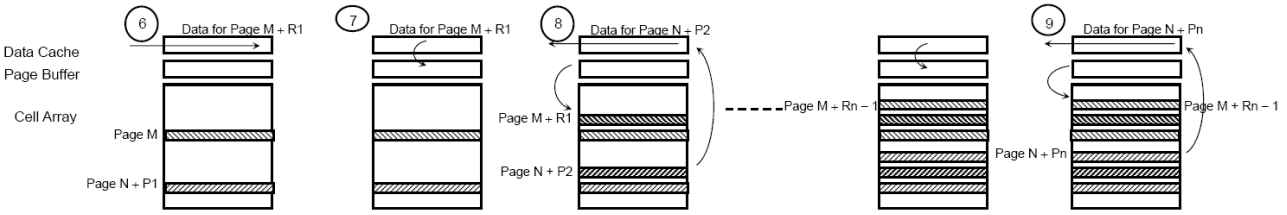




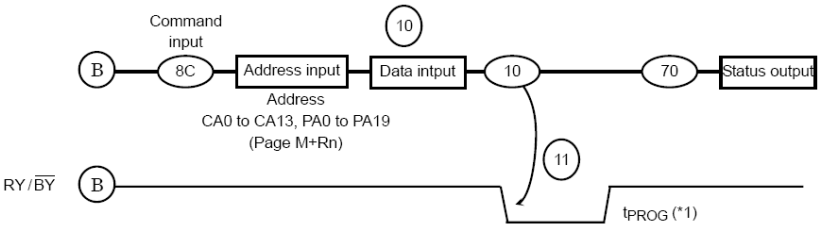
Page Copy (2) operation is as following.

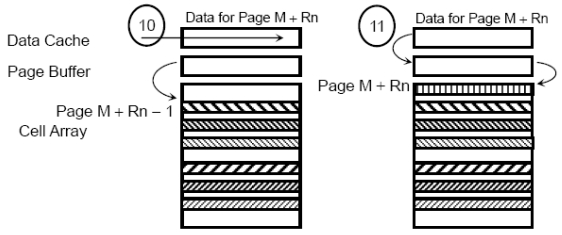
1 Data for Page N is transferred to the Data Cache.
2 Data for Page N is read out.
3 Copy Page address M is input and if the data needs to be changed, changed data is input.
4 Data Cache for Page M is transferred to the Page Buffer.
5 After the Ready state, Data for Page N + P1 is output from the Data Cache while the data of Page M is being programmed.





6 Copy Page address (M + R1) is input and if the data needs to be changed, changed data is input.
7 After programming of page M is completed, Data Cache for Page M + R1 is transferred to the Page Buffer.
8 By the 15h command, the data in the Page Buffer is programmed to Page M + R1. Data for Page N + P2 is transferred to the Data cache.
9 The data in the Page Buffer is programmed to Page M + Rn – 1. Data for Page N + Pn is transferred to the Data Cache.





10 Copy Page address (M + Rn) is input, and if the data must be changed, changed data is input.
11 By issuing the 10h command, the data in the Page Buffer is programmed to Page M + Rn.

(*1) Since the last page programming by the 10h command is initiated after the previous cache program, the t_{PROG} here is expected as follows:
t_{PROG} = t_{PROG} of the last page + tPROG of the previous page – (command input cycle + address input cycle + data output/input cycle time of the last page)

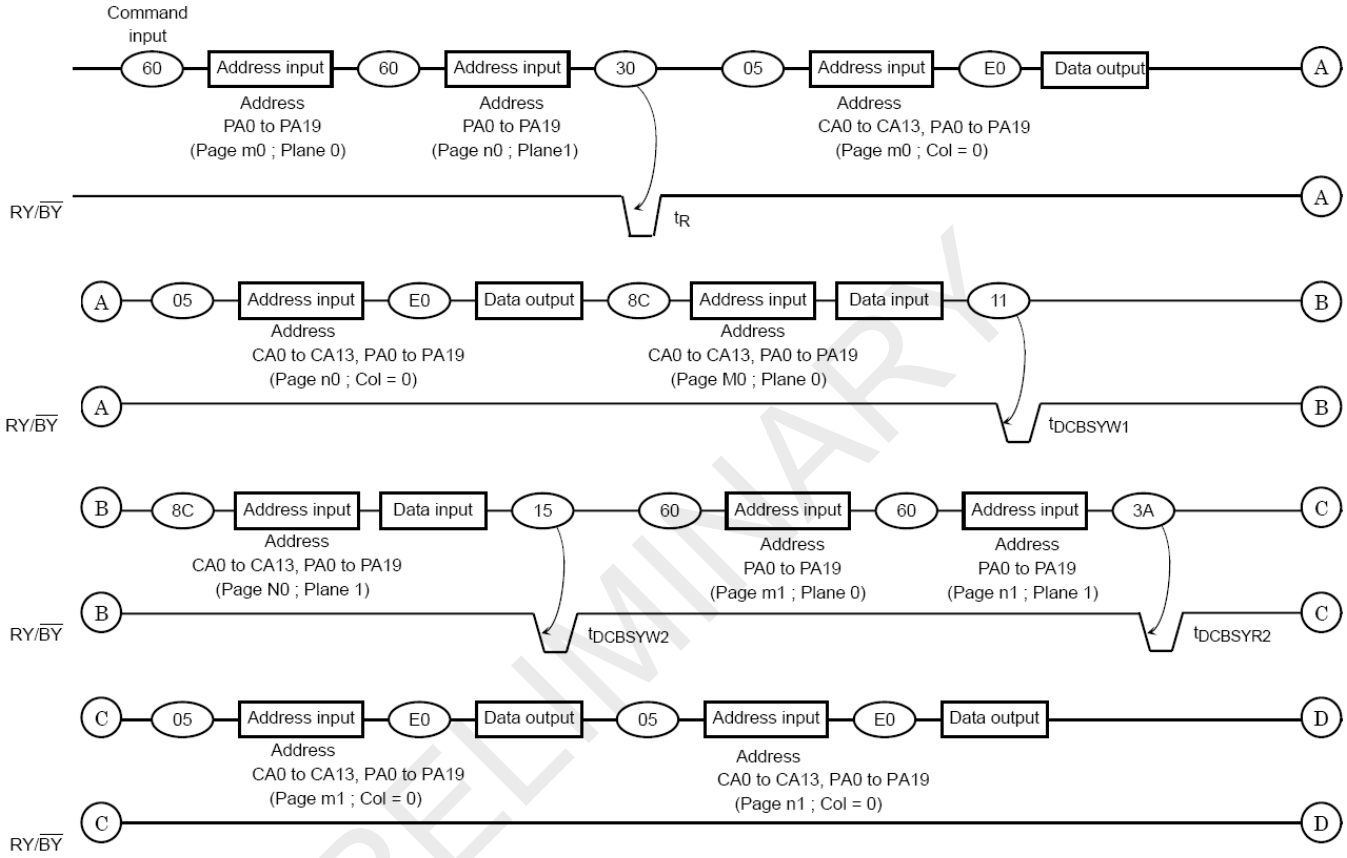
NOTE) This operation needs to be executed within each Plane.

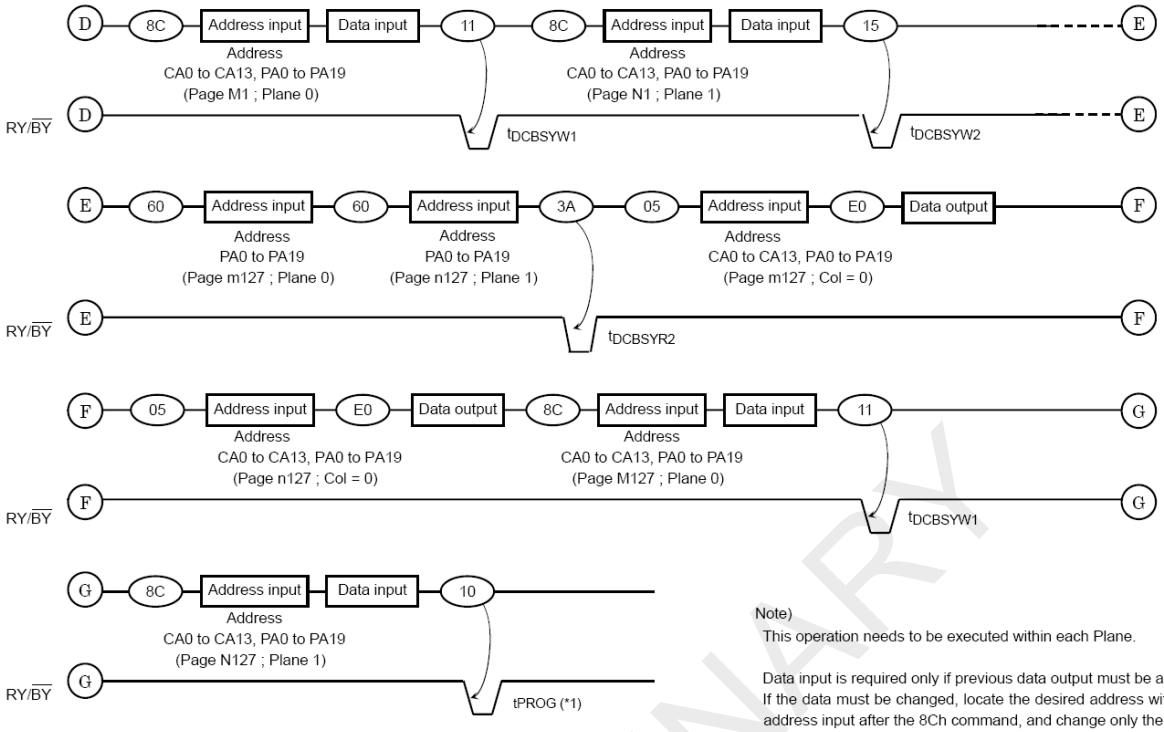
Data input is required only if previous data output must be altered.
If the data must be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that must be changed.
If the data does not have to be changed, data input cycles are not required.

Make sure $\overline{WP}$ is held to High when a Page Copy (2) operation is performed.
Also, make sure the Page Copy operation is terminated with an 8Ch-10h command sequence.

5.10 Multi Page Copy (2)

By using Multi Page Copy (2), data in two pages can be copied to another pages after the data has been read out.
When each block address changes (increments), this sequence must be started from the beginning.
Same page address (PA0 to PA6) within two Planes must be selected.





(*1) t_{PROG}: Since the last page programming by 10h command is initiated after the previous cache program, the t_{PROG*} during cache programming is given by the following equation.

$t_{PROG} = t_{PROG}$ of the last page + t_{PROG} of the previous page-A
A = (command input cycle + address input cycle + data output/input cycle time of the last page)
If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

Note)
This operation needs to be executed within each Plane.

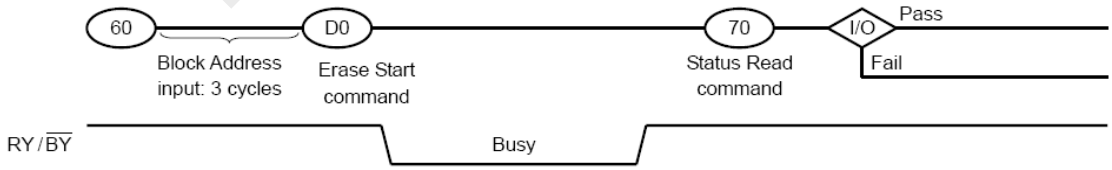
Data input is required only if previous data output must be altered.
If the data must be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that must be changed. If the data does not have to be changed, data input cycles are not required.

Make sure $\overline{WP}$ is held to High when a Multi Page Copy (2) operation is performed. Also, make sure the Multi Page Copy operation is terminated with an 8Ch-10h command sequence.

5.11 Single Block Erase

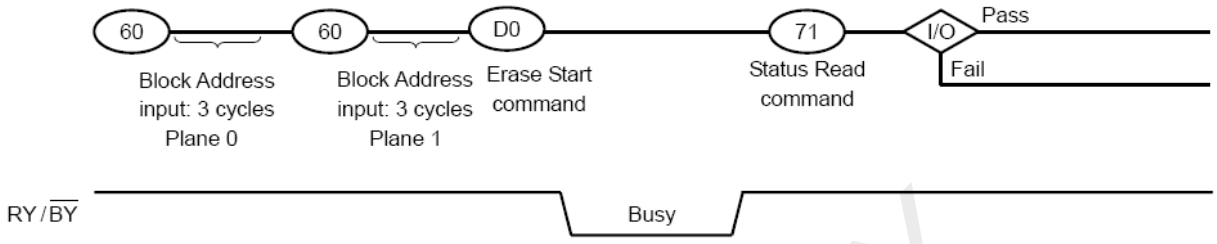
Single Block Erase

The Single Block Erase operation starts on the rising edge of $\overline{WE}$ after the "D0h" Erase Start command, which follows the "60h" Erase Setup command. This two-cycle process for Erase operations acts as an extra layer of protection against accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



5.12 Multi Block Erase

The Multi Block Erase operation starts by selecting two block addresses before a D0h command, as in the below diagram. The device automatically executes the Erase and Verify operations, and the result can be monitored by checking the status with a 71h status read command. For details on the 71h status read command, refer to the "Multi Page Program with Data Cache" section.



Internal Addressing in Relation to the Planes

When using a Multi Block Erase operation, internal addressing should be considered in relation to the Plane.

- The device consists of 2 Planes.
- Each Plane consists of 2048 erase blocks.
- The allocation rule is as follows:
  Plane 0: Block 0, Block 2, Block 4, Block 6, ···, Block 4094
  Plane 1: Block 1, Block 3, Block 5, Block 7, ···, Block 4095

- For 32GB with 4 $\overline{CE}$ control pins, each Plane has 4096 erase blocks:
  Plane 0: Block 0, Block 2, Block 4, Block 6, ···, Block 8190
  Plane 1: Block 1, Block 3, Block 5, Block 7, ···, Block 8191

Address Input Restriction for Multi Block Erase Operation

Restrictions when using Multi Block Erase are as follows:

(Restriction)
A maximum of one block should be selected from each Plane.
For example;
(60) [Plane 0] (60) [Plane 1] (D0)

(Acceptance)
There is no order limitation on the Plane for the address input. An address from either Plane can be entered first.
For example, the following operation is accepted;
(60) [Plane 1] (60) [Plane 0] (D0)

Any valid block address from each Plane can be entered. The selected block addresses from the two Planes do not need to be related.
Make sure to terminate the operation with a D0h command. If the operation must be terminated before a D0h command input, input the FFh reset command to terminate the operation.

5.13 ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

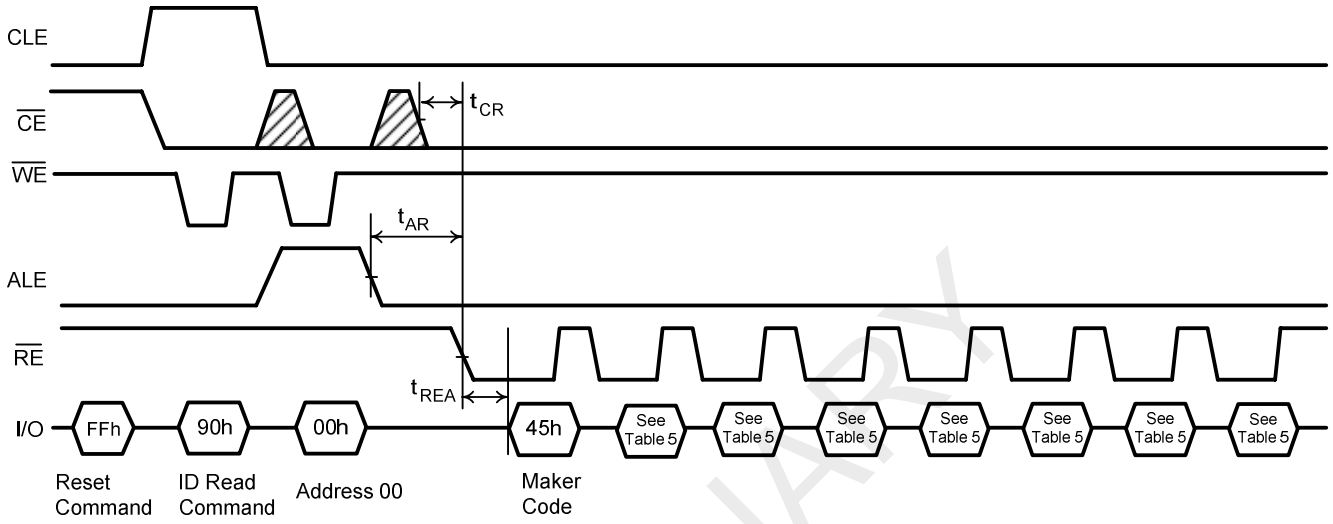


Table 5: CMD 90h ID Code

Chip	Address							
	00h	01h	02h	03h	04h	05h	06h	07h
	Maker Code	Device Code *	Multi-Die *	Block Size	Plane Info *	Technology Code	Reserved	Reserved
8GB	45h	D7h	94h	32h	76h	54h		
	SanDisk	32Gb	1-die	1MB	2-plane	43nm		
16GB	45h	D7h	94h	32h	76h	54h		
	SanDisk	32Gb	1-die	1MB	2-plane	43nm		
32GB	45h	DEh	95h	32h	7Ah	54h		
	SanDisk	64Gb	2-die	1MB	4-plane	43nm		

* Per $\overline{CE}$ pin

5.14 Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass / fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using RE after a “70h” command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

The resulting information is outlined in Table 6.

Table 6: Status Output

	Definition	Page Program Block Erase	Cache Program	Cache Read
I/O0	Chip Status1 Pass: 0 Fail: 1	Pass/Fail	Pass/Fail	Invalid
I/O1	Chip Status2 Pass: 0 Fail: 1	Invalid	Pass/Fail	Invalid
I/O2	Not Used	0	0	0
I/O3	Not Used	0	0	0
I/O4	Not Used	0	0	0
I/O5	Page Buffer Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O6	Data Cache Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O7	Write Protect Not Protected :1 Protected: 0	Write Protect	Write Protect	Write Protect

The Pass/Fail status on I/O0 and I/O1 is valid only during a Program/Erase operation when the device is in the Ready state.

Chip Status 1:

During a Single Page Program or Single Block Erase operation, this bit indicates the pass/fail result.

During a Auto Page Programming with Data Cache operation, this bit shows the pass/fail results of the current page program operation, and therefore this bit is valid only when I/O5 shows the Ready state.

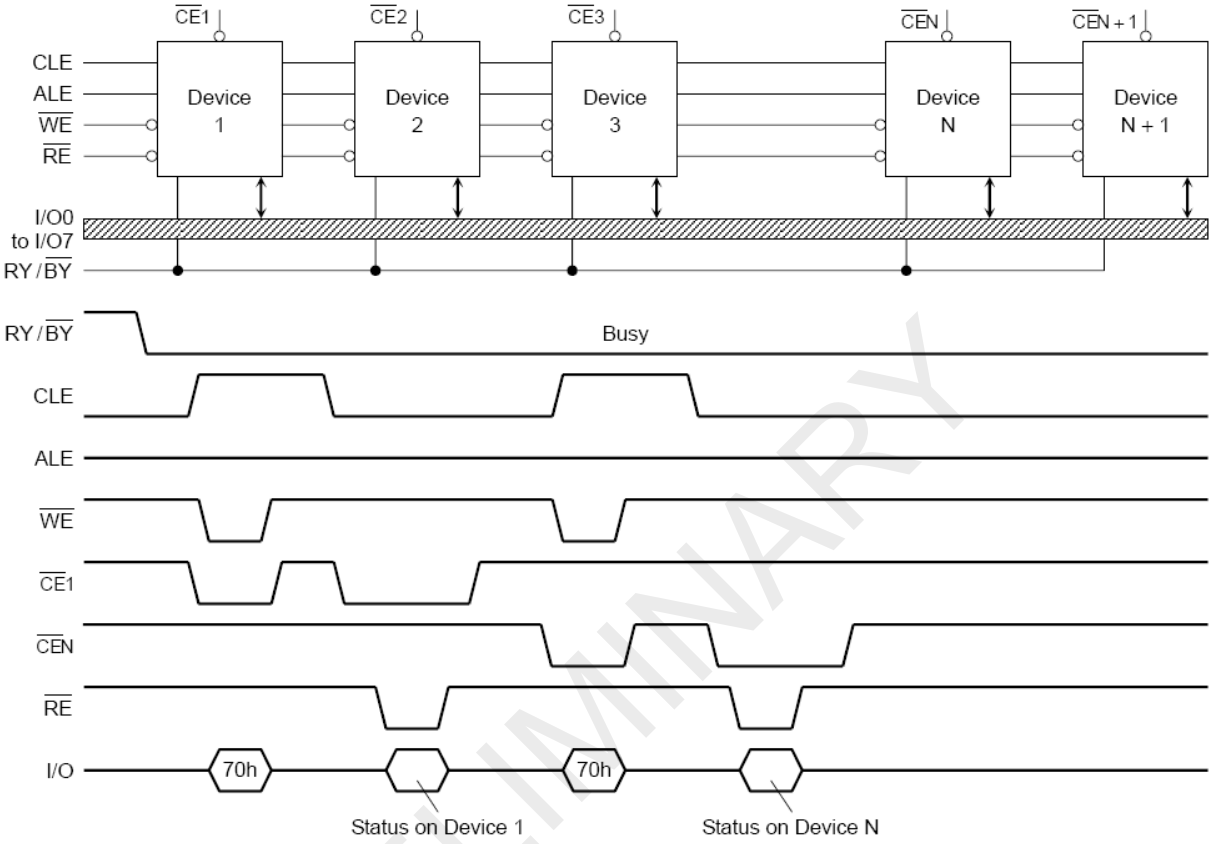
Chip Status 2:

This bit shows the pass/fail result of the previous page program operation during Auto Page Programming with Data Cache. This status is valid when I/O6 shows the Ready State.

The status output on the I/O5 is the same as that of I/O6 if the command input just before the 70h is not 15h or 31h.

Application Example

An application example with multiple devices is shown in the figure below.



System Design Note: If the RY / BY pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

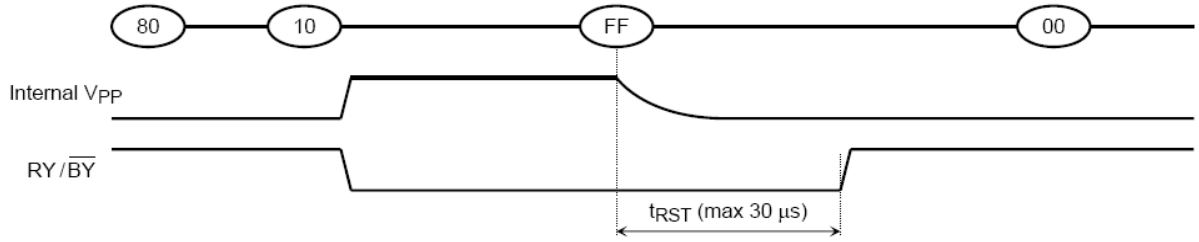
5.15 Reset

The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state.

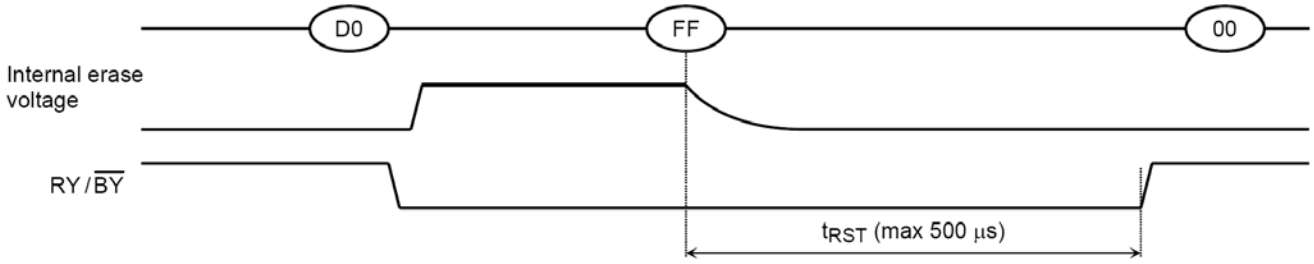
Reset during a Cache Program/Page Copy may not just stop the most recent page program but it may also stop the previous program to a page depending on when the FF reset is input.

The response to a "FFh" Reset command input during the various device operations is as follows:

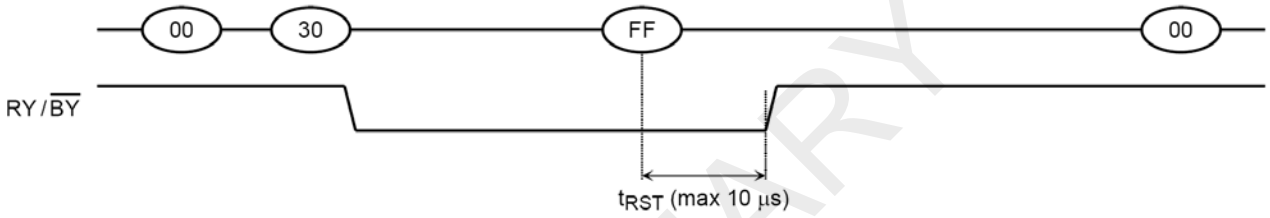
When a Reset (FFh) command is input during programming



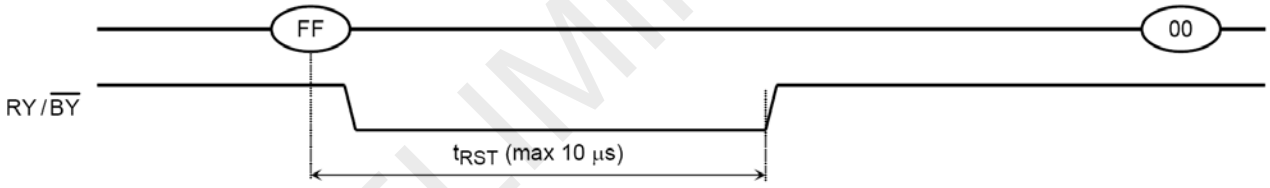
When a Reset (FFh) command is input during erasing



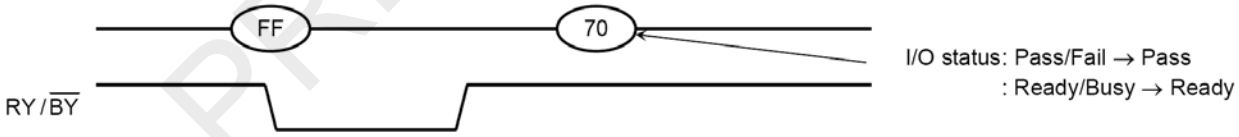
When a Reset (FFh) command is input during Read operation



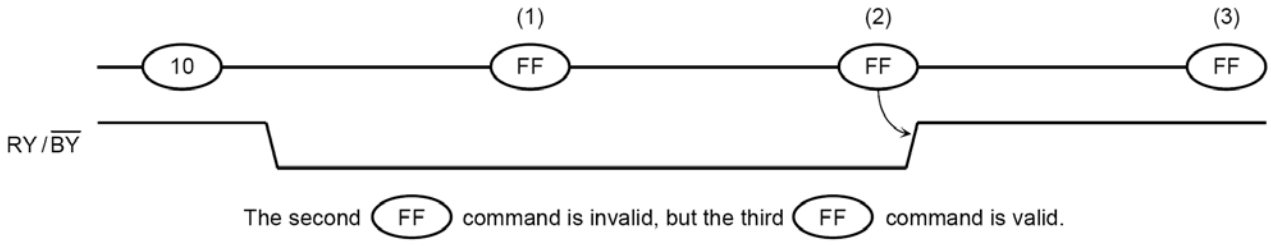
When a Reset (FFh) command is input during Ready



When a Status Read command (70h) is input after a Reset



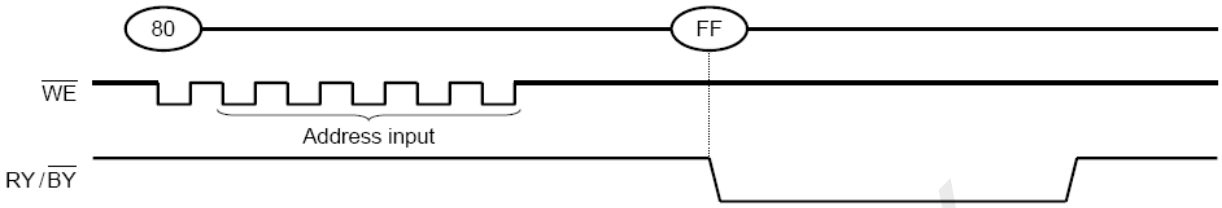
When two or more Reset commands are input in succession



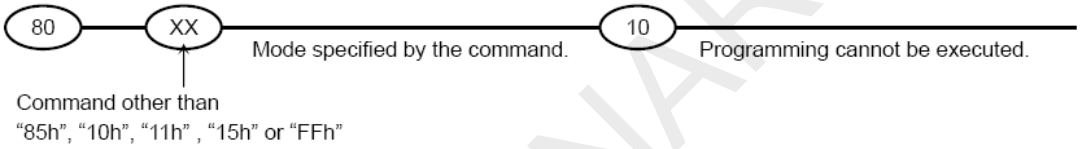
6. Application Notes and Comments

(1) Acceptable Commands After a Serial Input "80h" Command

Once the Serial Input command "80h" has been input, no command should be input other than a Column Address Change in Serial Data Input command "85h", Single Page Program command "10h", Multi Page Program command "11h", Auto Page Program with Data Cache Command "15h", or a Reset command "FFh".

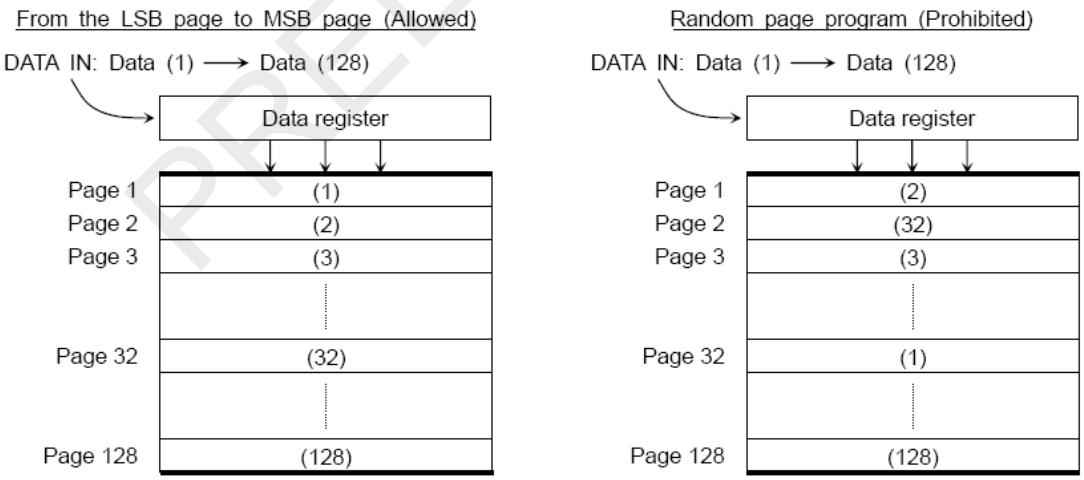


If a command other than "85h", "10h" , "11h" , "15h" or "FFh" is input, the Program operation is not performed and the device operation is set to the mode specified by the input command.

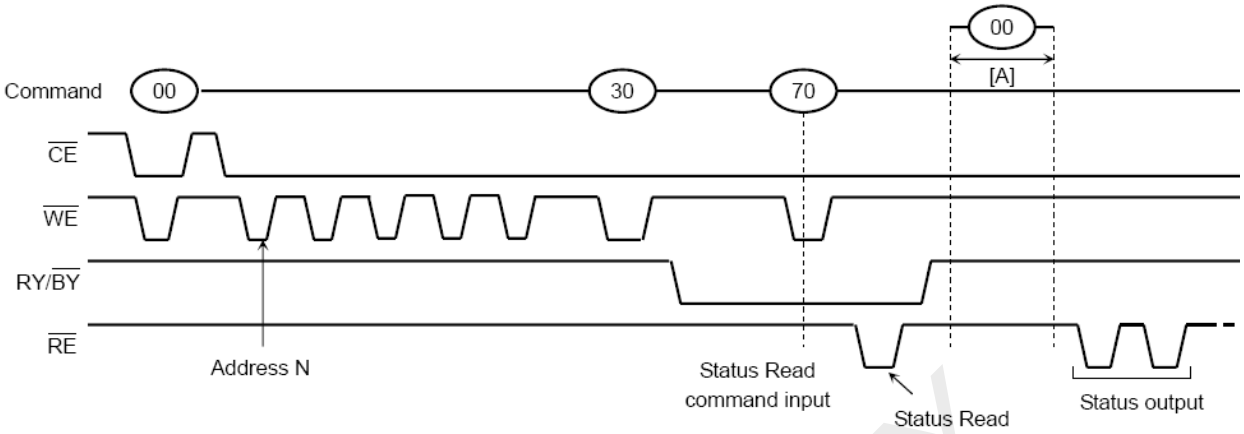


(2) Addressing for Program Operations

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

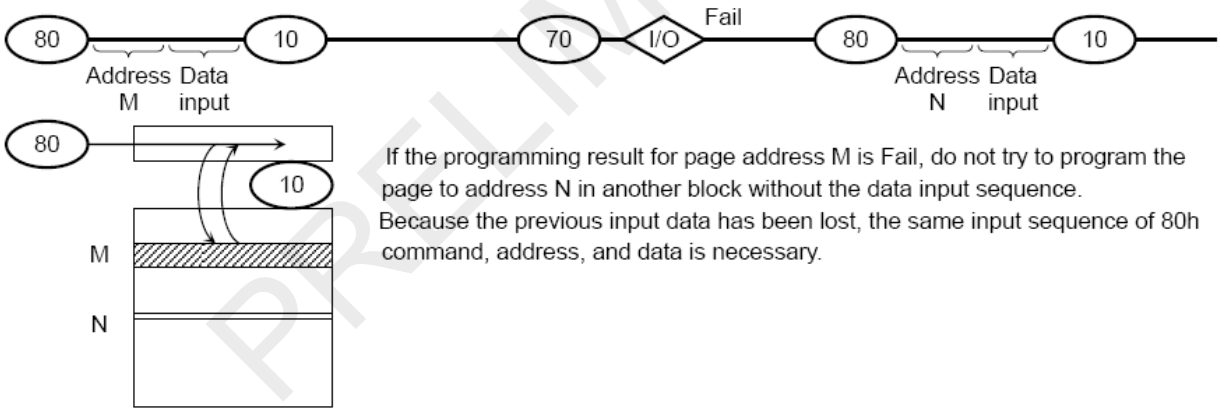


(3) Status Read During a Read Operation



The device status can be read out by inputting the Status Read command "70h" in Read mode. Once the device has been set to Status Read mode by a "70h" command, the device does not return to Read mode unless the Read command "00h" is input during [A]. If the Read command "00h" is input during [A], Status Read mode is reset, and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

(4) Page Programming Failure

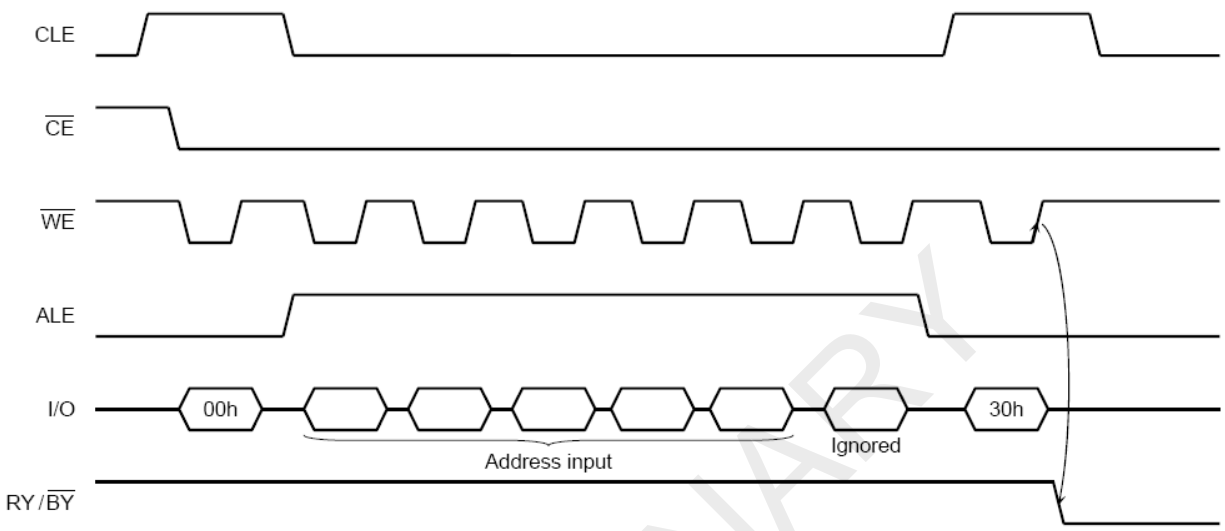


If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence. Because the previous input data has been lost, the same input sequence of 80h command, address, and data is necessary.

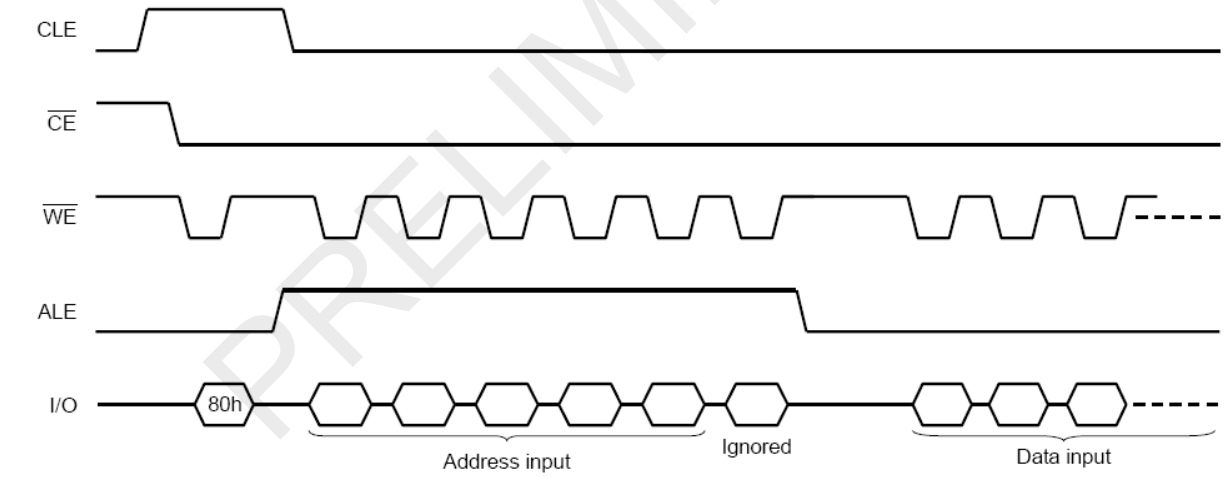
(5) When Six Address Cycles Are Input

Although the device can read in a sixth address, it is ignored inside the chip.

Read Operation

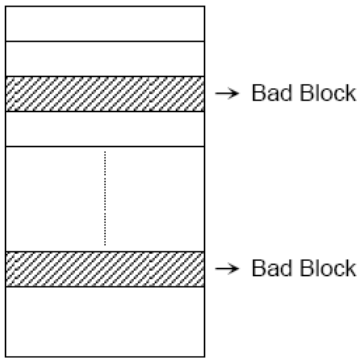


Program Operation



(6) Invalid Blocks (bad blocks)

A device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



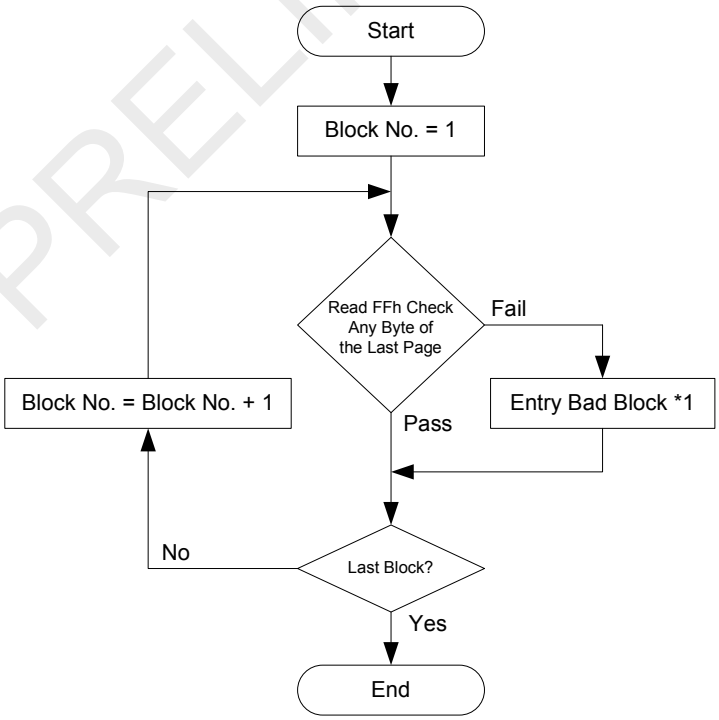
- At the time of shipment, the bad block information is marked on each bad block. Do not perform an erase operation on bad blocks; it might be impossible to recover the bad block information if the information is erased.
- Check for any bad blocks after installing the device into the system. Refer to the test flow for bad block detection. Bad blocks that are detected by the test flow must be managed as unusable blocks by the system.
- Up to 4% of all blocks available on a die might be marked as bad blocks throughout the lifetime of the device. The first logical block on each die is guaranteed to be good, and each block identified as good at shipment does not have program/erase status failure upon the first program/erase cycle. A bad block does not affect the performance of good blocks, because it is isolated from the bit lines by select gates.

The number of valid blocks over the device lifetime is as follows:

	MIN	TYP	MAX	UNITS
Valid (Good) Block Number	3933	—	4096	Block

Bad Block Test Flow

With regard to invalid blocks, the last page of the bad block is not all FFh.



*1: No erase operations are allowed on detected bad blocks.

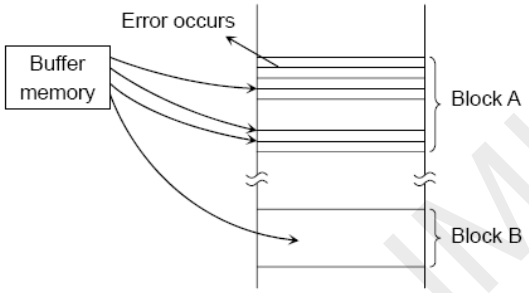
(7) Failure Phenomena for Program and Erase Operations

The device might fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Random Bit	Programming Failure "1 to 0"	ECC

- ECC: Error Correction Code. 8-bit correction per 512 Bytes is necessary.
- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(8) Power Loss

Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before a write/erase operation is complete causes loss of data and/or damage to data.

(9) Reset Command

If an FF reset command is input before completion of a write operation to page B, it might cause damage to data, not only to the programmed page, but also to the adjacent page A. For more information about page A and B, see "Operating Restriction During Multi Page Program w/ Data Cache Operation" on Page 48.

(10) Reliability Guidance

Although random bit errors might occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes might be recovered by a block erase. ECC treatment for read data is mandatory, due to the following Data Retention and Read Disturb failures.

- **Write/Erase Endurance**
  Write/Erase endurance failures might occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count increases along with the number of write/erase cycles.
- **Data Retention**
  The data in memory might change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block might become usable again.
- **Read Disturb**
  A read operation might disturb the data in memory. The data might change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge might build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block might become usable again.

All reliability-related parameters and results are measured using a random data pattern stored in memory. Results might differ if other data patterns are used.

7. Package Marking Specification

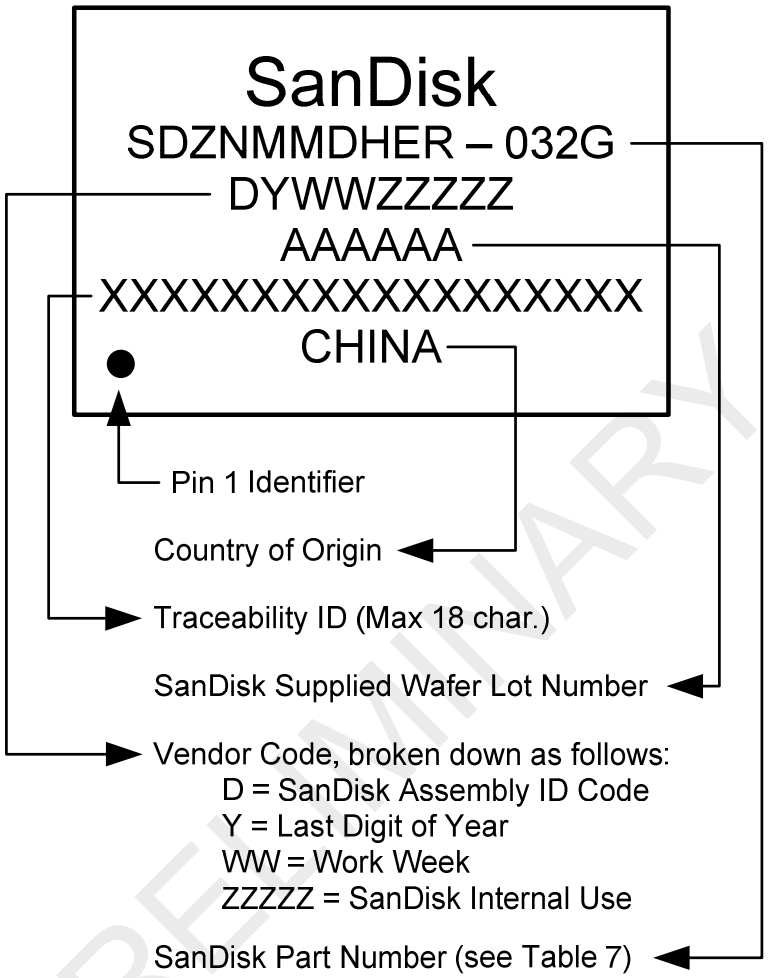


Table 7: SanDisk Internal Codes

Product Description	SanDisk Part Number
8GB	SDZNMMBHER – 008G
16GB	SDZNMMCHER – 016G
32GB	SDZNMMDHER – 032G