SHANGHAI SINO-IC
MICROELECTRONICS CO., LTD.

Apr 2015

SE3035

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

Features

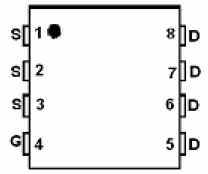
For a single MOSFET

- V_{DS} = 30V
- $R_{DS(ON)}$ = 5.5mΩ @ V_{GS}=10
- $R_{DS(ON)}$ = 9.5mΩ @ V_{GS}=4.5

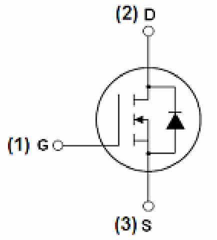
Pin configurations

See Diagram below

Marking and pin assignment



DFN 3x3 EP top view



Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current	Continuous	I_D	35	A
	Pulsed		120	
Total Power Dissipation	@TA=25℃	P_D	35	W
Operating Junction Temperature Range		T_J	-55 to 150	℃

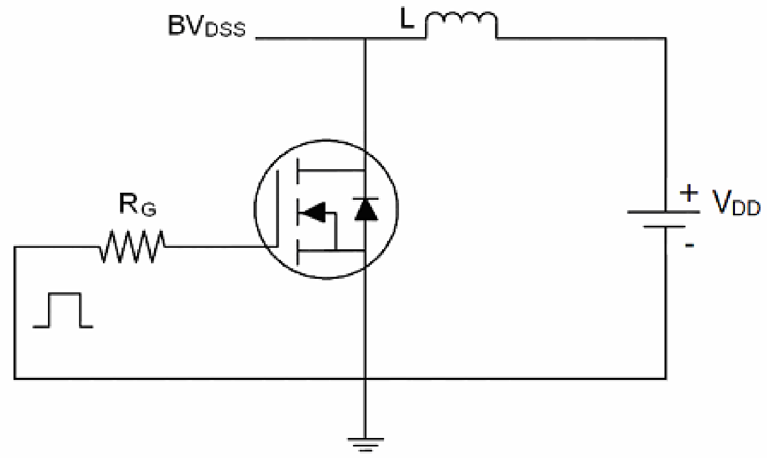
Electrical Characteristics (TJ=25℃ unless otherwise noted)						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
OFF CHARACTERISTICS (Note 2)						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0 V	30	33		V
I_{DSS}	Drain to Source Leakage Current	V_{DS}= 30V, V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	1	1.6	3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance [2]	V_{GS}=10V, I_D=12A	-	4.8	5.5	mΩ
		V_{GS}=4.5V, I_D=40A		8.2	9.5	
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		1265		pF
C_{oss}	Output Capacitance			600		pF
C_{rss}	Reverse Transfer Capacitance			130		pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge [2]	V_{GS}=10V, V_{DS}=15V, I_D=12A		19		nC
Q_{gs}	Gate Source Charge			2.7		nC
Q_{gd}	Gate Drain Charge			2.5		nC
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=15V, R_{GEN}=6Ω I_D=12A		18		ns
$t_{d(off)}$	Turn-Off Delay Time			34		ns
$t_{d(r)}$	Turn-On Rise Time			10		ns
$t_{d(f)}$	Turn-Off Fall Time			10		ns

Thermal Resistance

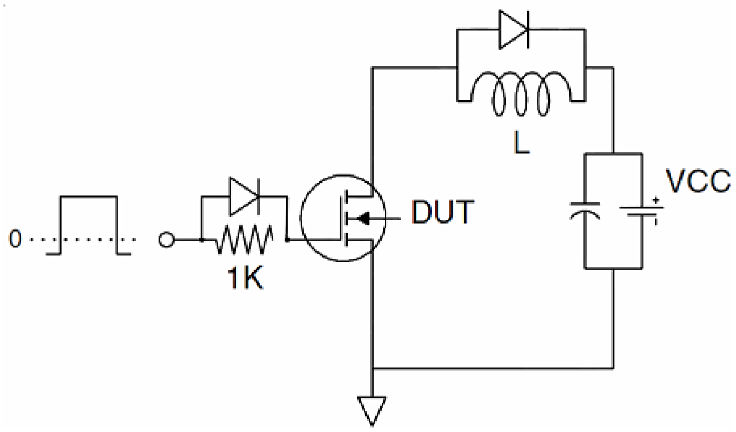
Symbol	**Parameter**	**Typ**	**Max**	**Units**
$R_{\theta JC}$	Thermal Resistance Junction to Case(t≤10s)	-	3.6	℃/W

Test Circuits and Waveform

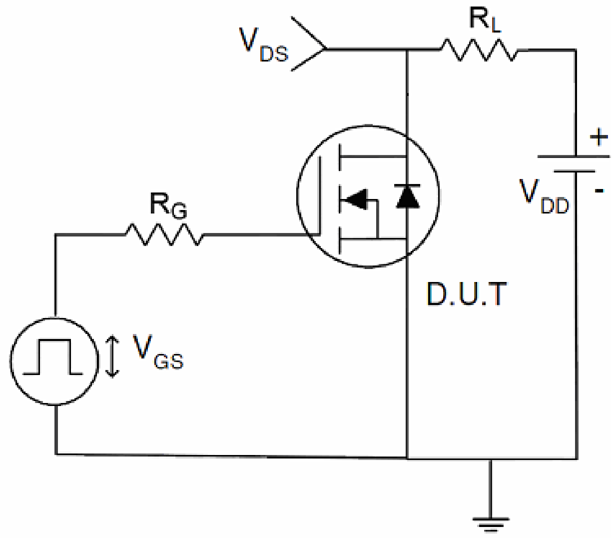
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Characteristics

Typical Electrical and Thermal Characteristics (Curves)

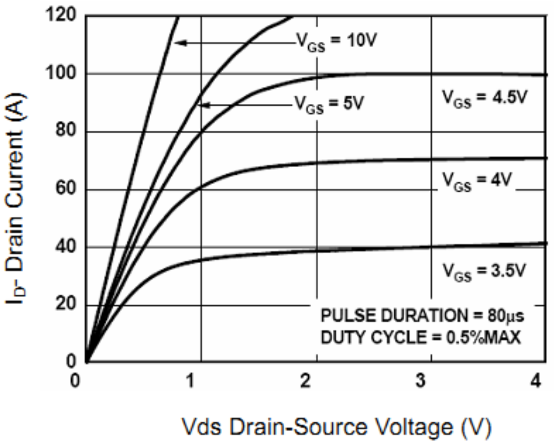


Figure 1 Output Characteristics

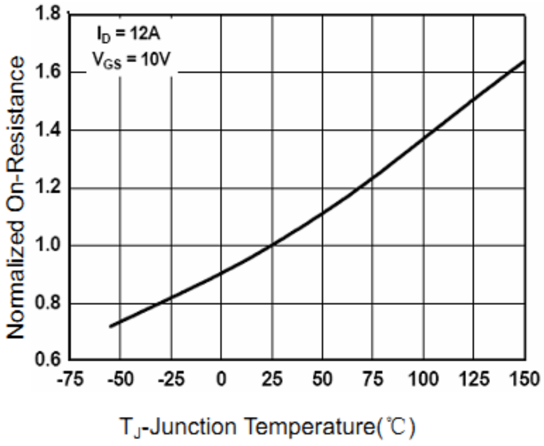


Figure 4 Rdson-Junction Temperature

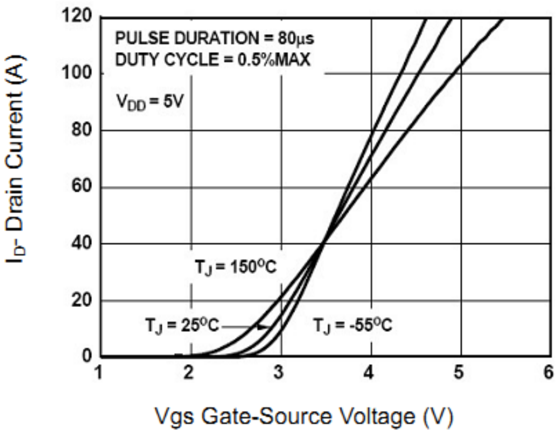


Figure 2 Transfer Characteristics

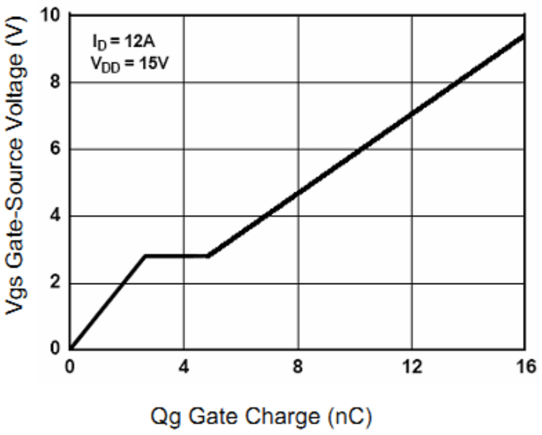


Figure 5 Gate Charge

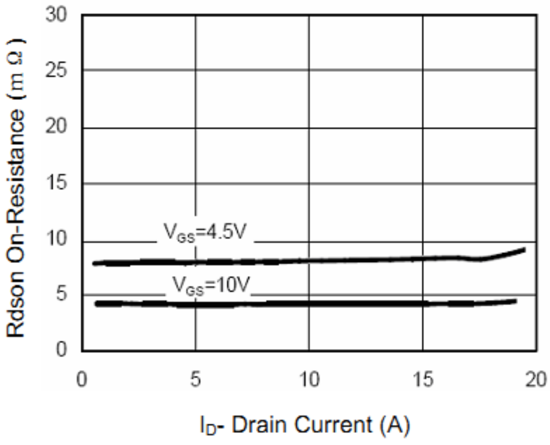


Figure 3 Rdson- Drain Current

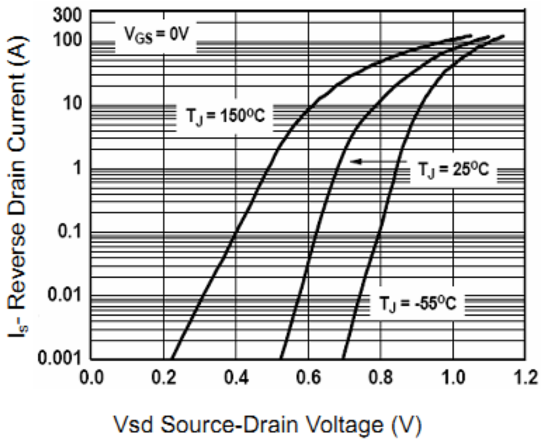


Figure 6 Source- Drain Diode Forward

Typical Characteristics

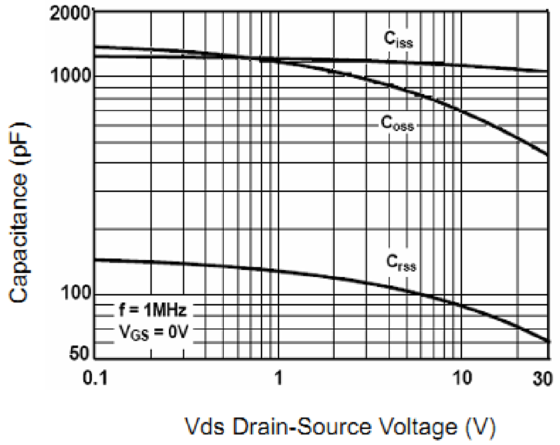


Figure 7 Capacitance vs Vds

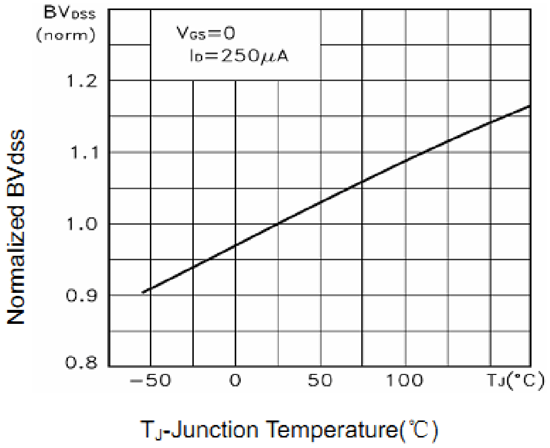


Figure 9 BV_{DSS} vs Junction Temperature

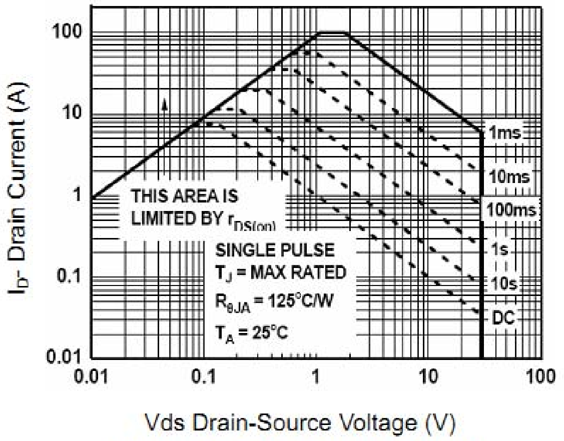


Figure 8 Safe Operation Area

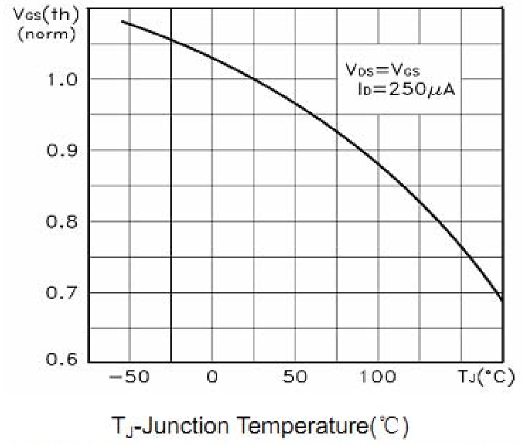


Figure 10 $V_{GS(th)}$ vs Junction Temperature

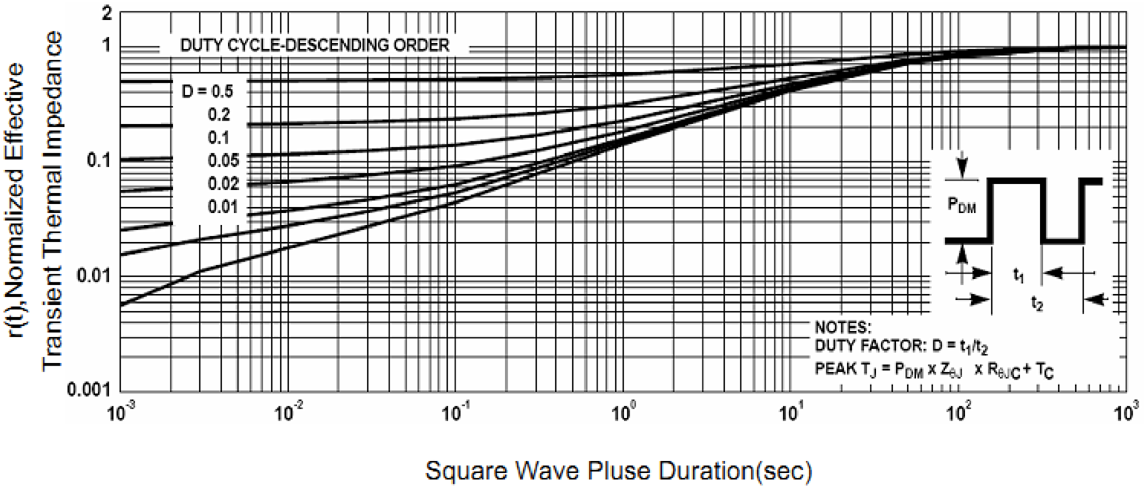
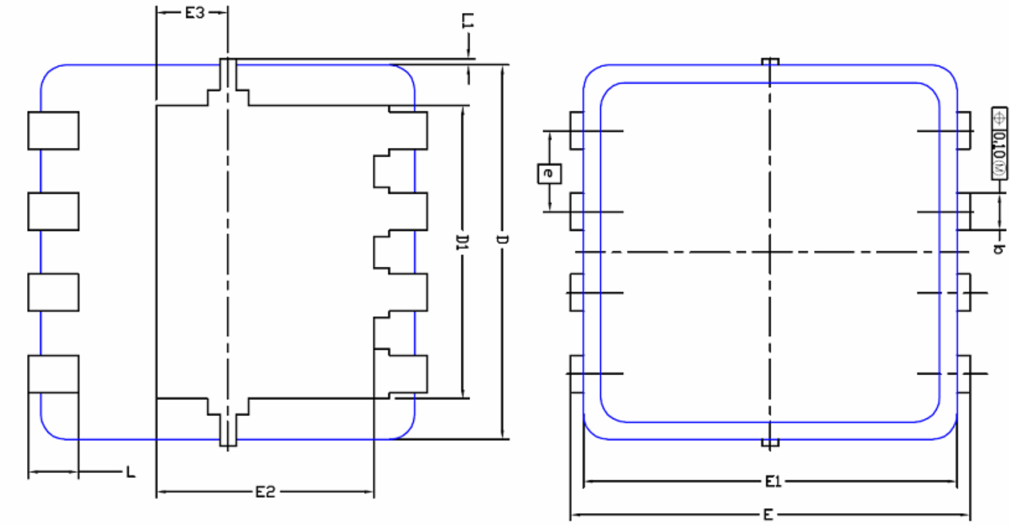
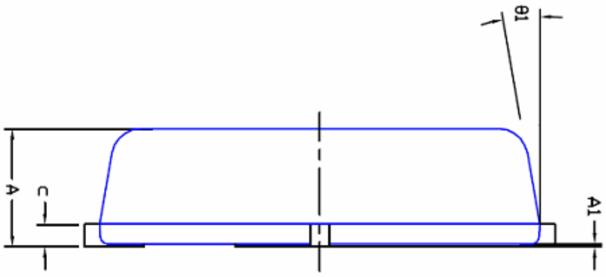


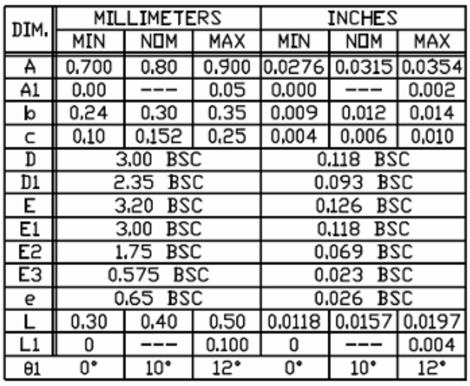
Figure 11 Normalized Maximum Transient Thermal Impedance

Package Outline Dimension

DFN3X3 EP







DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°

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