SE401 USB Video Image Controller

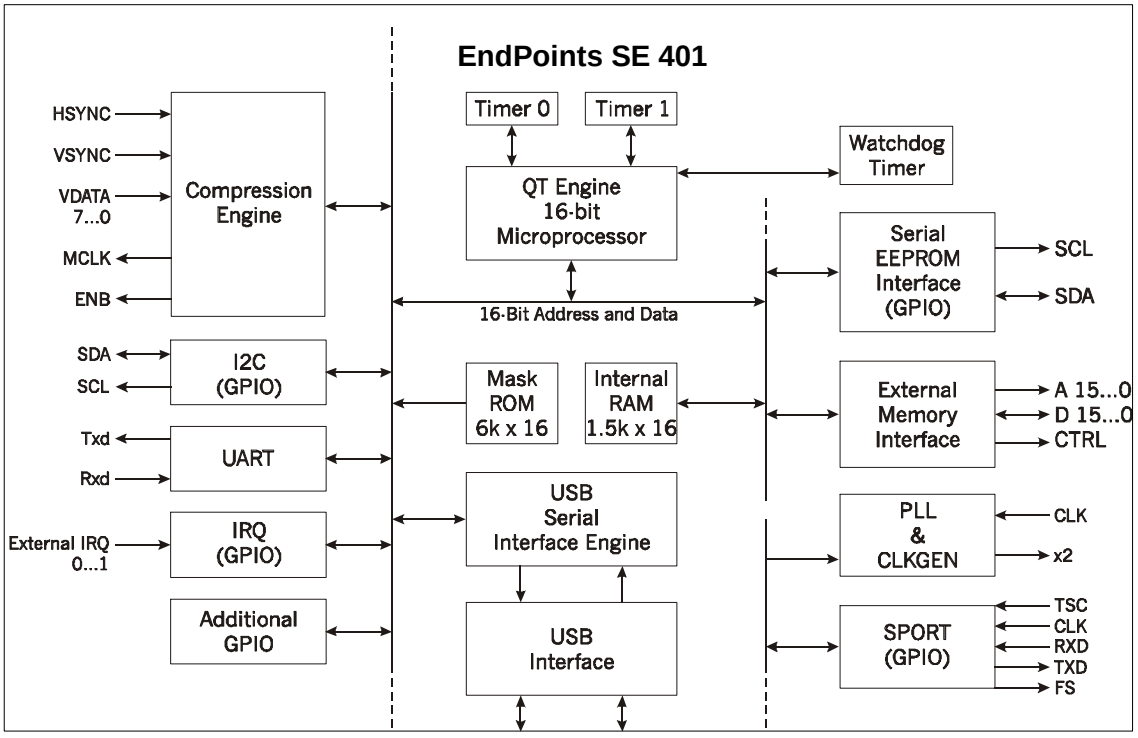
The SE401 USB Video Imager Controller is designed to form the core of a low-cost USB video camera. It is a single chip solution to control the image sensor and move the image data to the Universal Serial Bus. The only additional major components required are the CMOS image sensor and external DRAM to provide working storage for the compression engine. With the addition of an audio codec, the SE401 can also support sound, enabling a variety of audio and video applications.

The SE401 consists of a central 16-bit processor, an EndPoints-proprietary compression engine, masked ROM, a RAM buffer, a clock generator, and a flexible, extensible series of interfaces. The block diagram shows one example of the SE401 and its interfaces. Other variations can be implemented using external expansion ROM and the SE401's General Purpose Input/Output (GPIO) facilities.

Features

- **Video Imager Interface**
- **Video Compression Engine**
- **16-bit Processor**
- **USB Interface with 4 Endpoints**
- **SPORT Audio codec interface**
- **Internal Clock Generation (requires only low-cost internal crystal)**
- **1.5K X 16 Internal RAM**
- **6K X 16 Internal ROM BIOS**
- **External Memory Interface**
- **Serial EEPROM Interface**
- **Built-in UART**
- **MS Windows 95, 98 and 2000 drivers available**

Block Diagram



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Video Imager Interface	Interfaces directly with Hyundai CIF, VGA and SVGA CMOS sensors. Other sensors can be supported with the SE401's flexible GPIO architecture.
Video Compression Engine	Includes a proprietary image compression engine with variable compression rates. For maximum performance the compression engine supports DMA to the Frame Buffer and on to the USB Serial Interface Engine.
16-bit Processor	The SE401 USB Video Imager Controller has a built-in 16-bit EndPoints QT processor with its basic operating firmware in internal 6K X 16 masked ROM. The QT processor operates with a specialized instruction set designed for highly efficient coding of processing algorithms and USB transaction processing. Functionality of the QT Processor can be extended using external EEPROM
USB Subsystem	The SE401 USB Video Imager Controller contains a complete USB subsystem with a Serial Interface Engine (SIE) and built-in transceiver operating at full 12Mbits/sec data rate. The USB Subsystem meets the Universal Serial Bus (USB) specification v1.1. In addition to the default control endpoint, the SE401 supports three additional endpoints, which may be configured as Isochronous or Bulk/Interrupt.
PLL Clock Generator	An inexpensive 12 MHz external crystal may be used with the SE401 USB Video Imager Controller. The controller incorporates PLL circuitry to generate the internal 48MHz clock requirements of the device. Alternatively, an external 12 MHz clock signal may be used instead of the crystal.
Internal Ram Buffer	The SE401 USB Video Imager Controller contains 1.5K X 16 of internal buffer memory. The memory is used for expansion code and data, such as USB packets. It is accessed by both the processor and the Serial Interface Engine (SIE). USB control packets are automatically routed to the buffer memory.
6K ROM BIOS	Internal 6K X 16 Masked ROM contains a BIOS (Basic Input/Output System) with functions to manage Power-On initialization, USB Transactions, USB Enumeration, USB Power Management, Expansion EEPROM Scan support, Memory Management etc.
UART Interface	Supports 1200 to 115.2K baud at TTL-levels.
General Purpose I/O	Up to 32 general purpose I/O signals are available. GPIO may be configured for special purpose functions such as the SPORT Synchronous Serial Interface for audio codec etc.
Serial EEPROM Support	The SE401 USB Video Imager Controller serial EEPROM interface is used to provide access to external EEPROMs. The interface is implemented using general-purpose I/O signals and can support a variety of serial EEPROM formats.
External Memory Interface	A multiplexed address port and 16-bit data port has been provided to interface to an external SRAM, DRAM or EEPROM with programmable wait states. The port provides RAS, CAS, RD and WR control signals for data access and refresh cycles to the DRAM.

Development Tools

C Compiler, Assembler and debugging tools are available to qualified customers.

About EndPoints

EndPoints is a semiconductor company specializing in the digital imaging, networking and connectivity markets.

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