

DATA SHEET

SE5516A: Dual-Band 802.11a/b/g/n/ac WLAN Front-End Module

Applications

- 802.11a/b/g/n/ac WLANs
- Computing, networking

Features

- All RF ports matched to 50 Ω
- Integrated 2.4 GHz PA, 5 GHz PA, transmit filter, transmit/receive switches, and diplexers
- Integrated power detector for each transmit chain
- Power:
 - +21 dBm, 802.11b, 11 Mbps, ACPR = +35 dBc
 - +18 dBm @ 3.0% EVM, 802.11n, 64 QAM, 2G
 - +16 dBm @ 3.0% EVM, 802.11n, 64 QAM, 5G
 - +16 dBm @ 1.8% EVM, 802.11ac, 256 QAM, 2G
 - +13 dBm @ 1.8% EVM, 802.11ac, 256 QAM, 5G
 - Single supply voltage: 3.3 V \pm 10%
- Small LGA (24-pin, 4 x 4 mm) package (MSL3, 240 $^{\circ}$ C per JEDEC J-STD-020)



Skyworks Pb-free products are compliant with all applicable legislation. For additional information, refer to *Skyworks Definition of Lead (Pb)-Free*, document number SQ04-0073.

Description

The SE5516A is a complete 802.11a/b/g/n/ac WLAN RF Front-End Module (FEM) that provides all the functionality of the Power Amplifiers (PAs), filtering, power detector, transmit/receive (T/R) switch, diplexers, and associated matching.

The device provides a complete 2.4 GHz and 5.0 GHz WLAN RF solution from the output of the transceiver to the antenna in an ultra-compact form factor. The SE5516A delivers < 2% EVM at rated AC power, which meets the stringent linearity conditions of the 802.11ac standard.

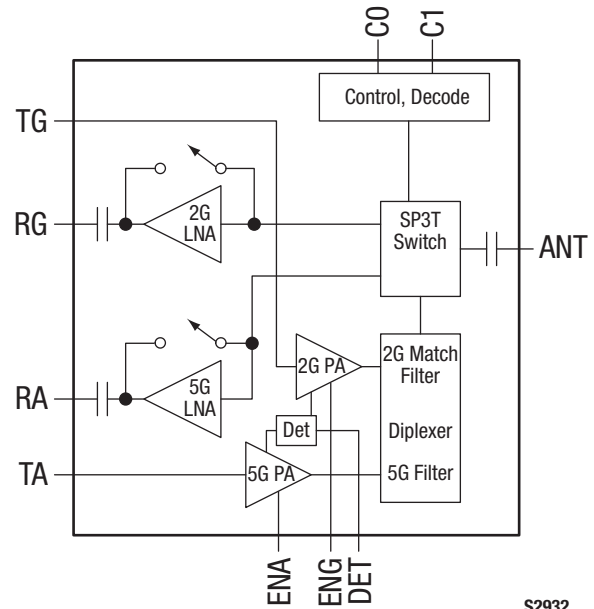


Figure 1. SE5516A Block Diagram

All RF ports are matched to 50 Ω to simplify the PCB layout and the interface to the transceiver. The device also includes a transmitter power detector with 20 dB of dynamic range for each transmit chain. Each PA has a separate digital enable control for transmitter on/off control. The power ramp rise/fall time is < 0.4 μ s.

The SE5516A also provides a notch filter from 3.260 to 3.267 GHz and 3.28 to 3.89 GHz before the input of each 2.4 GHz and 5.0 GHz PA, respectively.

The SE5516A is manufactured in a compact, 4 x 4 mm, 24-pin Land Grid Array (LGA) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

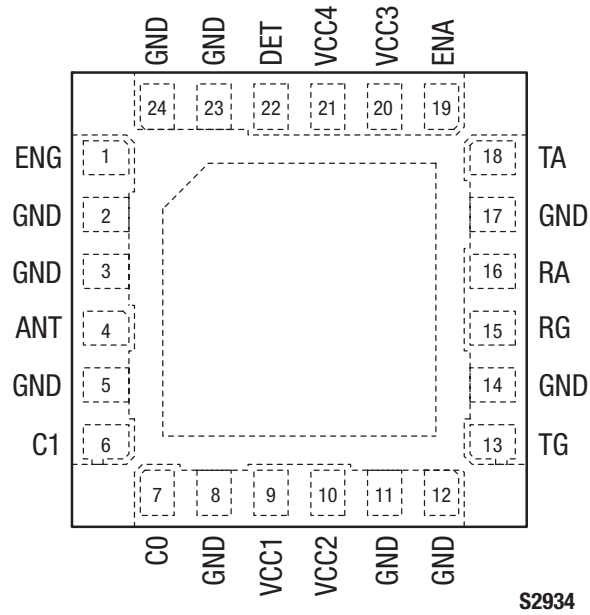


Figure 2. SE5516A Pinout – 24-Pin LGA (Top View)

Table 1. SE5516A Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	ENG	2.4 GHz PA enable	13	TG	2.0 GHz transmit RF input
2	GND	Ground	14	GND	Ground
3	GND	Ground	15	RG	2.0 GHz receive RF output
4	ANT	Antenna	16	RA	5.0 GHz receive RF output
5	GND	Ground	17	GND	Ground
6	C1	Switch control logic 1	18	TA	5.0 GHz transmit RF input
7	C0	Switch control logic 0	19	ENA	5.0 GHz PA enable
8	GND	Ground	20	VCC3	Supply voltage
9	VCC1	Supply voltage	21	VCC4	Supply voltage
10	VCC2	Supply voltage	22	DET	2.0/5.0 GHz power detector output
11	GND	Ground	23	GND	Ground
12	GND	Ground	24	GND	Ground

Table 2. SE5516A Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V _{CC}	-0.3	+3.6	V
PA enable voltage (pins ENA and ENG)		-0.3	+3.6	V
Maximum input power to TA and TG pins with ANT terminated in 6:1 load or better: @ +25°C @ -40°C	P _{IN}		+12 +5	dBm dBm
Operating temperature	T _A	-40	+85	°C
Storage temperature	T _{STG}	-40	+150	°C
Switch logic control	C0, C1	0	3.6	V
LNA power (receive mode)	P _{RX}		-3	dBm
Electrostatic discharge: ANT pin, Human Body Model (HBM), Class 1C All other pins, HBM, Class 1A	ESD		1000 250	V V

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 3. SE5516A Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	V _{CC}	3.0	3.3	3.6	V
Operating temperature	T _A	-40	+25	+85	°C
Junction temperature	T _J			+150	°C

Electrical and Mechanical Specifications

The absolute maximum ratings of the SE5516A are provided in Table 2. The recommended operating conditions are specified in Table 3 and electrical specifications are provided in Tables 4 through 12.

Typical performance characteristics of the SE5516A are illustrated in Figures 3 and 4.

Table 4. SE5516A Electrical Specifications: DC Characteristics (Note 1)
(Vcc = 3.3 V, Ta = +25 °C, All Unused Ports Terminated with 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Total 802.11a transmit supply current	Icc_A	No RF		175	210	mA
	Icc_A	P _{OUT} = +16 dBm, 54 Mbps, OFDM signal, 64 QAM		230	255	mA
Total 802.11g transmit supply current	Icc_G	No RF		135	165	mA
	Icc_G	P _{OUT} = +18 dBm, 54 Mbps, OFDM signal, 64 QAM		175	195	mA
Total 802.11b transmit supply current	Icc_B	P _{OUT} = +21 dBm, 11 Mbps, CCK signal, BT = 0.45		200	220	mA
Total 802.11ac transmit supply current, 2G	Icc_Ac2G	P _{OUT} = +16 dBm, 256 QAM, MCS9, 40 MHz		155	175	mA
Total 802.11ac transmit supply current, 5G	Icc_Ac5G	P _{OUT} = +13 dBm, 256 QAM, MCS9, 80 MHz		190	215	mA
Total receive supply current, 2G	Icc_rx2	ENG = ENA = 0 V, LNA on, switch condition 1			12	mA
Total receive supply current, 5G	Icc_rx5	ENG = ENA = 0 V, LNA on, switch condition 4			12	mA
Total supply current	Icc_OFF	No RF, ENG = ENA = 0 V, switch condition 3 or 6			50	μA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 5. SE5516A Electrical Specifications: Logic Characteristics (Note 1)
(Vcc = 3.3 V, Ta = +25 °C, All Unused Ports Terminated with 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Logic high voltage for ENG and ENA (module on)	V _{ENH}		1.8		V _{CC}	V
Logic low voltage for ENG and ENA (module off)	V _{ENL}		0		0.5	V
Input current logic high voltage (ENG and ENA)	I _{ENH}			350	400	μA
Input current logic low voltage (ENG and ENA)	I _{ENL}			0.2		μA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 6. SE5516A Electrical Specifications: Switch Characteristics (Note 1)
(V_{CC} = V_{EN} = 3.3 V, T_A = +25 °C, All Unused Ports Terminated with 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Control voltage (on state)	V _{CTL_ON}		3.0		3.6	V
Control voltage (off state)	V _{CTL_OFF}		0		0.2	V
Low loss switch control voltage	SW _{ON}	High state = V _{CTL_ON} – V _{CTL_OFF}	2.8		V _{CC}	V
High loss switch control voltage	SW _{OFF}	Low state = V _{CTL_OFF} – V _{CTL_OFF}	0		0.3	V
Switch control bias current RF applied No RF	I _{CTL_ON}	C0 and C1 pins driven high			100 30	μA μA
Control input capacitance	C _{CTL}				100	pF

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 7. SE5516A Electrical Specifications: 2.4 GHz Transmit Characteristics (1 of 2) (Note 1)
(V_{CC} = V_{ENG} = C0 = 3.3 V, V_{ENA} = C1 = 0 V, T_A = +25 °C, All Unused Ports Terminated with 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f		2400		2500	MHz
Output power, 802.11g	P _{OUT_802.11G}	54 Mbps OFDM signal, 64 QAM, DEVM = 3%, input signal EVM < 1%, 802.11g mask compliant		+18		dBm
Output power, 802.11n	P _{OUT_802.11N}	OFDM signal, MCS7, HT40, DEVM = 3%, 802.11n mask compliant, ±11 MHz offset, RBW = 100 kHz, VBW = 30 kHz DEVM = 2.5%	+18	+17		dBm dBm
Output power, 802.11ac	P _{OUT_802.11AC}	40 MHz, 256 QAM, MCS9, DEVM = 1.8%, 802.11ac mask compliant DEVM = 1.4%	+16	+15		dBm dBm
Output power, 802.11b	P _{OUT_802.11B}	11 Mbps CCK signal, BT = 0.45, ACPR (±11 MHz offset) < -35, ACPR (±22 MHz offset) < -56		+21		dBm
1 dB compression point	P1dB		+24.0	+24.5		dBm
Small signal gain	IS21I		25		31	dB
Small signal gain variation over any 40 MHz channel	ΔIS21I	Switch state 2		0.5	1.0	dB
Small signal gain variation over band	ΔIS21I			1	2	dB
Small signal gain @ ½ VCO frequency	IS21I_1.6	1608 to 1656 MHz		12	20	dB
Small signal gain @ VCO frequency	IS21I_3.2	3216 to 3312 MHz 1206 to 1242 MHz 3618 to 3726 MHz			0 +12 -10	dB dB dB

Table 7. SE5516A Electrical Specifications: 2.4 GHz Transmit Characteristics (2 of 2) (Note 1)
(V_{CC} = ENG = C0 = 3.3 V, ENA = C1 = 0 V, T_A = +25 °C, All Unused Ports Terminated with 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
2 nd and 3 rd harmonics	2fo, 3fo	P _{OUT} ≤ +21 dBm, 1 Mbps, CCK			-48	dBm/MHz
		P _{OUT} ≤ +18 dBm, 802.11g/n, all data rates			-50	dBm/MHz
Delay and rise/fall time	t _{DR} , t _{DF}	50% of V _{EN} edge and 90/10% of final output power level			0.4	μs
Input return loss	S ₁₁			7		dB
Output return loss	S ₂₂			10		dB
Stability	STAB	CW, P _{OUT} = +21 dBm, 0.1 to 21 GHz, load VSWR = 6:1	All non-harmonically related outputs <-42 dBm/MHz			
Ruggedness	Ru	TG = +12 dBm, ANT load varies over 6:1 VSWR	No irreversible damage			

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 8. SE5516A Electrical Specifications: 2.4 GHz Receive Characteristics (Note 1)
(V_{CC} = 3.3 V, Switch Condition 1, T_A = +25 °C, All Unused Ports Terminated with 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f		2400		2500	MHz
Small signal gain, LNA enabled	S ₂₁	2400 to 2485 MHz	10	13	15	dB
Small signal gain, bypass mode	S ₂₁	LNA bypassed, switch condition 3	-9.5	-8.5	-7.5	dB
Small signal gain, high band gain @ 5150 to 5850 MHz	S ₂₁	Switch condition 1		-17		dB
Small signal gain variation	Δ S ₂₁	2400 to 2485 MHz, over any 40 MHz band		0.25	0.50	dB
Noise Figure	NF	De-embedded to device		2.5	2.8	dB
Input return loss	S ₁₁		5	10		dB
Output return loss	S ₂₂		8	10		dB
3 rd Order Input Intercept Point	IIP ₃	Switch condition 1		+2.4		dBm
1 dB input compression point	IP _{1dB}	LNA enabled	-7.5			dBm
		LNA bypassed, switch condition 3		+8.0		dBm
Loopback isolation (ANT to RG pins)	LB	Switch condition 2, P _{OUT} = P _{SAT}	P _{SAT} + 10	39		dB
Enable time	t _{EN}	50% of C0 or C1 edge and 90/100% of final output power levels: (Note 2) (Note 3)			0.2	μs
					1.0	μs

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: Timing applies when transitioning in either direction between switch conditions 1 and 3 (see Table 13).

Note 3: Timing applies when transitioning in either direction between switch conditions 2, 4, 5, or 6 and switch conditions 1 or 3 (see Table 13).

Table 9. SE5516A Electrical Specifications: 5.0 GHz Transmit Characteristics (Note 1)
(V_{CC} = ENA = CO = 3.3 V, ENG = C1 = 0 V, TA = +25 °C, All Unused Ports Terminated with 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f		4900		5900	MHz
Output power, 802.11n	P _{OUT_802.11N}	OFDM signal, MCS7, HT40, DEVM = 3%, 802.11n mask compliant, ±11 MHz offset, RBW = 100 kHz, VBW = 30 kHz DEVM = 2.7%	+16 +15			 dBm dBm
Output power, 802.11ac	P _{OUT_802.11AC}	80 MHz, 256 QAM, MCS9, DEVM = 1.8%, input signal EVM < 0.6%, 802.11ac mask compliant DEVM = 1.6%	+13 +12			 dBm dBm
1 dB compression point	P1dB		+21.0	+22.5		dBm
Small signal gain	S21	In band @ 1.640 to 1.942 GHz @ 3.280 to 3.900 GHz	+25		+32 0 +2	 dB dB dB
Small signal gain variation over 80 MHz channel	Δ S21				1	dB
Small signal gain variation over sub-bands	Δ S21	5.15 to 5.50 GHz and 5.70 to 5.90 GHz			2	dB
Isolation	S12	Switch state 5, 4.9 to 5.9 GHz			-45	dB
2 nd and 3 rd harmonics	2fo, 3fo	@ +20 dBm, MCS0			-50	dBm/MHz
Delay and rise/fall time	t _{DR} , t _{DF}	50% of V _{EN} edge and 90/10% of final output power level			0.4	μs
Input return loss	S11			10		dB
Output return loss	S22			10		dB
Stability	STAB	64 QAM, P _{OUT} = +16 dBm, 0.1 to 21 GHz, load VSWR = 6:1	All non-harmonically related outputs <-42 dBm/MHz			-
Ruggedness	Ru	TA = +12 dBm, ANT load varies over 6:1 VSWR	No irreversible damage			-

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 10. SE5516A Electrical Specifications: 5.0 GHz Receive Characteristics (Note 1)
(V_{CC} = 3.3 V, Switch Condition 4, T_A = +25 °C, All Unused Ports Terminated with 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f		4900		5850	MHz
Small signal gain	S ₂₁	Switch condition 4: 4900 to 5850 MHz 2400 to 2500 MHz	+10	+12 -28	+14 -17	dB dB
Small signal gain, bypass mode	S ₂₁	LNA bypassed, switch condition 6	-10.5	-9.0	-7.5	dB
Small signal gain variation	Δ S ₂₁	4900 to 5850 MHz, over any 80 MHz band Over entire band	-0.5 -1.0		+0.5 +1.0	dB dB
Noise Figure	NF	De-embedded to device		2.8	3.0	dB
Input return loss	S ₂₁		8	10		dB
Output return loss	S ₂₂		6	10		dB
3 rd Order Input Intercept Point	IIP ₃	Switch condition 4		+3.5		dBm
1 dB input compression point	IP _{1dB}	LNA enabled LNA bypassed, switch condition 6	-6 +6			dBm dBm
Loopback isolation (ANT to RA pins)	LB	Switch condition 5, P _{OUT} = P _{SAT}		33		dB
Enable time	t _{EN}	50% of C0 or C1 edge and 90/100% of final output power levels: (Note 2) (Note 3)			0.2 1.0	μs μs

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: Timing applies when transitioning in either direction between switch conditions 4 and 6 (see Table 13).

Note 3: Timing applies when transitioning in either direction between switch conditions 1, 2, 3, or 5 and switch conditions 4 or 6 (see Table 13).

Table 11. SE5516A Electrical Specifications: 2.4 GHz Power Detector Characteristics (Note 1)
(V_{CC} = 3.3 V, Switch Condition 2, T_A = +25 °C, All Unused Ports Terminated with 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f		2400		2500	MHz
Power detector range, peak power	PDR	Measured at ANT pin	0		+22	dBm
Output voltage @ P _{OUT} = +22 dBm	PDV _{P22}	Measured into 26.5 kΩ	0.70	0.83	0.95	V
Output voltage @ P _{OUT} = +18 dBm	PDV _{P18}	Measured into 26.5 kΩ		0.55		V
Output voltage, no RF output power	PDV _{PNO RF}	Measured into 26.5 kΩ	0.15	0.18	0.22	V
Power detector low-pass filter -3 dB corner frequency	LPF-3DB	Measured into 26.5 kΩ	35			MHz
Power detector accuracy	PDET _{ACC}	Measured into 3:1 load at ANT port	-1.5		+1.5	dB

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 12. SE5516A Electrical Specifications: 5.0 GHz Power Detector Characteristics (Note 1)
(V_{CC} = 3.3 V, Switch Condition 5, T_A = +25 °C, All Unused Ports Terminated with 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f		4900		5900	MHz
Power detector range, peak power	PDR	Measured at ANT pin	0		+21	dBm
Output voltage @ P _{OUT} = +20 dBm	PDV _{P20}	Measured into 26.5 kΩ: 5.15 to 5.35 GHz 5.47 to 5.725 GHz 5.725 to 5.875 GHz	0.80 0.82 0.75		1.00 1.02 0.95	V V V
Output voltage @ P _{OUT} = +16 dBm	PDV _{P16}	Measured into 26.5 kΩ		0.60		V
Output voltage, no RF output power	PDV _{PNO RF}	Measured into 26.5 kΩ	0.15	0.18	0.22	V
Power detector low-pass filter –3 dB corner frequency	LPF-3DB	Measured into 26.5 kΩ	35			MHz
Power detector accuracy	PDET _{ACC}	Measured into 3:1 load at ANT port	–1.5		+1.5	dB

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

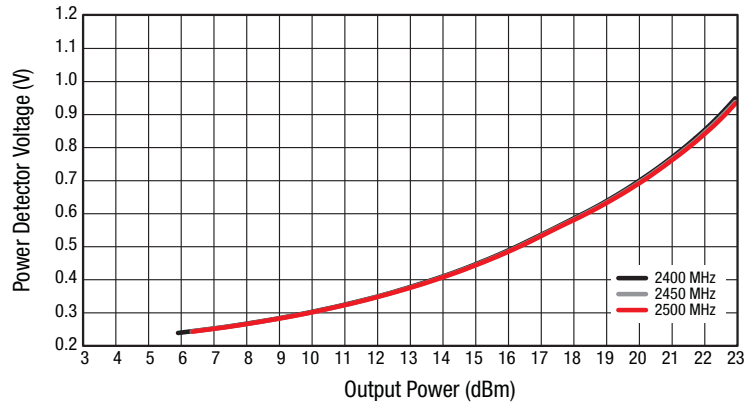


Figure 3. Power Detector vs Output Power Over Frequency @ 2.5 GHz

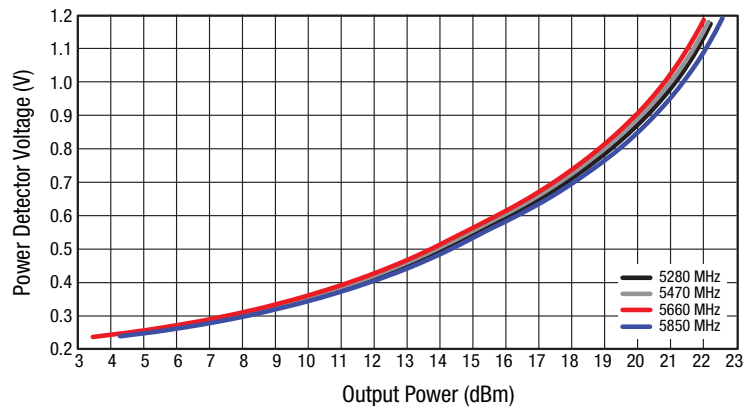


Figure 4. Power Detector vs Output Power Over Frequency @ 5.0 GHz

Evaluation Board Description

The SE5516A Evaluation Board is used to test the performance of the SE5516A WLAN FEM. An Evaluation Board schematic diagram is provided in Figure 5. A photograph of the Evaluation Board is shown in Figure 6. Component values for the SE5516A Evaluation Board are listed in Table 14.

Evaluation Board Setup Procedure

- Step 1: Connect system ground to pin 2 of connector J6.
 Step 2: Apply 3.3 V to pin 1 of connector J6.
 Step 3: Select a path according to the logic shown in Table 13.

Package Dimensions

The PCB layout footprint for the SE5516A is provided in Figure 7. Typical case markings are shown in Figure 8. Package dimensions for the 24-pin LGA are shown in Figure 9, and tape and reel dimensions are provided in Figure 10.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

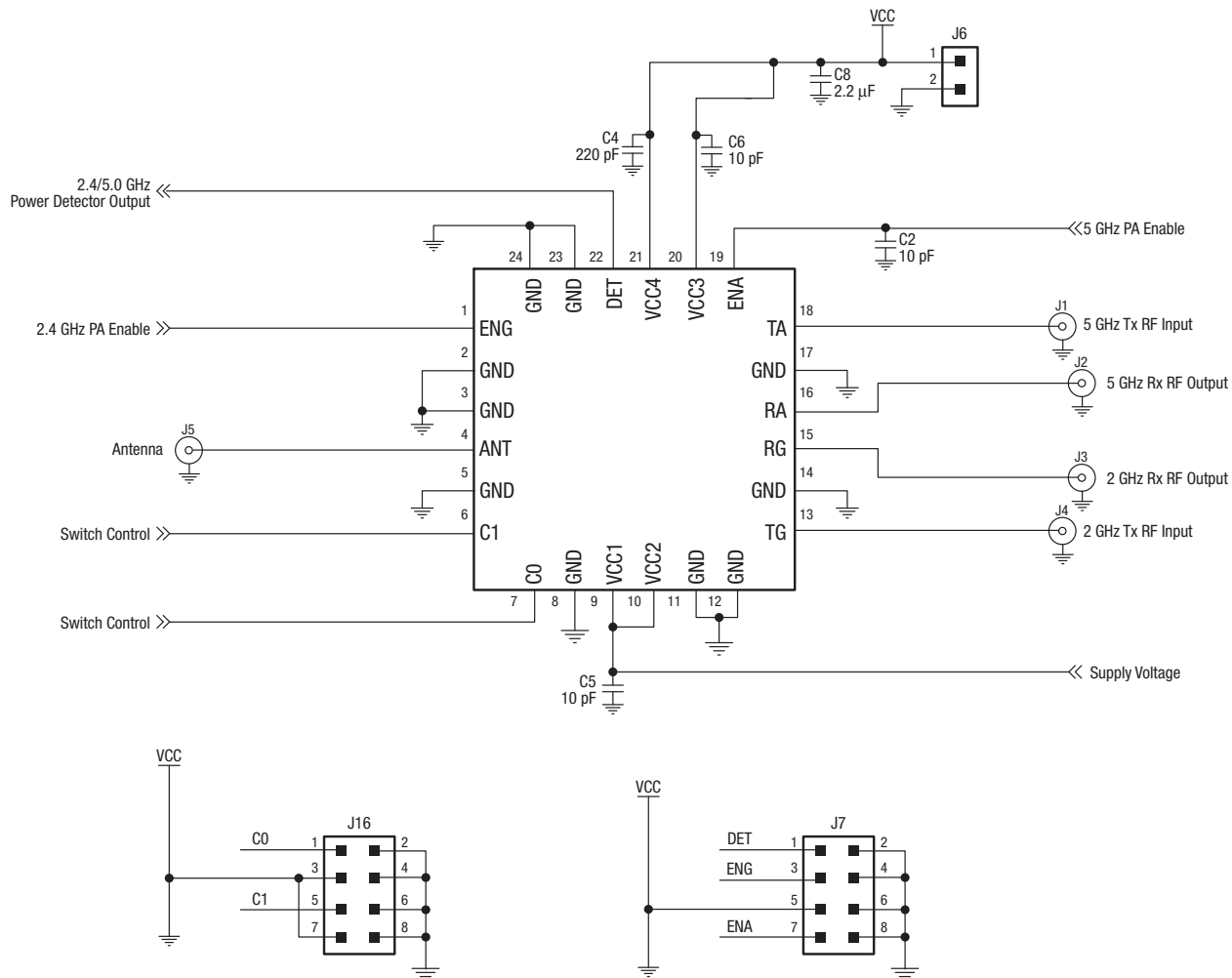
The SE5516A is rated to Moisture Sensitivity Level 3 (MSL3) at 240 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

Table 13. SE5516A Evaluation Board Switch Control Logic

Condition	Logic				State		
	C0 (Pin 1, J16 Header)	C1 (Pin 5, J16 Header)	ENA (Pin 7, J7 Header)	ENG (Pin 3, J7 Header)	SP3T	LNA	Bypass
1	0	1	0	0	RG	RG enable	Open
2	0	0	0	1	TG	RG off	RG bypass
3	0	0	0	0	RG	RG off	RG bypass
4	1	1	0	0	RA	RA enable	Open
5	1	0	1	0	TA	RA off	RA bypass
6	1	0	0	0	RA	RA off	RA bypass

Note: "0" = 0 V. "1" = +3.3 V. Any state other than described in this Table places the switch into an undefined state. An undefined state will not damage the device.



Note: Some component labels may be different than the corresponding component symbol shown here. Component values, however, are accurate as of the date of this Data Sheet.

S2935

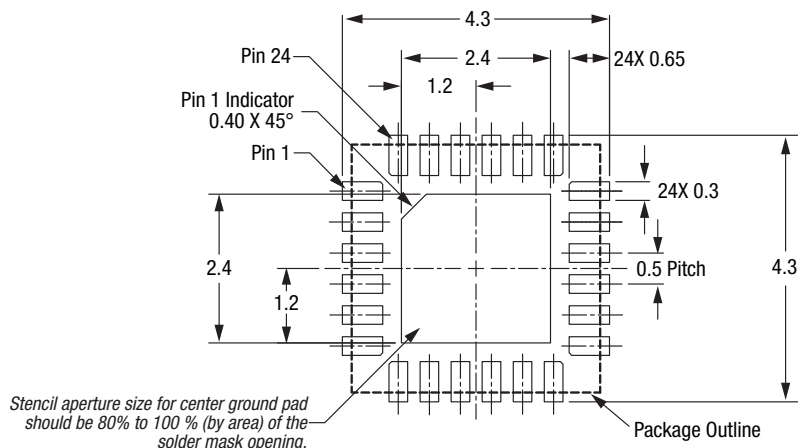
Figure 5. SE5516A Evaluation Board Schematic



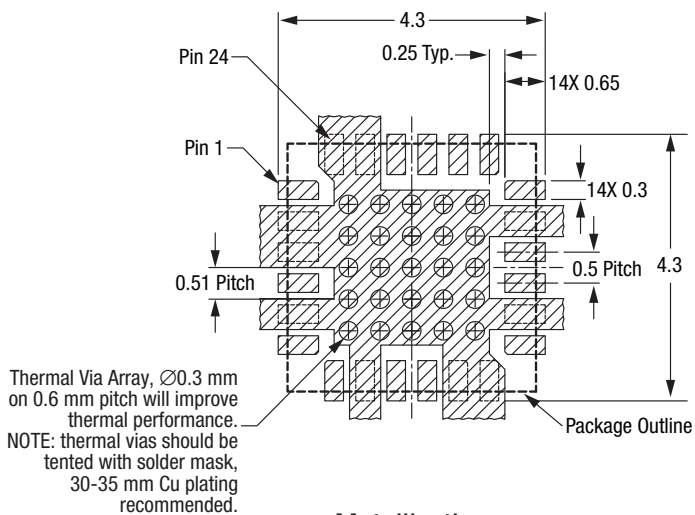
Figure 6. SE5516A Evaluation Board Photo

Table 14. SE5516A Evaluation Board Bill of Materials

Component	Size	Value	Vendor	Part #	Comments
C2, C5, C6	0402	10 pF	Murata	GRM1555C1H100JZ01	Multilayer ceramic
C4	0402	220 pF	Murata	GRM1555C1H221JA01	Multilayer ceramic
C8	0805	2.2 μ F	Murata	GRM21BR71A225KA01L	Ceramic capacitor, 10 V, 10% X7R

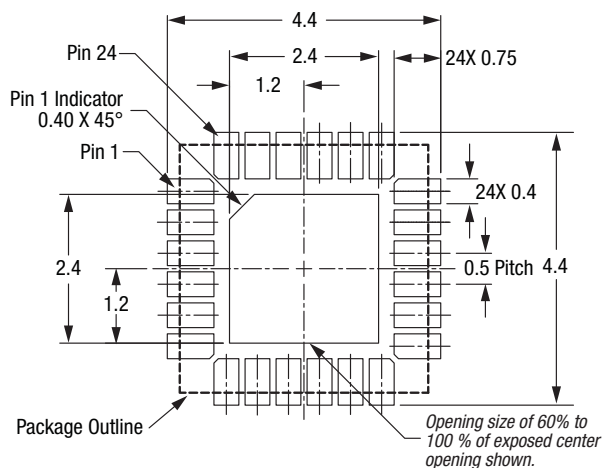


Stencil Aperture Top View



Thermal Via Array, $\varnothing 0.3$ mm on 0.6 mm pitch will improve thermal performance.
NOTE: thermal vias should be tented with solder mask, 30-35 μ m Cu plating recommended.

Metallization Top View



Solder Mask Opening Top View

All dimensions are in millimeters

S3017

Figure 7. SE5516A PCB Layout Footprint

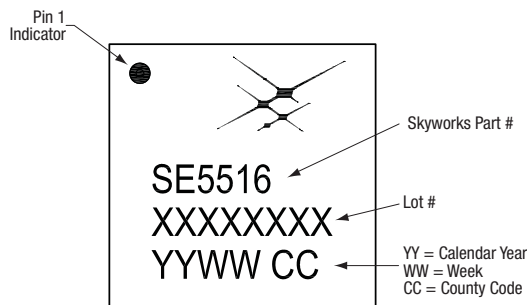
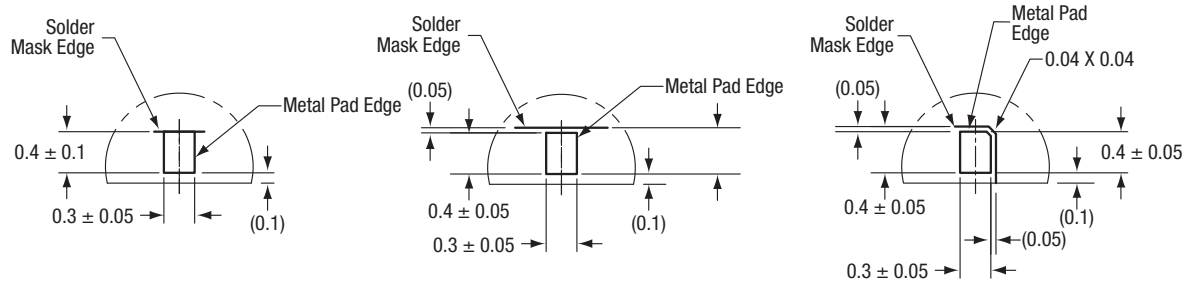
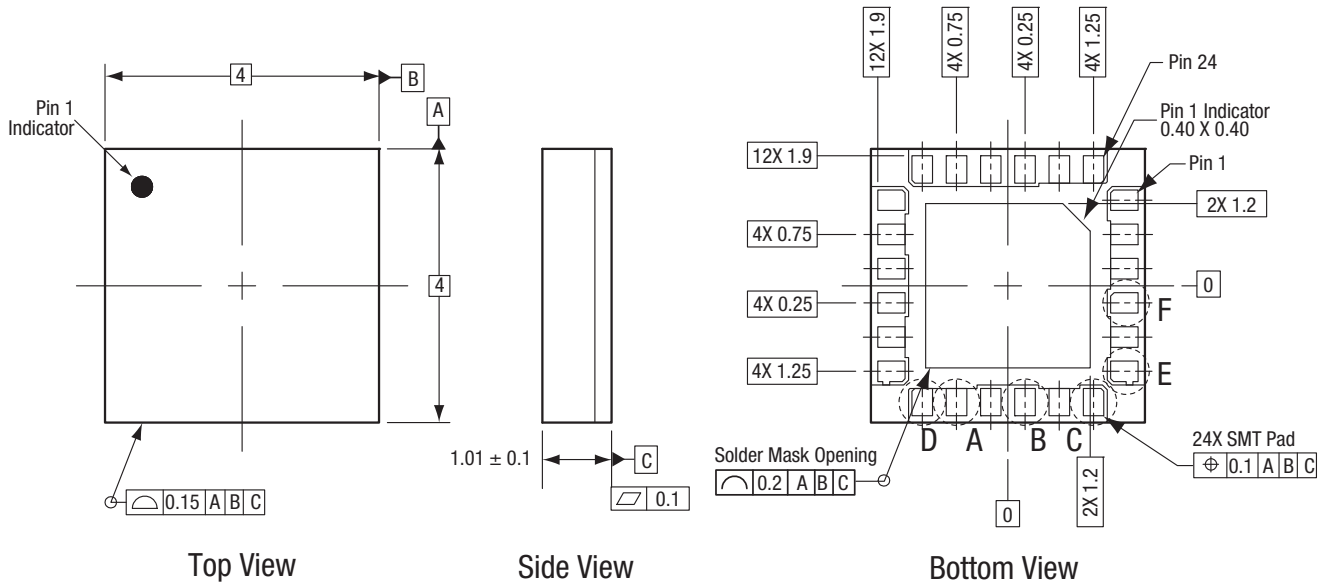


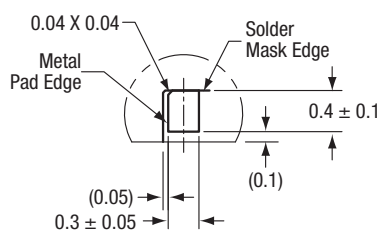
Figure 8. Typical Case Markings (Top View)



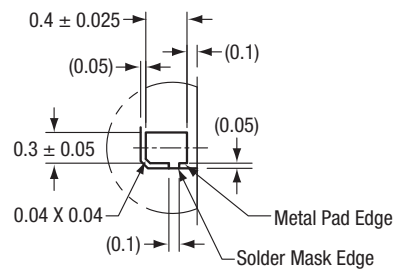
Detail A
Pad
Scale: 2X
2X This rotation
1X Rotated 180°
2X Rotated 90° CW
3X Rotated 90° CCW

Detail B
Pad
Scale: 2X
2X This rotation
3X Rotated 180°
2X Rotated 90° CW

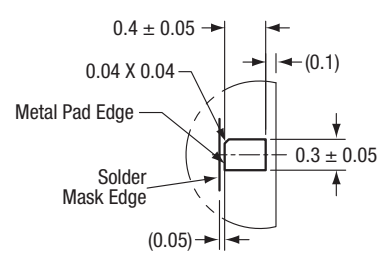
Detail C
Pad
Scale: 2X
1X This rotation
1X Rotated 180°
1X Rotated 90° CCW
1X Mirrored 45°



Detail D
Pad
Scale: 2X
1X This rotation
1X Rotated 180°



Detail E
Pad
Scale: 2X
1X This rotation
1X Mirrored 180°



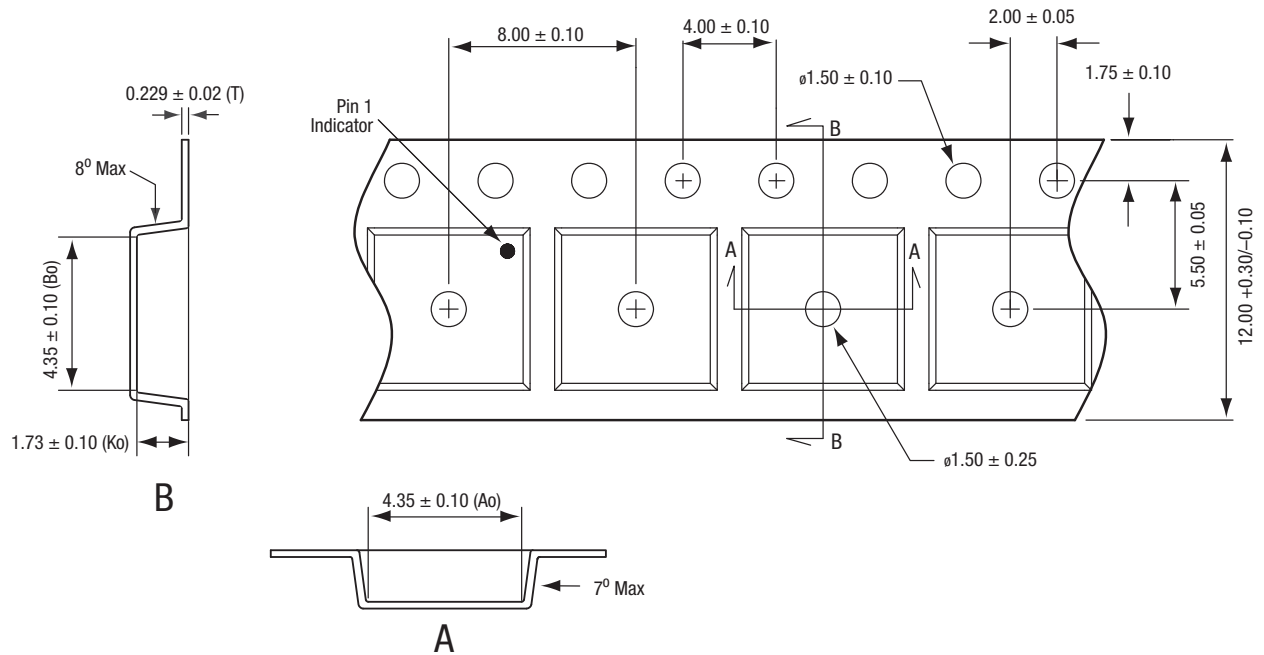
Detail F
Pad
Scale: 2X
1X This rotation

All measurements are in millimeters

Dimensioning and tolerancing according to ASME Y14.5M-1994

S2933

Figure 9. SE5516A 24-Pin LGA Package Dimensions



Notes:

1. Carrier tape material: black conductive polycarbonate or polystyrene
2. Cover tape material: transparent conductive PSA
3. Cover tape size: 9.3 mm width
4. ESD surface resistivity is $\leq 1 \times 10^8$ Ohms/square per EIA, JEDEC tape and reel specification.
5. Tolerance: .XX = ± 0.10
6. All measurements are in millimeters

S3496

Figure 10. SE5516A Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SE5516A WLAN FEM	SE5516A	SE5516A-EVB

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