

SE80100

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

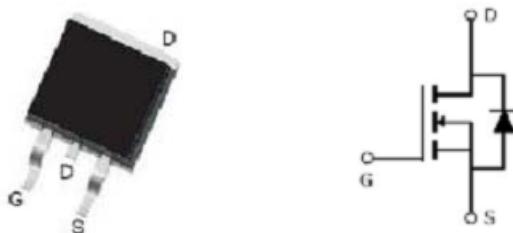
Features

For a single MOSFET

- $V_{DS} = 80V$
- $R_{DS(ON)} = 6.8m\Omega @ V_{GS}=10$

Pin configurations

See Diagram below



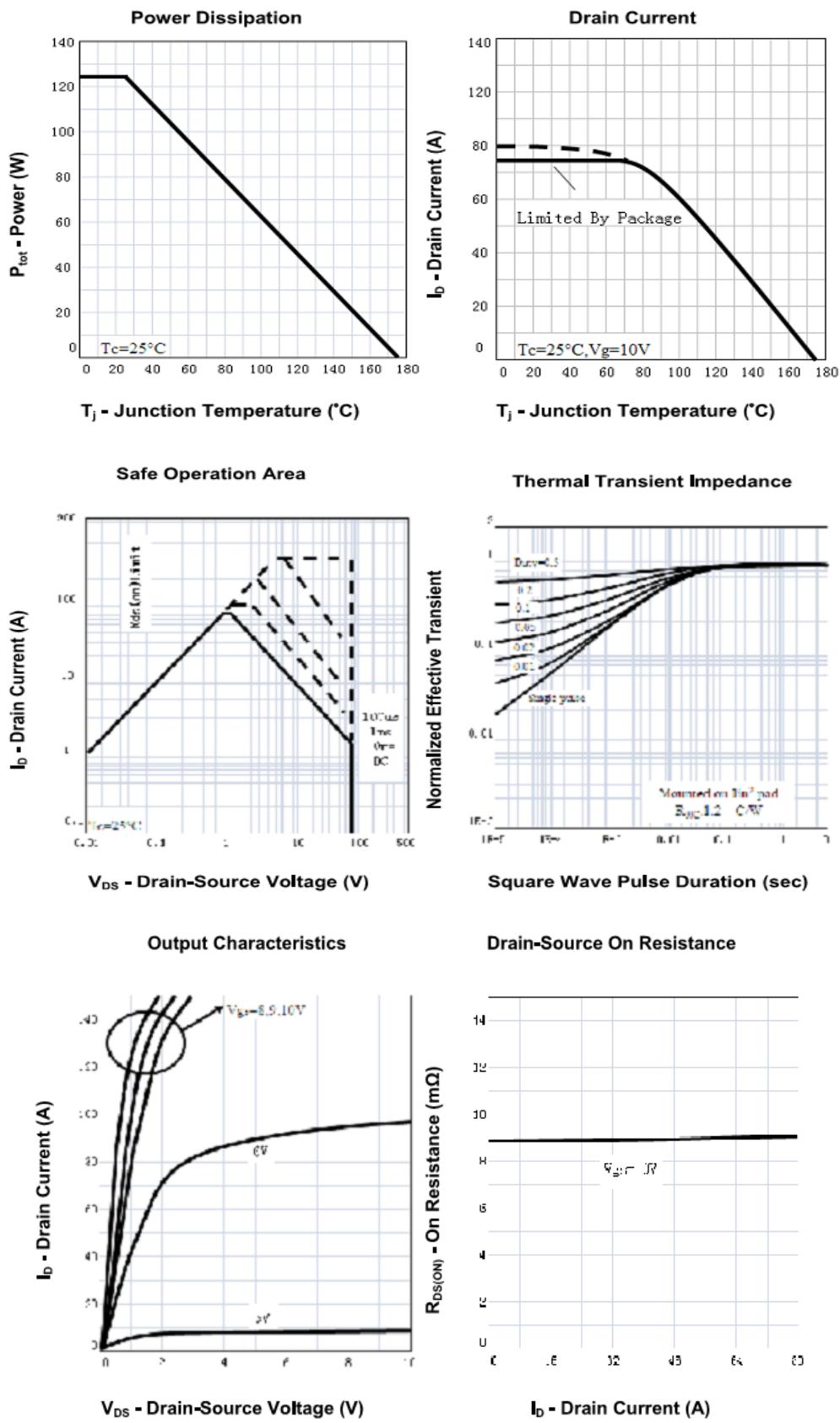
Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	Continuous	I_D	A
Pulsed			
Total Power Dissipation @ $T_A=25^\circ C$	P_D	125	W
Operating Junction Temperature Range	T_J	-55 to 175	°C

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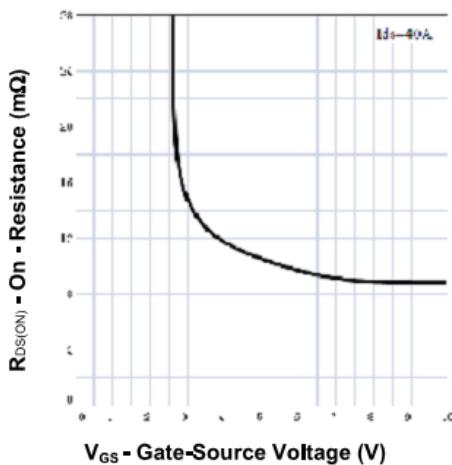
Electrical Characteristics (TJ=25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0 V	80			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 64V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	2		4	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =40A	-	6.8	8	mΩ
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =40V, f=1MHz		4120		pF
C _{oss}	Output Capacitance			520		pF
C _{rss}	Reverse Transfer Capacitance			200		pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =64V, I _D =40A		58		nC
Q _{gs}	Gate Source Charge			15		nC
Q _{gd}	Gate Drain Charge			19		nC
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =40V, R _{GEN} =4.7Ω I _D =2A		34		ns
t _{d(off)}	Turn-Off Delay Time			103		ns
t _{d(r)}	Turn-On Rise Time			95		ns
t _{d(f)}	Turn-Off Fall Time			33		ns
Thermal Resistance						
Symbol	Parameter		Typ	Max	Units	
R _{θJC}	Thermal Resistance Junction to Case(t≤10s)		-	1.2		°C/W

Typical Characteristics

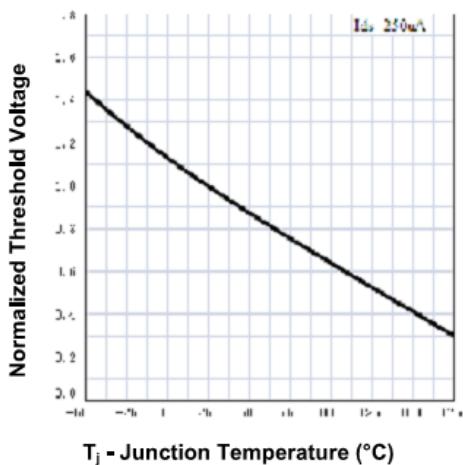


Typical Characteristics

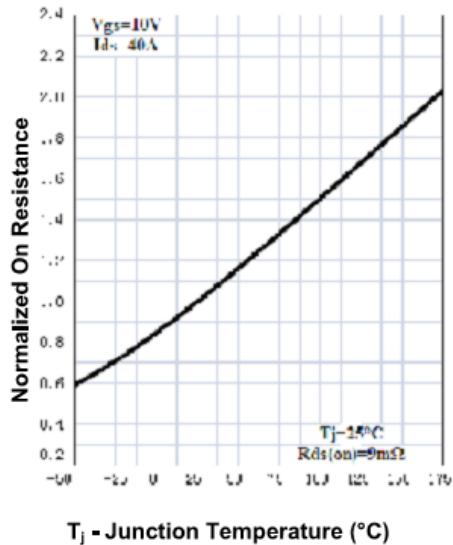
Drain-Source On Resistance



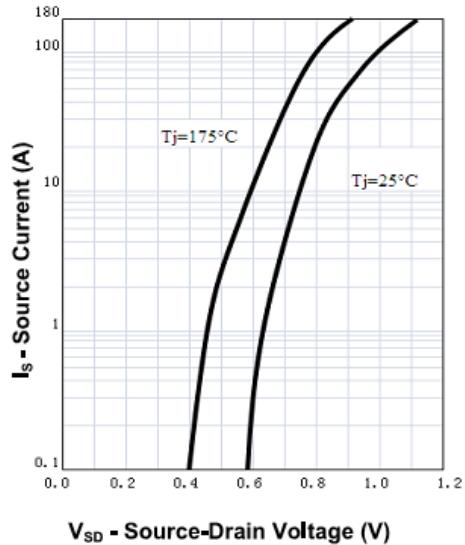
Gate Threshold Voltage



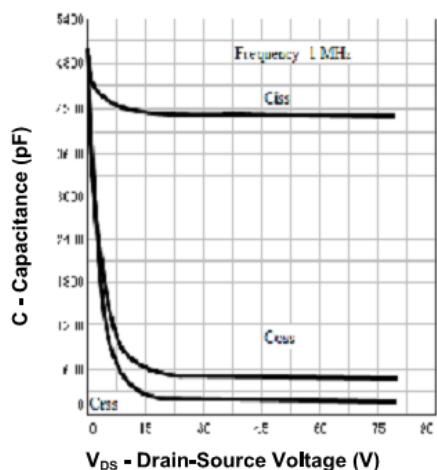
Drain-Source On Resistance



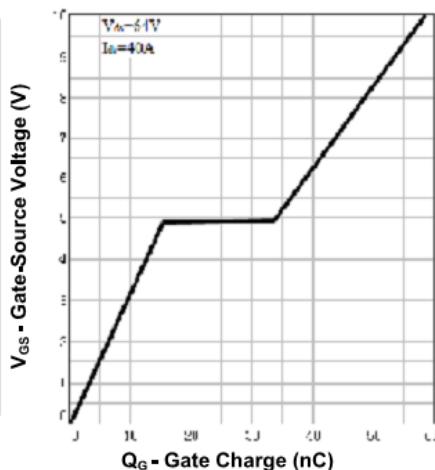
Source-Drain Diode Forward



Capacitance



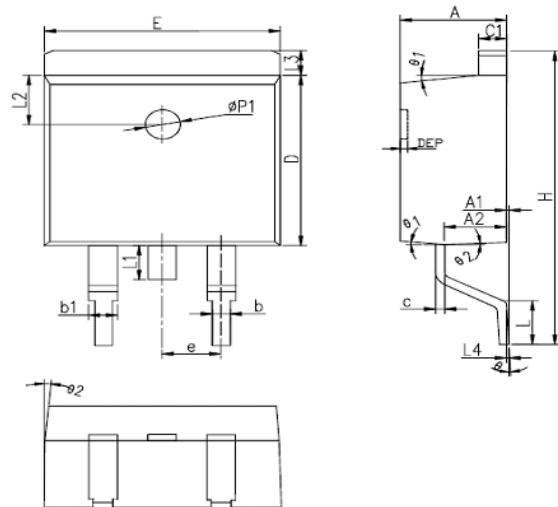
Gate Charge



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Package Outline Dimension

TO-263



SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185	L	2.00	2.30	2.60	0.079	0.090	0.102
A1	0	0.10	0.25	0	0.004	0.010	L3	1.17	1.27	1.40	0.046	0.050	0.055
A2	2.59	2.69	2.79	0.102	0.106	0.110	L1	-	-	1.70	-	-	0.067
b	0.77	-	0.90	0.030	-	0.035	L4	0.25BSC			0.01BSC		
b1	1.23	-	1.36	0.048	-	0.052	L2	2.50REF.			0.098REF.		
c	0.34	-	0.47	0.013	-	0.019	Ø 1	0°	-	8°	0°	-	8°
C1	1.22	-	1.32	0.048	-	0.052	Ø 2	5°	7°	9°	5°	7°	9°
D	8.60	8.70	8.80	0.338	0.343	0.346	DEP	1°	3°	5°	1°	3°	5°
E	10.00	10.16	10.26	0.394	0.4	0.404	Øp1	0.05	0.10	0.20	0.002	0.004	0.008
e	2.54BSC			0.1BSC				1.40	1.50	1.60	0.055	0.059	0.063
H	14.70	15.10	15.50	0.579	0.594	0.610							

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