



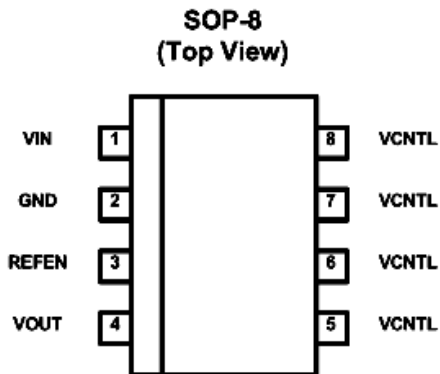
**Description**

The SE9174 regulator is designed to convert voltage supplies ranging from 1.6V to 6V into a desired output voltage, which is adjusted by two external voltage divider resistors. The regulator is capable of sourcing or sinking up to 2.0A of current while regulating an output voltage to within 2% (DDR 1 or DDR 2) or less.

The SE9174, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed back-plane designs. The voltage output of the regulator can be used as a termination voltage for DDR SDRAM.

Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of the output fault conditions.

**Pin Configuration**



**Features**

- Support Both DDR 1 (1.25V<sub>TT</sub>) and DDR 2 (0.9V<sub>TT</sub>) Requirements
- SOP-8 Packages
- Capable of Sourcing and Sinking Current 2.0A
- Current-limiting Protection
- Thermal Protection
- Current-shoot-through protection
- Integrated Power MOSFETs
- Generates Termination Voltages for SSTL-2
- High Accuracy Output Voltage at Full-Load
- Adjustable Vout by External Resistors
- Minimum External Components
- Shutdown for Standby or Suspend Mode Operation with High-impedance Output

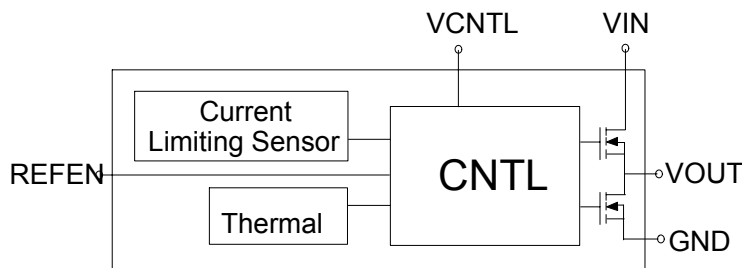
**Application**

- DDR Memory Termination
- Active Termination Buses
- Supply Splitter

**Pin Description**

Pin Name	Pin function
V <sub>IN</sub>	Power Input
GND	Ground
V <sub>CNTL</sub>	Gate Drive Voltage
REFEN	Reference Voltage input and Chip Enable
V <sub>OUT</sub>	Output Voltage

**Block Diagram**





**Absolute Maximum Rating <sup>(1)</sup>**

Parameter	Symbol	Value	Unit
Input Voltage	V <sub>IN</sub>	6	V
Power Dissipation	P <sub>D</sub>	Internally Limited	--
ESD Rating	--	3	KV
Storage Temperature Range	T <sub>S</sub>	-65 to 150	°C
Lead Temperature (Soldering, 5 sec.)	T <sub>LEAD</sub>	260	°C
Package Thermal Resistance	Θ <sub>JC</sub>	15.7	°C/W

**Electrical Characteristics**

V<sub>IN</sub>=2.5V, V<sub>CNTL</sub>=3.3V, V<sub>REFEN</sub>=1.25V, C<sub>OUT</sub>=10μF (Ceramic), T<sub>A</sub>=25°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Offset Voltage <sup>(2)</sup>	V <sub>OS</sub>	I <sub>OUT</sub> = 0A	-20	-5	20	mV
Load Regulation (DDR 1/2)	ΔV <sub>LOAD</sub>	I <sub>L</sub> : 0A→2.0A	--	0.5	2	%
		I <sub>L</sub> : 0A→-2.0A	--	0.5	2	
Input Voltage Range (DDR 1/2)	V <sub>IN</sub>	Keep V <sub>CNTL</sub> ≥ V <sub>IN</sub> on operation power on and power off sequences	1.6	2.5/1.8	--	V
	V <sub>CNTL</sub>		--	3.3	6	
Current In Shutdown Mode	I <sub>SHDN</sub>	V <sub>REFEN</sub> < 0.2V, R <sub>L</sub> = 180Ω	--	1	90	μA
Short Circuit Protection						
Current limit	I <sub>LIMIT</sub>		--	2.5	--	A
Quiescent Current	I <sub>Q</sub>	I <sub>L</sub> =2.0A	--	1.4	3	mA
Over Temperature Protection						
Thermal Shutdown Temperature	T <sub>CASE</sub>	3.3V ≤ V <sub>CNTL</sub> ≤ 5V	--	100	--	°C
Thermal Shutdown Hysterresis		Guaranteed by design	--	30	--	
Shutdown Function						
Shutdown Threshold Trigger		Output=High	0.8	--	--	V
		Output=Low	--	--	0.2	

**Note 1:** Exceeding the absolute maximum rating may damage the device.

**Note 2:** V<sub>OS</sub> offset is the voltage measurement defined as V<sub>OUT</sub> subtracted from V<sub>REFEN</sub>

## Application Information

### Internal parasitic diode

www.datasheet4u.com  
Avoid forward-bias internal parasitic diode,  $V_{OUT}$  to  $V_{CNTL}$ , and  $V_{OUT}$  to  $V_{IN}$ , the  $V_{OUT}$  should not be forced same voltage respect to ground on this pin while the  $V_{CNTL}$  or  $V_{IN}$  is disappeared.

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on  $V_{REFEN}$  is below 0.2V.

In addition to item1, the capacitor and voltage divider form the low-pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.

### Thermal Consideration

SE9174 regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continuous normal load conditions however, the maximum junction temperature rating of 150°C must not be exceeded. Higher continuous currents or ambient temperature require additional heatsinking. Heat sinking to the IC package must consider the worst case power dissipation which may occur.

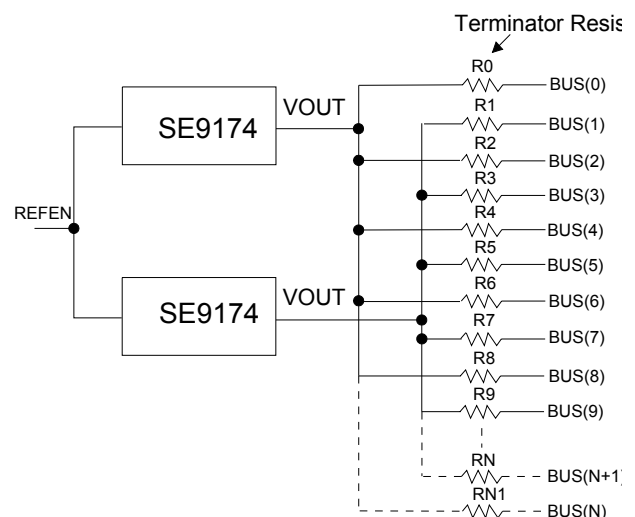
It should also be noted that with the  $V_{CNTL}$  equal to 5V, the point of thermal shutdown will be degraded by approx. 20°C compared to the  $V_{CNTL}$  equipped with 3.3V. It is highly recommended that to use the 3.3V rail acting as the  $V_{CNTL}$  so as to minimize the thermal concern of the SE9174 in the SOP-8 package.

## Layout Consideration

The SE9174 regulator is packaged in thermally enhanced plastic SOP-8 package. This small footprint package is unable to convectively dissipate the heat generated when the regulator is operating at high current levels. In order to control die operating temperatures, the PC board layout should allow for maximum possible copper area at the  $V_{CNTL}$  pins of the SE9174.

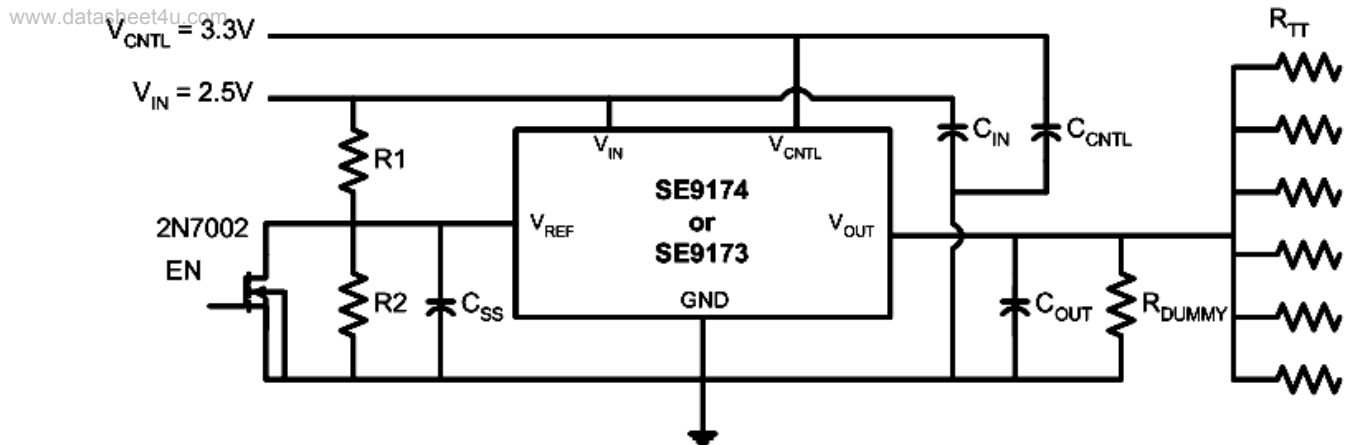
The multiple  $V_{CNTL}$  pins on the SOP-8 package are internally connected, but lowest thermal resistance will result if these pins are tightly connected on the PC board. This will also aid heat dissipation at high power levels.

If the large copper around the IC is unavailable, a buried layer may be used as a heat spreader, Use via to conduct the heat into the buried or backside of PCB layer. The via should be small enough to retain solder when the board is wave-soldered.





### Application Diagram



$R_1 = R_2 = 100\text{K}\Omega$ ,  $R_{TT} = 50\Omega/33\Omega/25\Omega$

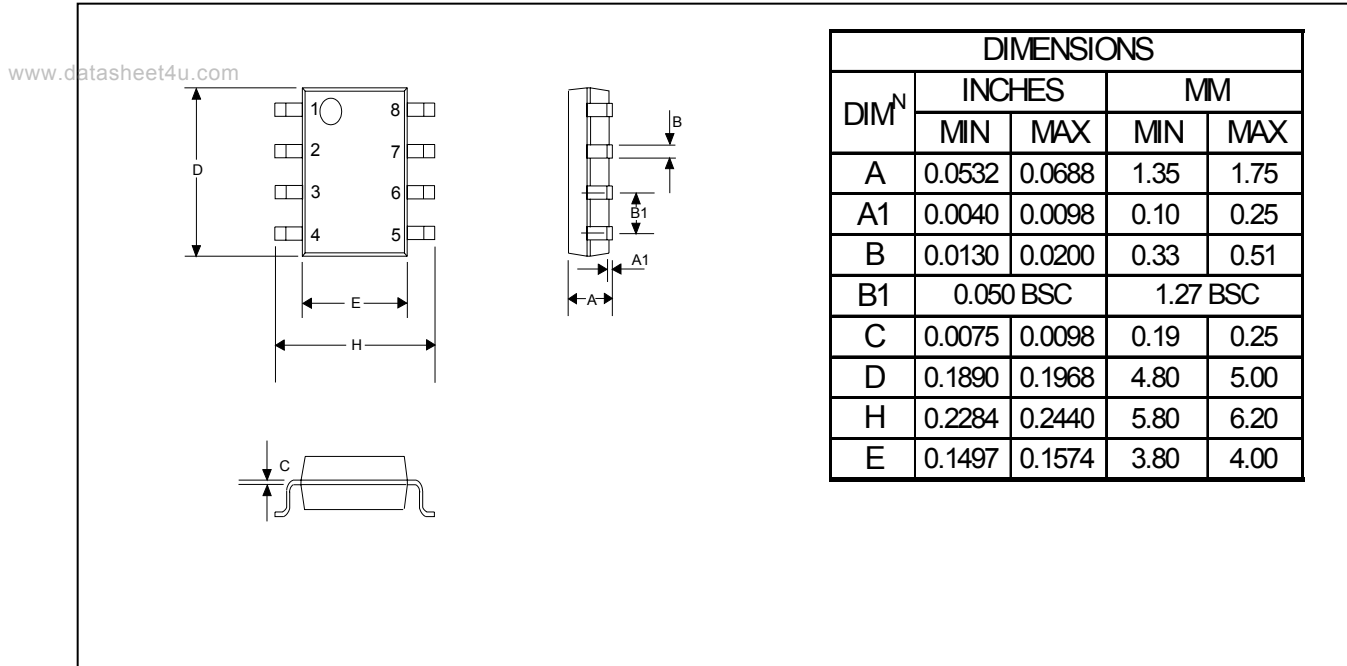
$C_{OUT, \min} = 10\mu\text{F}$  (Ceramic) +  $1000\mu\text{F}$  under the worst case testing condition

$R_{DUMMY} = 1\text{K}\Omega$  as for  $V_{OUT}$  discharge when  $V_{IN}$  is not present but  $V_{CNTRL}$  is present

$C_{SS} = 1\mu\text{F}$ ,  $C_{IN} = 470\mu\text{F}$  (Low ESR),  $C_{CNTRL} = 47\mu\text{F}$



**Outline Drawing SOP-8**



**Contact Information**

Seaward Electronics Incorporated – China

Room 1605, Building 1, International Pioneering Park, #1 Shangdi Xinxi Rd.

Haidian District, Beijing 100085, China

Tel: 86-10-8289-5700/01/05

Fax: 86-10-8289-5706

Email: sales@seawardinc.com.cn

Seaward Electronics Corporation – Taiwan

2F, #181, Sec. 3, Min Quan East Rd.

Taipei, Taiwan R.O.C

Tel: 886-2-2712-0307

Fax: 886-2-2712-0191

Email: sales@seawardinc.com.tw

Seaward Electronics Incorporated – North America

49 Showers Dr. J126

Mountain View, CA 94040, USA

Tel: 1-408-821-6600

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