SED1181

CMOS LCD 64-SEGMENT DRIVER

■ DESCRIPTION

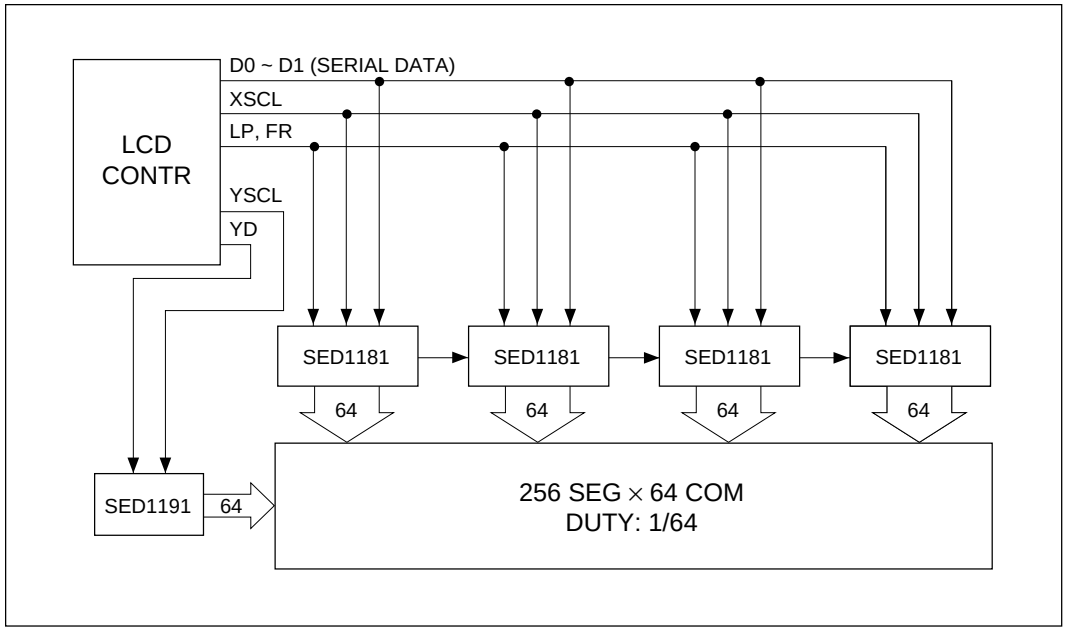
The SED1181 is a dot matrix LCD segment (column) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI contains 64-bit shift register for display data. The display data is supplied through LCD controller, and serially transferred through 16 × 4 shift register. The display data is held in a 64-bit latch circuit. The LSI converts the level of the latched data to an LCD drive waveform.

The SED1181 is used in conjunction with the SED1191 (64-bit row driver) to drive a large-capacity dot-matrix LCD panel.

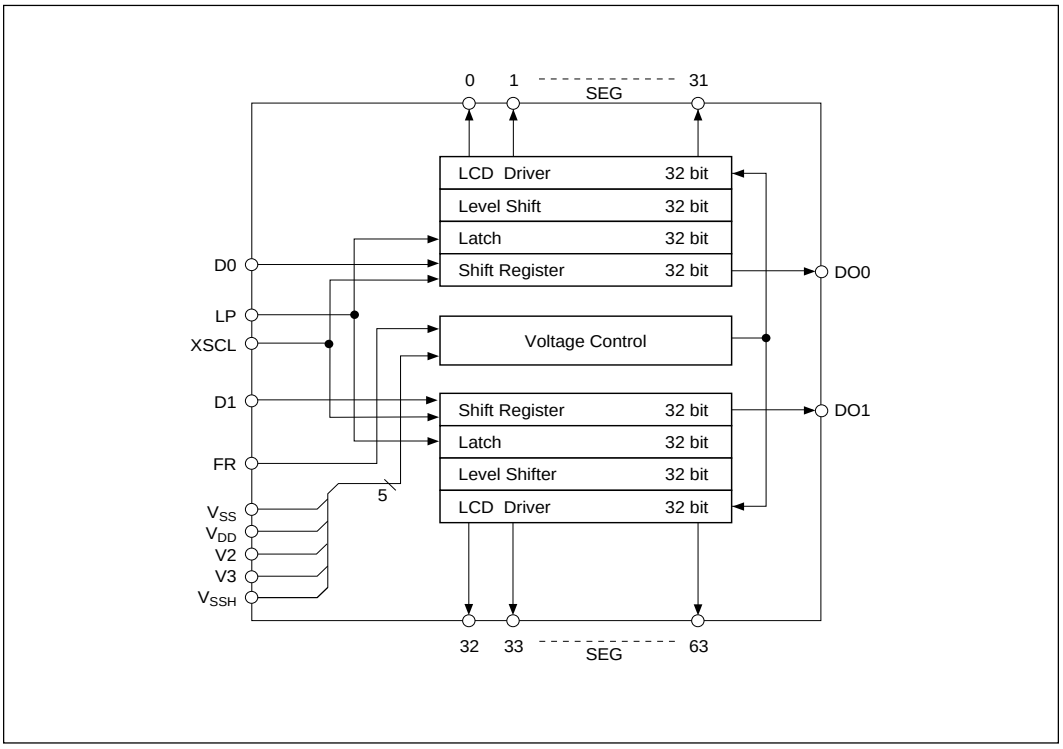
■ FEATURES

- Low-power CMOS technology
- 64-bit segment (column) driver
- Serial 2-bit input data
- Duty cycle ..... 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage ..... –14V to –25V
- Supply voltage ..... 5.0V ± 10%
- Package ..... QFP1-80 pin (F_{0A})
  QFP5-80 pin (F_{5A})

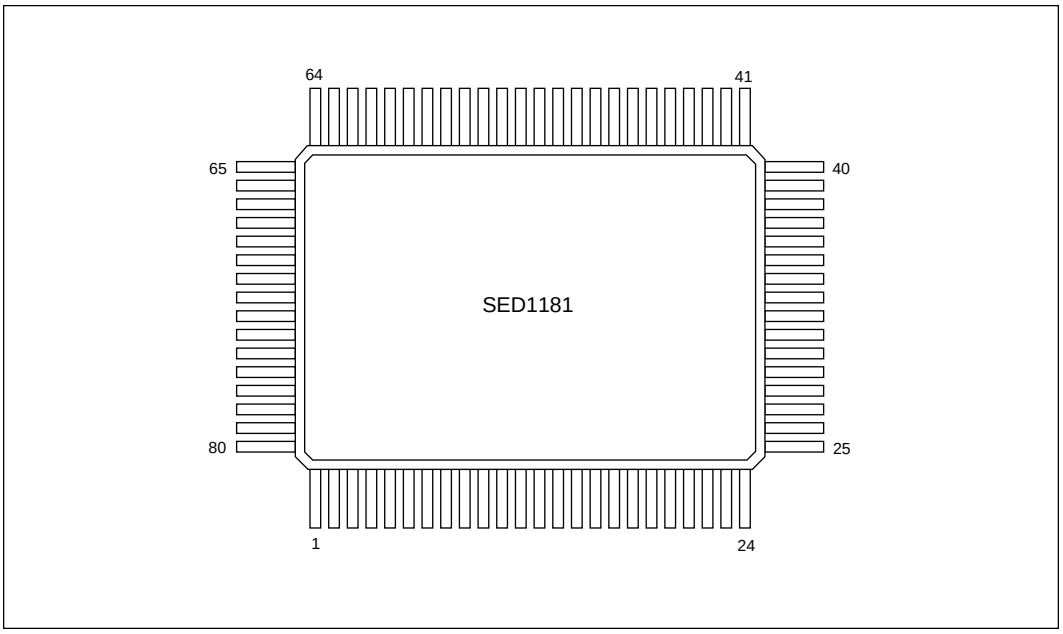
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



Number	Name	Number	Name	Number	Name	Number	Name
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	DO0	49	SEG44	69	V_{SSH}
10	SEG18	30	NC	50	SEG45	70	V2
11	SEG17	31	NC	51	SEG46	71	V3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	DO1
15	SEG13	35	LP	55	SEG50	75	NC
16	SEG12	36	FR	56	SEG51	76	NC
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

■ PIN DESCRIPTION

Pin Name	Function
D0	Serial data input to upper shift register
D1	Serial data input to lower shift register
SEG0 to SEG 31	Segment driver outputs supplied by the upper shift register
SEG 32 to SEG 63	Segment driver outputs supplied by the lower shift register
XSCL	Data shift clock input
LP	Data latch pulse input
FR	LCD frame signal input
DO0	Serial data output from upper shift register
DO1	Serial data output from lower shift register
V_{DD}, V_{SS}	Logic circuitry power inputs
V_{SSH}, V2, V3	LCD drive power inputs $V_{DD} > V2 > V3 > V_{SSH}$

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_{SSH}	–28.0 to +0.3	V
	V2, V3		
Input voltage	V_I	V_{SS} -0.3 to +0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–65 to +150	°C
Soldering temperature, time	T_{sol}	260°C, 10 sec (at lead)	°C / Sec

Notes:

1. All voltages are based on a V_{DD} of 0V.
2. V2 and V3 must satisfy the condition $V_{DD} \geq V2, V3 \geq V_{SSH}$.
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced during the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

● **DC Electrical Characteristics**

(V_{DD} = 0V, V_{SS} = –5.0V ± 10%, T_a = –20 to 75°C)

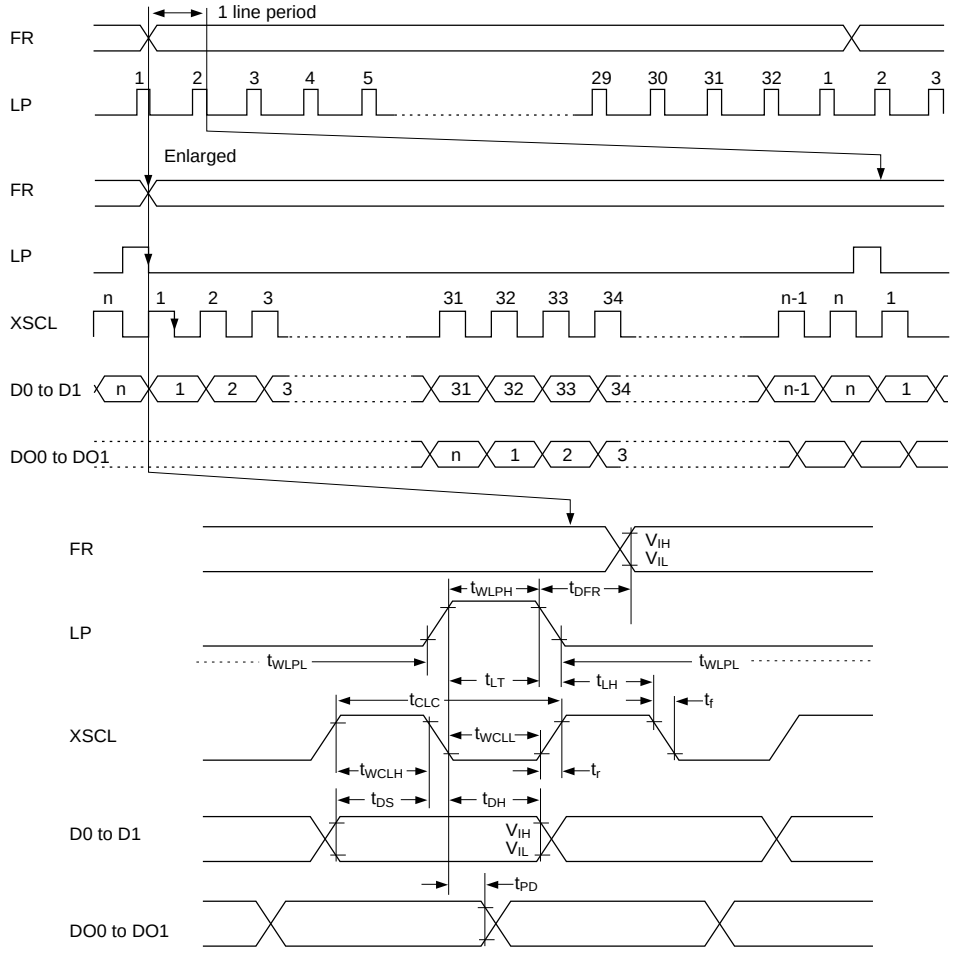
Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Supply voltage (1)	V_{SS}		–5.5	–5.0	–4.5	V
Supply voltage (2)	V_2		V_{SSH}	—	V_{DD}	V
	V_3		V_{SSH}	—	V_{DD}	V
	V_{SSH}		–25.0	—	–14.0	V
High level input voltage	V_{IH}		0.2V_{SS}	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}		V_{SS}–0.3	—	0.8V_{SS}	V
High level output voltage	V_{OH}	I_{OH} = –0.6 mA	–0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 0.6 mA	—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{SS}	—	0.05	2.0	µA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{SS}	—	0.05	5.0	µA
Shift clock	XSCL		—	—	6.0	MHz
Frame signal	FR		—	1/60	—	sec
Input capacitance	C_I	T_a = 25°C	—	5.0	8.0	pF
Segment output on resistance	R_{SEG}	V_{SSH} = –14.0 V V_{OH} = V_{DD} –0.5 V V_{OL} = V_{SSH} +0.5 V SEG./ bit	—	3.0	6.0	kΩ
Quiescent current	I_Q	V_{SSH} = –25.0V, V_{SS} = –5.5 V, V_I = V_{DD}	—	0.05	30	µA
Logic circuit	I_{SSOP}	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, FR period = 130 µs (duty 50%), LP period = 130 µS, XSCL frequency = 1.5 MHz (duty 50%)	—	850	1200	µA
LCD circuit operating current	I_{SSHOP}	V_{SS} = –4.5 V, V_2 = –4.0 V, V_3 = –16.0 V, V_{SSH} = –20.0 V, Other parameters as for I_{SSOP}	—	70	100	µA

Notes:

1. All voltages are based on a V_{DD} of 0V.
2. The driver will operate with a value of V_{SSH} in this range, however the "on" source impedance of a segment drive can be higher than at the recommended value of V_{SSH}. It is recommended that the drivers are tested with the LCD panel they will be used with to determine a suitable value for V_{SSH}.

■ AC ELECTRICAL CHARACTERISTICS

● Display Data Input/Output Timing



$V_{IH} = 0.2 \times V_{SS}$

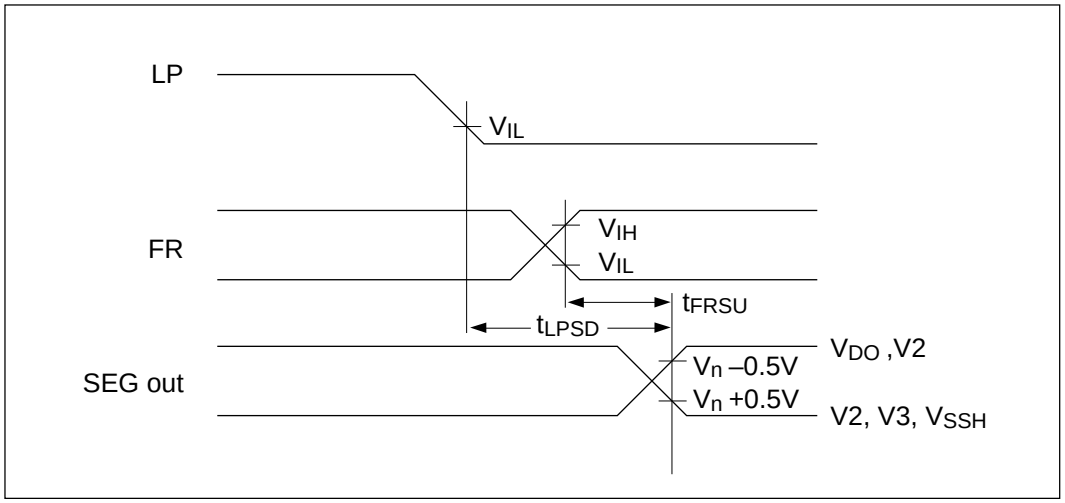
$V_{IL} = 0.8 \times V_{SS}$

- **AC Electrical Characteristics**

V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Shift clock cycle time	t_{CLC}		166	—	—	ns
Shift clock “H” width	t_{WCLH}		63	—	—	ns
Shift clock “L” width	t_{WCLL}		63	—	—	ns
Data setup time	t_{DS}		50	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
Latch pulse “H” time	t_{WLPH}		110	—	—	ns
Latch pulse “L” time	t_{WLPL}		220	—	—	ns
Latch hold time	t_{LT}		100	—	—	ns
XSCL to LP fall time	t_{LH}		0	—	—	ns
Permissible frame signal delay	t_{DFR}		–500	0	500	ns
Input signal rise time	t_r		—	—	—	ns
Input signal fall time	t_f		—	—	—	—
Data output delay time	t_{pD}		20	—	150	—

- **Segment Drive Output Timing**



V_{IH} = 0.2V_{SS}; VIL = 0.8V_{SS}; Vn: V_{DD}, V2, V3, V_{SSH}; (V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
LP-SEG output delay time	t_{LPSD}	V_{SSH}=–3.0 to –12.0 V,	—	—	4.5	µs
FR-SEG output delay time	t_{FRSD}	C_L= 100 pF	—	—	4.5	µs

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