SED1234/35 Series
LCD Controller/Drivers

Technical Manual

Contents

SED1234/35 Series

OVERVIEW

The SED1234, 1235 Series is a dot matrix LCD controller driver for character display, and can display a maximum of 48 characters, 4 user-defined characters, and a maximum of 48 symbols by means of 4-bit, 8-bit or serial data sent from a microcomputer.

A built-in character generator ROM is prepared for 256 character types, and each character font consists of 5×7 dots. A user-defined character RAM for four characters of 5×7 dots are incorporated, and a symbol register is also incorporated. With these, it is possible to apply this Series to display with a high degree of freedom. This Series can operate handy units with a minimum power consumption by means of its low power consumption and sleep mode.

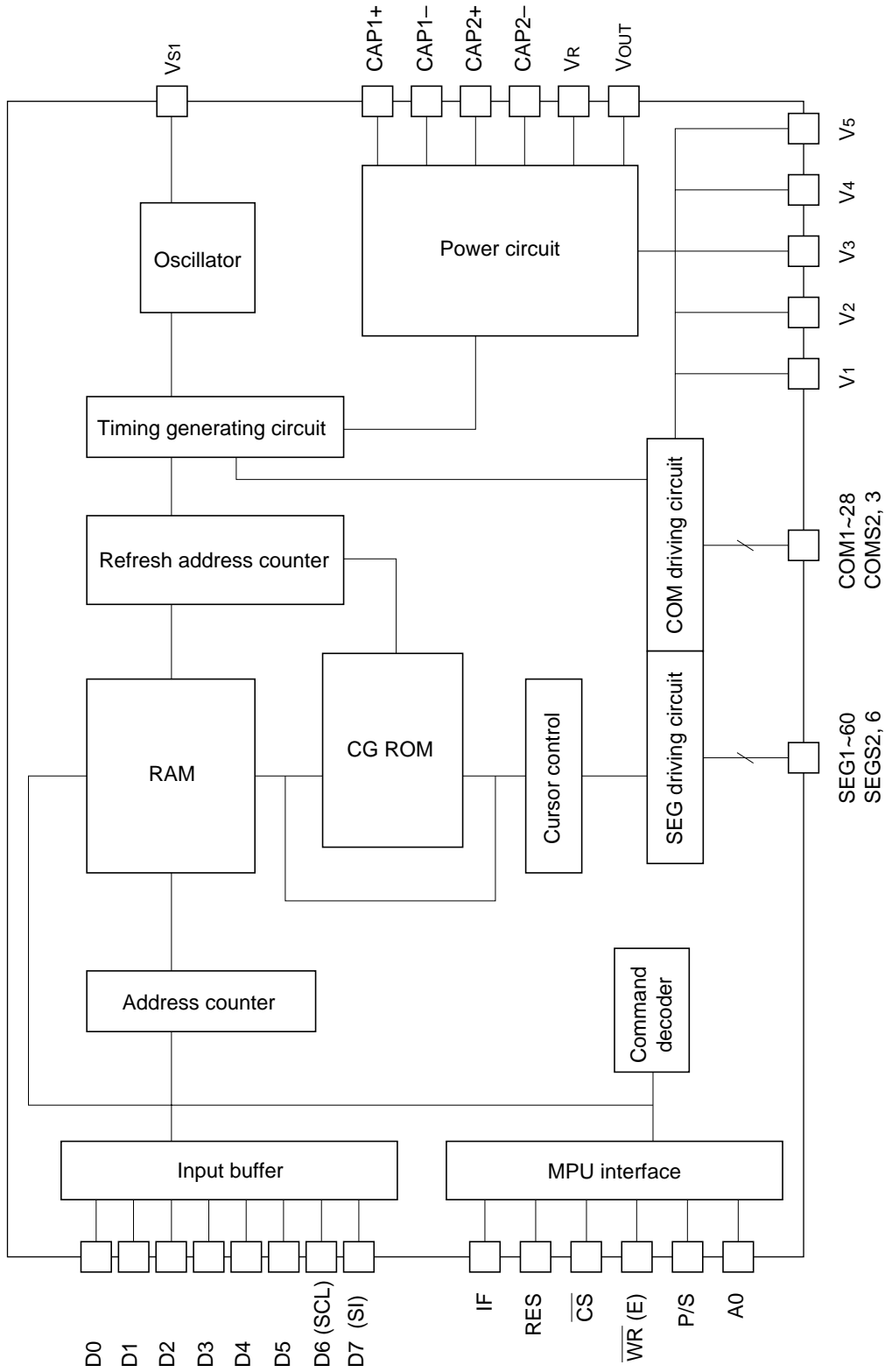SED1234, and 1235 depending on the duty of use and the number of display columns.

FEATURES

- Built-in diplay RAM
  48 characters + 4 user-defined characters + 48 symbols
- CG ROM (for up to 256 characters), CG RAM (4 characters), and symbol register (48 symbols)
- Number of display columns × number of lines
  (12 columns + 2 segment for signal) × 4 lines + 48 symbols: SED1234
  (12 columns + 2 segment for signal) × 2 lines + 48 symbols: SED1235
- CR oscillation circuit (on-chip C and R)

- High-speed MPU interface
  Interfacing with both 68 series and 80 series MPU
  Interfacing in 4 bits/8 bits
- Serial interface
- Character font 5×7 dots
- Duty ratio   1/16 (SED1235)
          1/30 (SED1234)
- Simple command setting
- Built-in liquid crystal driving power circuit
  Power boosting circuit, power regulating circuit, voltage follower × 4
- Built-in electronic volume function
- Low power consumption
  100 µA Max.   (In normal operation mode: Including the operating current of the built-in power supply)
- Power supply
  V_{DD} - V_{SS} (logic section): –2.4 V to –3.6 V
  V_{DD} - V_5 (liquid crystal drive section)
          : –5.0 V to –8.0 V
- Wide operating temperature range
  Ta = -30 to 85°C
- CMOS process
          (Pad   Pitch)
- COB assemble   126 µm   min.
- Delivery form: Chip SED123✶D✶A, SED123✶D✶C, SED123✶D✶F
- This IC is not designed with a protection against radioactive rays.

SED1230 Series (SED1234, SED1235) Chip Specifications

Product name	Duty	No. of digits indicated	No. of lines indicated	Font	V_{REG} temperature slope	Chip thickness	Form at delivery
SED1234D$_{BA}$	1/30	12 columns + 2 segment for signal	4 lines	Table 6 SED123✶D$_{B*}$	–0.17%/°C	625µm	AL-PAD chip
SED1235D$_{AA}$	1/16	12 columns + 2 segment for signal	2 lines	Table 5 SED123✶D$_{A*}$	–0.17%/°C	625µm	AL-PAD chip
SED1235D$_{AB}$	1/16	12 columns + 2 segment for signal	2 lines	Table 6 SED123✶D$_{B*}$	–0.17%/°C	625µm	AL-PAD chip
SED1235D$_{GA}$	1/16	12 columns + 2 segment for signal	2 lines	Table 7 SED123✶D$_{G*}$	–0.17%/°C	625µm	AL-PAD chip
SED1235D$_{2C}$	1/16	12 columns + 2 segment for signal	2 lines	Table 7 SED123✶D$_{G*}$	External Input	525µm	AL-PAD chip

BLOCK DIAGRAM

CHIP SPECIFICATION

SED1234D∗∗   1/30 duty
SED1235D∗∗   1/16 duty
          ↑
          #1 Column for CG ROM pattern change

Chip size: 10.23×3.11 mm
Pad pitch: 126 μm (Min.)
Chip thickness: 625 ± 25 μm (SED123∗D∗A)
                   525 ± 25 μm (SED123∗D∗C)

1) A1 pad specification
          Pad size: A 91 μm $\times$ 90 μm
                      B 114 μm $\times$ 114 μm

<SED1234D∗∗> (1/2)

Unit: μm

PAD		COORDINATES		PAD		COORDINATES	
No.	Name	X	Y	No.	Name	X	Y
1	V_{DD}	−4077	−1371	55	SEG15	2106	1406
2	V_{SSL}	−3526		56	SEG16	1979	
3	V_5	−2975		57	SEG17	1852	
4	V_4	−2424		58	SEG18	1725	
5	V_3	−1855		59	SEG19	1598	
6	V_2	−1287		60	SEG20	1471	
7	V_1	−719		61	SEG21	1345	
8	V_0	−151		62	SEG22	1218	
9	V_R	400		63	SEG23	1091	
10	V_{OUT}	968		64	SEG24	964	
11	CAP2−	1519		65	SEG25	837	
12	CAP2+	2070		66	SEG26	710	
13	CAP1−	2638		67	SEG27	584	
14	CAP1+	3189		68	SEG28	457	
15	V_{SSR}	3757		69	SEG29	330	
16	V_{DD}	4308		70	SEG30	203	
17	(NC)	4883		71	SEG31	76	
18	(NC)	4883		72	SEG32	−51	
19	(NC)	4883		73	SEG33	−177	
20	(NC)	4883		74	SEG34	−304	
21	V_{S1}	4929		75	SEG35	−431	
22	P/S	4924		76	SEG36	−558	
23	IF	4924		77	SEG37	−685	
24	RES	4924		78	SEG38	−812	
25	COMS2	4950		79	SEG39	−938	
26	COM1	4950		80	SEG40	−1065	
27	COM2	4950		81	SEG41	−1192	
28	COM3	4950		82	SEG42	−1319	
29	COM4	4950		83	SEG43	−1446	
30	COM5	4950		84	SEG44	−1572	
31	COM6	4950		85	SEG45	−1699	
32	COM7	4950		86	SEG46	−1826	
33	COM8	4896		87	SEG47	−1953	
34	COM9	4769		88	SEG48	−2080	
35	COM10	4642		89	SEG49	−2207	
36	COM11	4515		90	SEG50	−2333	
37	COM12	4388		91	SEG51	−2460	
38	COM13	4262		92	SEG52	−2587	
39	COM14	4135		93	SEG53	−2714	
40	SEGS2	4008		94	SEG54	−2841	
41	SEG1	3881		95	SEG55	−2968	
42	SEG2	3754		96	SEG56	−3094	
43	SEG3	3627		97	SEG57	−3221	
44	SEG4	3501		98	SEG58	−3348	
45	SEG5	3374		99	SEG59	−3475	
46	SEG6	3247		100	SEG60	−3602	
47	SEG7	3120		101	SEGS6	−3729	
48	SEG8	2993		102	COM28	−3855	
49	SEG9	2866		103	COM27	−3982	
50	SEG10	2740		104	COM26	−4109	
51	SEG11	2613		105	COM25	−4236	
52	SEG12	2486		106	COM24	−4363	
53	SEG13	2359		107	COM23	−4679	1405
54	SEG14	2232		108	COM22	−4806	1405

<SED1234D∗∗> (2/2)

PAD		COORDINATES	
No.	**Name**	**X**	**Y**
109	COM21	−4933	1405
110	COM20	−4964	1094
111	COM19		966
112	COM18		839
113	COM17		712
114	COM16		584
115	COM15		457
116	COMS3		330
117	A0		202
118	WR		75
119	CS		−52
120	D7		−180
121	D6		−307
122	D5		−434
123	D4		−562
124	D3		−689
125	D2		−816
126	D1		−943
127	D0		−1071

Note 1 : Set the pin (NC) to the floating state.
  2 : Be sure to connect the pins V_{SSL} and V_{SSR}
      outside.   They are called V_{SS} in the
      following text descriptions.

<SED1235D∗∗> (1/2)

Unit: μm

PAD		COORDINATES		PAD		COORDINATES	
No.	Name	X	Y	No.	Name	X	Y
1	VDD	−4077	−1371	55	SEG15	2106	−1406
2	VSSL	−3526		56	SEG16	1979	
3	V5	−2975		57	SEG17	1852	
4	V4	−2424		58	SEG18	1725	
5	V3	−1855		59	SEG19	1598	
6	V2	−1287		60	SEG20	1471	
7	V1	−719		61	SEG21	1345	
8	V0	−151		62	SEG22	1218	
9	VR	400		63	SEG23	1091	
10	VOUT	968		64	SEG24	964	
11	CAP2−	1519		65	SEG25	837	
12	CAP2+	2070		66	SEG26	710	
13	CAP1−	2638		67	SEG27	584	
14	CAP1+	3189		68	SEG28	457	
15	VSSR	3757		69	SEG29	330	
16	VDD	4308	↓	70	SEG30	203	
17	(NC)	4883	−1343	71	SEG31	76	
18	(NC)	4883	−1233	72	SEG32	−51	
19	(NC)	4883	−1123	73	SEG33	−177	
20	(NC)	4883	−1013	74	SEG34	−304	
21	VS1	4929	−903	75	SEG35	−431	
22	P/S	4924	−184	76	SEG36	−558	
23	IF	4924	−57	77	SEG37	−685	
24	RES	4924	70	78	SEG38	−812	
25	COMS2	4950	255	79	SEG39	−938	
26	COM1	4950	382	80	SEG40	−1065	
27	COM2	4950	510	81	SEG41	−1192	
28	COM3	4950	637	82	SEG42	−1319	
29	COM4	4950	764	83	SEG43	−1446	
30	COM5	4950	891	84	SEG44	−1572	
31	COM6	4950	1019	85	SEG45	−1699	
32	COM7	4950	1146	86	SEG46	−1826	
33	COM8	4896	1406	87	SEG47	−1953	
34	COM9	4769		88	SEG48	−2080	
35	COM10	4642		89	SEG49	−2207	
36	COM11	4515		90	SEG50	−2333	
37	COM12	4388		91	SEG51	−2460	
38	COM13	4262		92	SEG52	−2587	
39	COM14	4135		93	SEG53	−2714	
40	SEGS2	4008		94	SEG54	−2841	
41	SEG1	3881		95	SEG55	−2968	
42	SEG2	3754		96	SEG56	−3094	
43	SEG3	3627		97	SEG57	−3221	
44	SEG4	3501		98	SEG58	−3348	
45	SEG5	3374		99	SEG59	−3475	
46	SEG6	3247		100	SEG60	−3602	
47	SEG7	3120		101	SEGS6	−3729	
48	SEG8	2993		102	(NC)	−3855	
49	SEG9	2866		103	(NC)	−3982	
50	SEG10	2740		104	(NC)	−4109	
51	SEG11	2613		105	(NC)	−4236	
52	SEG12	2486		106	(NC)	−4363	↓
53	SEG13	2359		107	(NC)	−4679	1405
54	SEG14	2232	↓	108	(NC)	−4806	1405

EPSON

<SED1235D∗∗> (2/2)

PAD		COORDINATES	
No.	**Name**	**X**	**Y**
109	COM14	−4933	1405
110	COM13	−4964	1094
111	COM12		966
112	COM11		839
113	COM10		712
114	COM9		584
115	COM8		457
116	COMS3		330
117	A0		202
118	WR		75
119	CS		−52
120	D7		−180
121	D6		−307
122	D5		−434
123	D4		−562
124	D3		−689
125	D2		−816
126	D1		−943
127	D0		−1071

Note 1 : Set the pin (NC) to the floating state.
2 : Be sure to connect the pins VSSL and VSSR
outside.   They are called VSS in the
following text descriptions.

DESCRIPTION OF PINS

Power Pins

Pin name	I/O	Description	Q'ty
V_{DD}	Power supply	Logic + power pin. Also used as MPU power pin V_{CC}.	2
V_{SS}	Power supply	Logic – power pin. Connected to the system GND.	2
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined in the liquid crystal cell is resistance-divided or impedance-converted by operational amplifier, and the resultant voltage is applied. The potential is determined on the basis of V_{DD} and the following equation must be respected. $$V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5, V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$$ When the built-in power supply is ON, the following voltages are given to pins V_1 to V_4 by built-in power circuit: $V_1 = 1/5\ V_5$ $V_2 = 2/5\ V_5$ $V_3 = 3/5\ V_5$ $V_4 = 4/5\ V_5$	6
V_{S1}	O	Power supply voltage output pin for oscillating circuit. Don't connect this pin to an external load.	1

LCD Power Circuit Pins

Pin name	I/O	Description	Q'ty
CAP1+	O	Capacitor positive side connecting pin for boosting. This pin connects the capacitor with pin CAP1–.	1
CAP1–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP+.	1
CAP2+	O	Capacitor positive side connecting pin for boosting. This pin connects a capacitor with pin CAP2–.	1
CAP2–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP2+.	1
V_{OUT}	O	Output pin for boosting. This pin connects a smoothing capacitor with VSS pin.	1
V_R	I	Voltage regulating pin. This pin gives a voltage between V_{DD} and V_5 by resistance-division of voltage.	1

Pins for System Bus Connection

Pin name	I/O	Description	Q'ty
D7 (SI) D6 (SCL) D5 ~ D0	I	8-bit input data bus. These pins are connected to a 8-bit or 16-bit standard MPU data bus. When P/S = "Low", the D7 and D6 pins are operated as a serial data input and a serial clock input respectively. | P/S	D7	D6	D5 ~ D0	$\overline{CS}$	A0
---	---	---	---	---	---
"Low"	SI	SCL	—	$\overline{CS}$	A0
"High"	D7	D6	D5 ~ D0	$\overline{CS}$	A0	 When P/S = "Low," be sure to fix D5 to D0 to "High" or "Low."	8
A0	I	Usually, this pin connects the least significant bit of the MPU address bus and identifies a data command. 　0 : Indicates that D0 to D7 are a command. 　1 : Indicates that D0 to D7 are display data.	1
RES	I	In case of a 68 series MPU, initialization can be performed by changing RES ⌐↓. In case of an 80 series MPU, initialization can be performed by changing ∟↑. A reset operation is performed by edge sensing of the RES signal. An interface type for the 68/80 series MPU is selected by input level after initialization. 　"L" : 80 series MPU interface 　"H" : 68 series MPU interface	1
$\overline{CS}$	I	Chip select signal. Usually, this pin inputs the signal obtained by decoding an address bus signal. At the "Low" level, this pin is enabled.	1
$\overline{WR}$ (E)	I	<When connecting an 80 series MPU> 　Active "Low". This pin connects the $\overline{WR}$ signal of the 80 series 　MPU. The signal on the data bus is fetched at the rise of the $\overline{WR}$ 　signal. When P/S = "Low," be sure to fix the $\overline{WR}$ signal to "High" or "Low." <When connecting a 68 series MPU> 　Active "High". This pin becomes an enable clock input of the 68 　series MPU.	1
P/S	I	This pin switches between serial data input and parallel data input. 	P/S	Chip Select	Data/Command	Data	Serial Clock
---	---	---	---	---
"High"	$\overline{CS}$	A0	D0~D7	–
"Low"	$\overline{CS}$	A0	SI	SCL		1
IF	I	Interface data length select pin for parallel data input. 　"High": 8-bit parallel input 　"Low": 4-bit parallel input When P/S = "Low", connect this pin to V_{DD} or V_{SS}.	1

Liquid Crystal Drive Circuit Signals

SED1234

Pin name	I/O	Description	Q'ty
COM1~ COM28	O	Common signal output pin (for characters)	28
COMS2, CMOS3	O	Common signal output pin (except for characters) CMOS2, CMOS3: Common output for symbol display	2
SEG1~ SEG60	O	Segment signal output pin (for characters)	60
SEGS2, SEGS6	O	Segment signal output pin (except for characters) SEGS2, SEGS6: Segment output for signal output	2

SED1235

Pin name	I/O	Description	Q'ty
COM1~ COM14	O	Common signal output pin (for characters) COM8~COM14:W output	14 (21)
COMS2, CMOS3	O	Common signal output pin (except for characters) CMOS2, CMOS3: Common output for symbol display	2
SEG2~ SEG60	O	Segment signal output pin (for characters)	60
SEGS2, SEGS6	O	Segment signal output pin (except for characters) SEGS2, SEGS6: Segment output for signal output	2

FUNCTIONAL DESCRIPTION

MPU Interface

Selection of interface type

In the SED1234, SED1235, data transfer is performed through a 8-bit or 4-bit data bus or a serial data input (SI). By selecting "High" or "Low" as P/S pin polarity, a parallel data input or a serial data input can be selected as shown in Table 1.

Table 1

P/S	Type	$\overline{CS}$	A0	$\overline{WR}$	SI	SCL	D0~D7
"High"	Parallel Input	$\overline{CS}$	A0	$\overline{WR}$	—	—	D0~D7
"Low"	Serial Input	$\overline{CS}$	A0	—	SI	SCL	—

Parallel Input

In the SED1234, SED1235, when parallel input is selected (P/S = "High"), it can be directly connected to the 80 series MPU bus or 68 series MPU bus, as shown in Table 2, if either "High" or "Low" is selected as RES pin polarity after a reset input, because the RES pin has an MPU select function.

Selection between 8 bits and 4 bits is performed by command.

Table 2

RES input polarity	Type	A0	$\overline{WR}$	$\overline{CS}$	D0~D7
High-to-low active	68 series	A0	E	$\overline{CS}$	D0~D7
Low-to-high active	80 series	A0	$\overline{WR}$	$\overline{CS}$	D0~D7

Interface with 4-bit MPU interface

When data transfer is performed by 4-bit interface (IF = 0), an 8-bit command, data and address are divided into two parts.
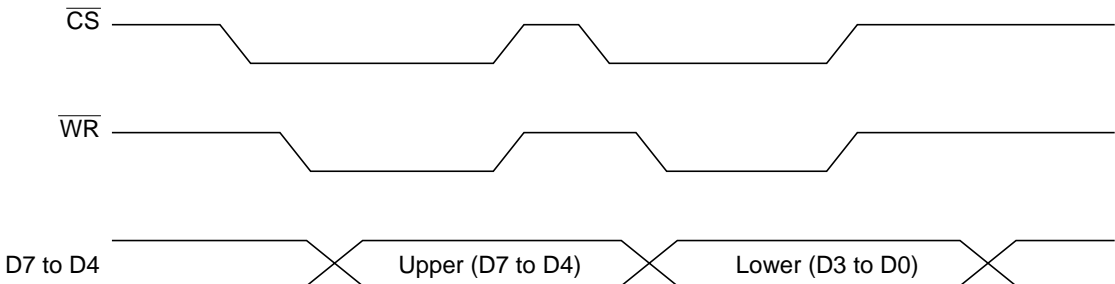
Note: When performing writing in succession, reverse a time exceeding the system cycle time (t_{cyc}) and then perform writing.

Serial interface (P/S = "Low")

The serial interface consists of a 8-bit shift register and a 3-bit counter and acceptance of an SI input or SCL input is enabled in the ship selected status (CS = "Low").

When no chip is selected, the shift register and counter are reset to the initial status.

Serial data is input in the order of D7, D6 .... D0 from the serial data input pin (SI) at the rise of Serial Clock (SCL). At the rising edge of the 8th serial clock, the serial data is converted into 8-bit parallel data and this data is processed. The A0 input is used to identify whether the serial data input (SI) is display data or a command. That is, when A0 = "High", it is regarded as display data. When A0 = "Low", it is regarded as a command.

The A0 input is read in and identified at the rise of the 8 x n-th clock of Serial Clock (SCL) after chip selection.

Fig. 1 shows a timing chart of the serial interface.

Regarding the SCL signal, special care must be exercised about terminal reflection and external noise due to a wire length. We recommend the user to perform an operation check with a real machine.

We also recommend the user to periodically refresh the write status of each command to prevent a malfunction due to noise.
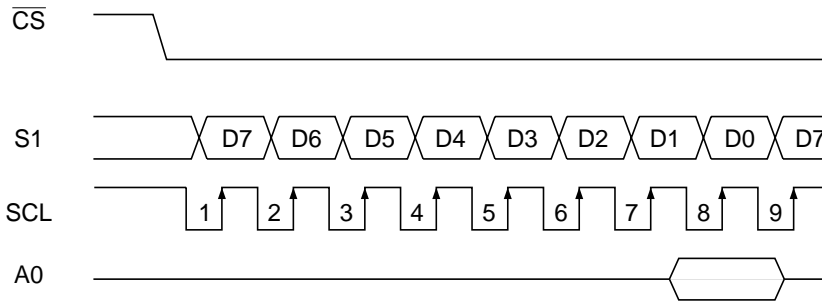
Fig. 1

Identification of data bus signals

The SED1234, SED1235 series identifies data bus signals, as shown in Table 3, by combinations of A0 and $\overline{\text{WR}}$ (E).

Table 3

Common	68 series	80 series	Function
A0	E	$\overline{\text{WR}}$	
1	1	0	Writing to RAM and symbol register
0	1	0	Writing to internal register (command)

Chip select

The SED1234, SED1235 series has a chip select pin ($\overline{\text{CS}}$). Only when $\overline{\text{CS}}$ = "Low", MPU interfacing is enabled. In any status other than Chip Select, D0 to D7 and A0, WR, SI and SCL inputs are invalidated. When a serial input interface is selected, the shift register and counter are reset.

However, the Reset signal is input regardless of the $\overline{\text{CS}}$ status.

Power Circuit

This is a low-power-consumption power circuit that generates a voltage required for liquid crystal drive.
The power circuit consists of a boosting circuit, voltage regulating circuit and voltage follower.

The power circuit incorporated in the SED1234, SED1235 Series is set for a small-scale liquid crystal panel, so that its display quality may be greatly deteriorated if it is used for a liquid crystal panel with a large display capacity.
In this case, an external power supply must be used.

A power circuit function can be selected by power control command. With this, an external power supply and a part of the internal power supply can be used together.

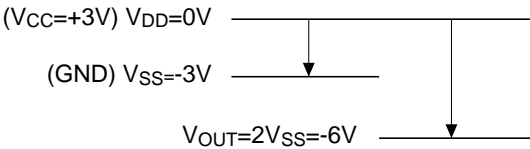|	Boosting circuit	Voltage regulating circuit	Voltage follower	External voltage input	Boosting system pin
	○	○	○	—	
Note 1	×	○	○	V_{OUT}	OPEN
Note 2	×	×	○	$V_5 = V_{OUT}$	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

Note 1: When the boosting circuit is turned off, make boosting system pins (CAP1+, CAP1-, CAP2+, CAP2-) open and give a liquid crystal drive voltage to the V_{OUT} pin from the outside.

Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, make the boosting system pins open, connect between the V_5 pin and V_{OUT} pin, and give a liquid crystal drive voltage from the outside.

Note 3: When all the internal power supplies are turned off, supply liquid crystal drive voltages V_1, V_2, V_3, V_4 and V_5 from the outside, and make the CAP1+, CAP1-, CAP2+, CAP2- and V_{OUT} pins open.

Triple boosting circuit

When a capacitor is connected between CAP1+ and CAP1-, between CAP2+ and CAP2-, and between VSS pin and VOUT pin respectively, the potential between the VDD pin and VSS pin is boosted triple and output to the VOUT pin. In case of double boosting, remove the capacitor between CAP2+ and CAP2- in connection for triple boosting operation and strap between CAP2- and

VOUT pin. Then, a double boosted output can be obtained from the VOUT pin (CAP2-).

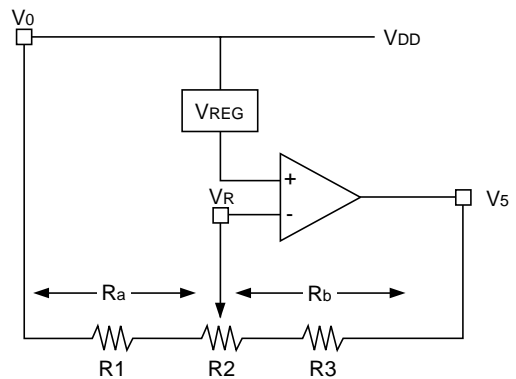The boosting circuit uses a signal from the oscillator ourput.

Accordingly, it is necessary that the oscillating circuit must be in operation. The potential relationship of boosting is shown below.

Potential during double boosting
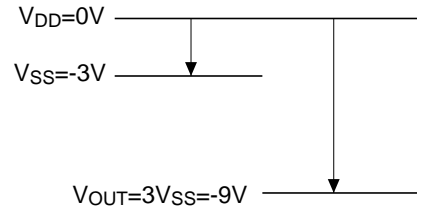
Potential during triple boosting

Voltage regulating circuit

The voltage regulation circuit regulates the boosted voltage developed at Vout. It outputs the regulated LCD driving voltage at the V5 terminal. An internal resistor can be inserted into the regulation circuit feedback loop providing the following voltage levels at the V5 terminal.

When V5 is required to be different than the above case, leave the internal feedback resistor out of the circuit. V5 can be regulated within a range of $|V5| < |VOUT|$. It may be calculated by the following formula:

$$V5 = (1 + \frac{Rb}{Ra}) \cdot VREG \ \text{..............................} ①$$

Wherein, VREG is the constant voltage source inside the SED1230 Series and the voltage is constant at VREG ≒ 3.1V. Voltage regulation of the V5 output is accomplished by connecting a variable resistor between VR, VDD and V5. For fine adjustment of the V5 voltage, use a combination of fixed resistors R1 and R3 and a variable resistor R2.

The voltage regulator circuit carries a temperature gradient of about -0.17%/°C under VREG outputs. When any other temperature gradient is required, connect a thermistor in series to the output voltage regulating register.

Since the VR terminal has a high input impedance, it is necessary to take noise suppression measures such as shortening the input wiring and shielding the wiring run.

Example 1:
   Condition: I(R1, R2, R3) ≤ 5μA   V5 = –6 to –8V

Setting: R1+R2+R3 = 8V/5μA = 1.6MΩ   R1 = 600KΩ
            8V = (1+Rb/Ra) 3.0V Rb/Ra = 1.67 ⟩ .... R2 = 200KΩ
            6V = (1+Rb/Ra) 3.0V Rb/Ra = 1   R3 = 800KΩ

● Voltage Regulation Circuit Using Electronic Contrast Control Register

The contrast control register controls the liquid crystal driving voltage (V5). This is accomplished by an electronic volume control register set command that adjusts the contrast of the liquid crystal display (see section 1-22).

The commands provide 4-bits of voltage level data to the electronic volume control register. This provides for the selection of 16 different voltage levels for the liquid crystal driving voltage. When using the electronic volume control function, it is necessary to close the voltage regulation circuit using electronic control commands. For reference information, when the electronic volume control registor value is at $(1, 1, 1, 1)$, the constant current value becomes: $I_{REF} \fallingdotseq 3.65\mu A$.

[An exemplary constant setting when the electronic volume control function is being used]

$$V_5 = (1 + \frac{R_b}{R_c}) \bullet V_{REG} \cdots\cdots\cdots\cdots\cdots ②$$

$$R_c = \frac{R_a \times R_I}{R_a + R_I}$$
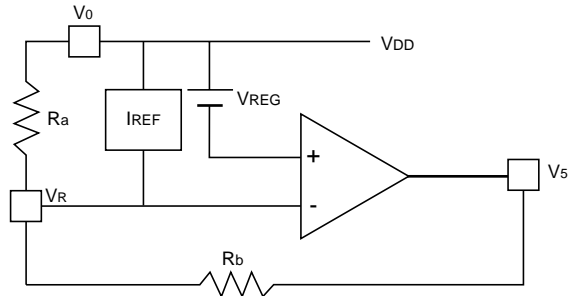
$$R_I = \frac{V_R}{I_{REF}}$$

Fig. 9

(1) Determining the V5 voltage setting range by the electronic volume control
     Liquid crystal driving voltage V5: max. -6v ~ min. -8V
     V5 variable voltage range: 2V

(2) Determinig the Rb
     R_b = V5 variable voltage range/ I_{REF}
        = $2V/3.65\mu A$
        = $548K\Omega$

(3) Determining the Ra
     $$R_a = \frac{V_{REG}}{(V5 \text{ voltage setting max} - V_{REG}) / R_b} \quad \text{(Use absolute values for } V_{REG} \text{ and V5 voltage settings.)}$$

     $$= \frac{3.1V}{(6V - 3.1V) / 548K\Omega}$$

     $$= 585K\Omega$$

(4) Regulating the Ra
     Set the electronic volume control register to $(D3, D2, D1, D0) = (1, 0, 0, 0)$ or $(0, 1, 1, 1)$ before matching the Ra value to the optimum contrast.

     Since I_{REF} is a simplified constant voltage source, fluctuations upto $\pm 40\%$ must be taken into consideration, as a dispersion range during manufacture. Meanwhile, the temperature dependency of I_{REF} is : $\Delta I_{REF} \fallingdotseq -0.037\mu A/°C$. Determine the Ra and Rb for the using LCD panel in consideration of the above dispersion and the variation by the temperature.

     When using the electronic volume control function, in order to compensate the V5 voltage for dispersion of V_{REG} and I_{REF}, use a variable registor as Ra and perform optimum contrast adjustment according to the above item (4) with each IC chip.

     When the electronic volume control function is not being used, set the electronic volume control register to $(0, 0, 0, 0)$ using the RES signal or the electronic volume control register setting command.

Liquid crystal voltage generating circuit

The V_5 potential is resistance-divided inside the IC so that V_1, V_2, V_3 and V_4 potentials are generated for liquid crystal drive.

Furthermore, the V_1, V_2, V_3 and V_4 are impedance-converted by voltage follower and the then supplied to the liquid crystal drive circuit.
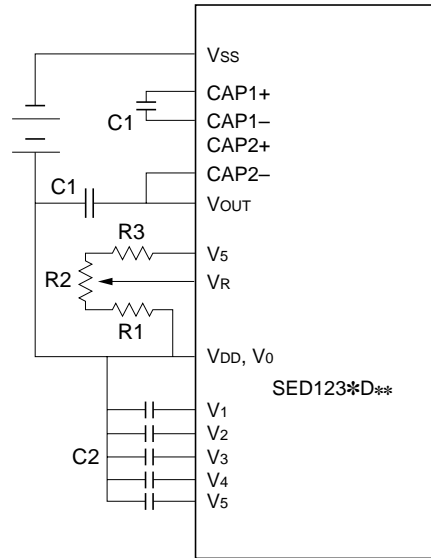
The liquid crystal drive voltage is fixed to 1/5 bias.

As shown in the diagrams below, the capacitor (C2) for voltage stabilization must be externally connected to the V_1 to V_5 pins of liquid crystal power pins.
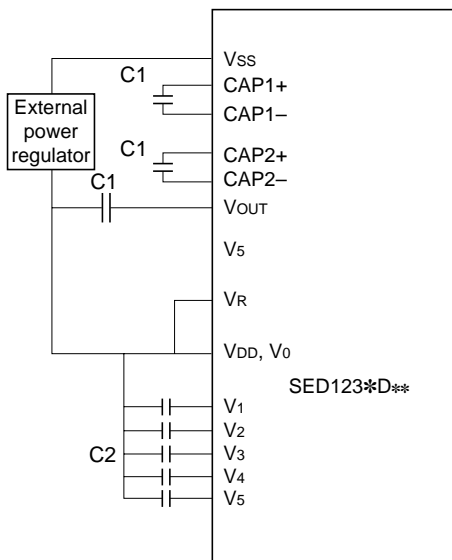
When a built-in power supply is used
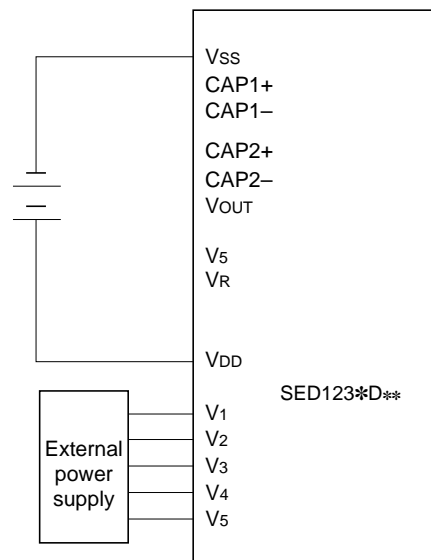Under a triple boosting
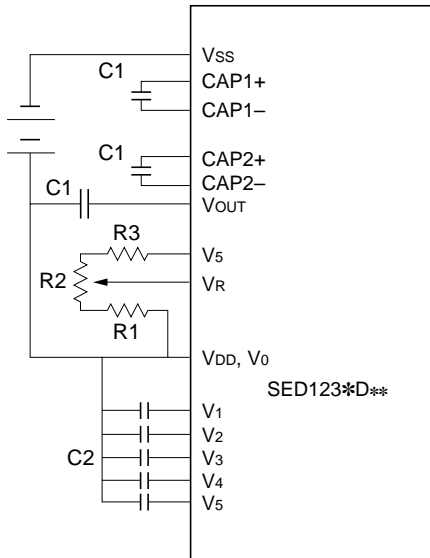
The diagram under a double boosting

When an external power regulator is used
(The built-in power regulator is not used)

When a built-in power supply is not used

Reference setting values: C1: 0.1 - 4.7 μF
C2: 0.1 μF

We recommend the user to set the optimum values to capacitors C1 and C2 according to the panel size watching the liquid crystal display and drive waveforms.

Low Power Consumption Mode

The SED1234, SED1235 Series is provided with the standby mode and sleep mode with the object of low power consumption when the unit is in the standby state.

● Sleep Mode

After the power circuit and oscillating circuit are turned off by command and the power save command is executed, the sleep mode is set. This mode permits reducing current consumption nearly to the static current value.

1. Liquid crystal display output
    COM1 ~ COM28, COMS2, COMS3 : V_{DD} level
    SEG1 ~ SEG60, SEGS2, SEGS6   : V_{DD} level
2. DD RAM, CG RAM and symbol register
    Written contents do not change and are stored regardless of whether the sleep mode is turned on or off.
3. In the operation mode, the status precedent to execution of the sleep mode is held. All the internal circuits stops.
4. Power circuit and oscillating circuit
    Turn off the built-in power supply and oscillating circuit by power save command and power control command.

Reset Circuit

When the RES input goes active, this LSI enters the initialization status.

1. Display ON/OFF control
    C   = 0 : Cursor OFF
    B   = 0 : Blink OFF
    DC = 0 : Double cursor OFF
    D   = 0 : Display OFF
2. Power save
    O   = 0 : Oscillating circuit OFF
    PS   = 0 : Power save OFF
3. Power control
    VC   = 0 : Voltage regulating circuit OFF
    VF   = 0 : Voltage follower OFF
    P   = 0 : Boosting circuit OFF
4. System set
    CG   = 0 : No use of CG RAM

As described in 6.1 MPU Interface, the RES pin is connected to the MPU reset pin and performs initialization concurrently with the MPU.

Regarding the reset signal, a pulse of at least 10 μs or more active level must be input as described in 9. DC Characteristics. Usually, the operation status is started in 1 μs from the edge of the RES signal.

In the SED 1230 Series where the built-in liquid crystal power circuit is not used, the RES input must be active when the external liquid crystal power supply is turned on.

COMMANDS

Table 4 shows a command list. In the SED1230 Series, each data bus signal is identified by a combination of A0 and $\overline{WR}$ (E).

Command interpretation and execution are performed by only internal timing. This permits high-speed processing.

• **Outline of Commands**

Command type	Command name	A0	WR
Display control instruction	Cursor Home	0	0
	Display ON/OFF Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
	Electronic Volume Register Set	0	0
Address control instruction	Address Set	0	0
Data input instruction	Data Write	1	0

The execution time of each instruction is determined by the internal processing time of the SED1230 Series. Accordingly, to execute instructions in succession, reserve a time exceeding the cycle time (t_{cyc}) and execute the next instruction.

• **Outline of Commands**

(1) Cursor Home
This command presets the address counter to 30H. When the cursor is displayed, this command moves it to column 1 of line 1.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	*	*	*	*

* : Don't Care

(2) Display ON/OFF Control
This command performs display and cursor setting.

Note: Control the symbols that are driven by COMS1 and SEGS1, by the Static Display Control command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	C	B	DC	D

D = 0 : Display OFF
   1 : Display ON

DC = 0 : Double cursor OFF
    1 : Double cursor ON

B = 0 : Cursor blink OFF
   1 : Cursor blink ON

In the blink state, display characters in normal video and display characters in monochrome reverse video are displayed alternately.
The repetition cycle of alternate display is about 1 second.

C = 0 : Non-display of cursor
   1 : Display of cursor

The relationship between C and B registers and cursor display is shown in the following table.

C	B	Cursor display
0	0	Non-display
0	1	Non-display
1	0	Display in monochrome reverse video
1	1	Alternate display of display characters in normal video and display characters in monochrome reverse video

The cursor display position corresponds to the position indicated by address counter.

Accordingly, to move the cursor, change the address counter value by the RAM Address Set command or auto increment by writing RAM data.

If the address counter is set at the symbol register position with (C, B) = (1, 0), symbols can be caused to blink selectively.

(3) Power Save
This command is used to control the oscillating circuit and set and reset sleep mode.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	*	*	O	PS

* : Don't Care

PS = 0 : Power save OFF (reset)
    1 : Power save ON (set)

O = 0 : Oscillating circuit OFF (stop of oscillation)
   1 : Oscillating circuit ON (oscillation)

(4) Power Control
This command is used to control the operation of the built-in power circuit.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	VC	VF	P

P　　　= 0　: Boosting circuit OFF
　　　　　1　: Boosting circuit ON

Note:　To operate the boosting circuit the oscillating circuit must be in operation.

VF　　= 0　: Voltage follower OFF
　　　　　1　: Voltage follower ON

VC　　= 0　: Voltage regulating circuit OFF
　　　　　1　: Voltage regulating circuit ON

(5) System Set
This command set the use or non-use of display lines and CG RAM.
Execute this command first after turning on the power supply or after resetting.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	N2	N1	*	PS

* : Don't Care

CG　　= 0　: Use of CG RAM
　　　　　1　: Non-use of CG RAM

N2	N1	
0	0	: 2 lines
0	1	: 3 lines
1	0	: 4 lines

(6) Electronic Volume Register Set
This command controls the liquid crystal driving voltage V_5 output from the voltage regulating circuit of the built-in liquid crystal power supply,

thereby adjusting the gradation of liquid crystal display.
When data is set in the 4-bit register, the liquid crystal driving voltage can take one of 16 voltage states.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	MSB	*	*	LSB

Hex Code
70H ~7FH

MSB	.	.	LSB	$\mid V_5 \mid$	$\mid I_{REF} \mid$
0	0	0	0	Small	0.0μA
		:		:	:
		. :		:	:
1	1	1	1	Large	3.65μA

When the electronic volume function is not used, set (A3, A2, A1, A0) = (0, 0, 0, 0).

(7) RAM Address Set
This command sets addresses to write data into the DD RAM, CG RAM and symbol register in the address counter.

When the cursor is displayed, the cursor is displayed at the display position corresponding to the DDRAM address set by this command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1				ADDRESS			

① The settable address length is ADDRESS = 00H to 7FH.
② Before writing data into the RAM, set the data write address by this command. Next, when data is written in succession, the address is automatically incremented.

RAM Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 H	C G R A M (0 0 H)							–	C G R A M (0 1 H)							–
1 0 H	C G R A M (0 2 H)							–	C G R A M (0 3 H)							–
2 0 H	Unused															
3 0 H	DDRAM line 1													Unused		
4 0 H	DDRAM line 2					For signals								"		
5 0 H	DDRAM line 3													"		
6 0 H	DDRAM line 4													"		
7 0 H	Symbol register													"		

　　　　–　　　　: Unused
For signals : Output from SEGS2 to SEGS6.

(8)   Data Write

A0	$\overline{\text{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0				DATA				

① This command writes data into the DD RAM, CG RAM or symbol register.

② After this command is executed, the address counter is automatically incremented by 1. This permits writing data in succession.

<Example of Data Writing>

The following is an example of writing one-line data into the DD RAM in succession.

RAM Address Set

Data Writing

NO   One Line Completed?

YES
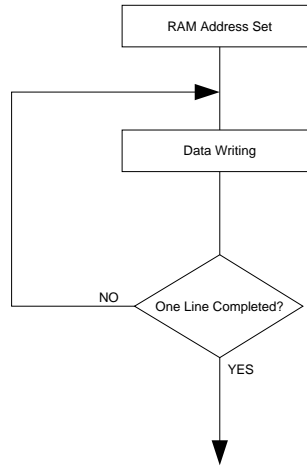
Note: When executing instructions in succession, reserve a time exceeding t_{CYC} and execute the next instruction.

Table 4 SED1234/SED1235 Command List

Command	Code										Function
	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Moves the cursor to the home position.
(2) Display ON/OFF Control	0	0	0	0	1	1	C	B	DC	D	Sets cursor ON/OFF (C), cursor blink ON//OFF (B), double cursor ON/OFF (DC) and display ON/OFF (D). C = 1 (cursor ON) 0 (cursor OFF), B = 1 (blink ON) 0 (blink OFF) DC = 1 (double cursor ON) 0 (double cursor OFF), D = 1 (display ON) D = 0 (display OFF)
(3) Power Save	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (0). PS = 1 (power save ON) 0 (power save OFF), 0 = 1 (oscillating circuit ON) 0 (oscillating circuit OFF)
(4) Power Control	0	0	0	1	0	1	0	VC	VF	P	Sets voltage regulating circuit ON/OFF and boosting circuit ON/OFF (P). VC = 1 (voltage regulating circuit ON) 0 (voltage regulating circuit OFF) VF = 1 (voltage follower ON) 0 (voltage follower OFF), P = 1 (boosting circuit ON) 0 (boosting circuit OFF)
(5) System Set	0	0	0	1	1	0	N2	N1	*	CG	Sets the use or non-use of CG RAM and display lines (N2, N1). CG = 1 (use of CG RAM) 0 (non-use of CG RAM), N2, N1 = 0, 0 (2 lines) 0, 1 (3 lines) 1, 0 (4 lines)
(6) Electronic Volume Register	0	0	0	1	1	1	MSB			LSB	Sets the electronic volume register value.
(7) RAM Address Set	0	0	1	ADDRESS							Sets the DD RAM, CG RAM or symbol register address.
(8) RAM Write	1	0	DATA								Writes data into the DD RAM, CG RAM or symbol register address.
(9) NOP	0	0	0	0	0	0	0	0	0	0	Non-operation command
(10) Test Mode	0	0	0	0	0	0	1	0	1	0	Command for IC chip test. Don't use this command.

EPSON

CHARACTER GENERATOR

Character Generator ROM (CG ROM)

The SED1234/1235 is provided with a character generator ROM consisting of a up to 256-type characters. Each character size is 5×7 dots.

Table 5 shows a character code table of the SED1230 Series.

The 4characters of character codes 00H to 03H are set by the System Set command to specify for which of CG ROM and CG RAM they are to be used.

The CG ROM of the SED1234/1235 is a mask ROM and compatible with the use-dedicated CG ROM. Please ask us for further information of it.

Regarding changed CG ROM, it is defined in product name as follows:

(Example) S E D 1 2 3 4 D 0 A
                              ↑
                        Digit for CG ROM
                        pattern change

SED1234/35
Series

SED123∗D∗   Table 5

Character code table showing 16×16 grid. Columns labeled "Lower 4 Bit of Code" (0-F), rows labeled "Higher 4 Bit of Cord" (0-F).

SED123∗DB∗

SED1234/35
Series

SED123∗DG∗

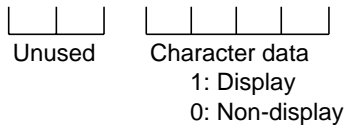**EPSON**

Character Generator RAM (CG RAM)

The SED1230 Series is provided with a CG RAM that permits user-programming character patterns so that they can be displayed with a high degree of freedom for signal display.

Before using the CG RAM, select the use of CG RAM by the System Set command.

The capacity of the CG RAM is 140 bits and arbitrary patterns of 4 types consisting of 5×7 dots can be registered.

The relationship among CG RAM patterns, CG RAM addresses, and character codes is shown below.

Character code	RAM address		CGRAM data (character pattern)								Display
			D7							D0	
00H	00H~06H	0	*	*	*	0	1	1	1	1	□■■■■
02H	10H~16H	1	*	*	*	1	0	0	0	0	■□□□□
		2	*	*	*	1	0	0	0	0	■□□□□
		3	*	*	*	0	1	1	1	1	□■■■■
		4	*	*	*	0	0	0	0	1	□□□□■
		5	*	*	*	0	0	0	0	1	□□□□■
		6	*	*	*	1	1	1	1	0	■■■■□
01H	08H~0EH	8	*	*	*	0	0	1	0	0	□□■□□
03H	18H~1EH	9	*	*	*	0	0	1	0	0	□□■□□
		A	*	*	*	0	1	1	1	0	□■■■□
		B	*	*	*	0	1	1	1	0	□■■■□
		C	*	*	*	0	1	1	1	0	□■■■□
		D	*	*	*	1	1	1	1	1	■■■■■
		E	*	*	*	1	1	1	1	1	■■■■■

Unused   Character data
                        1: Display
                        0: Non-display

Symbol Register

The SED1234, 1235 provided with a symbol register that permits displaying each symbol so that symbol display may be performed on the screen.
The capacity of the symbol register is 48 bits. In case of 48 symbols can be displayed.
The relationship among symbol register display patterns, RAM addresses and write data is shown below.
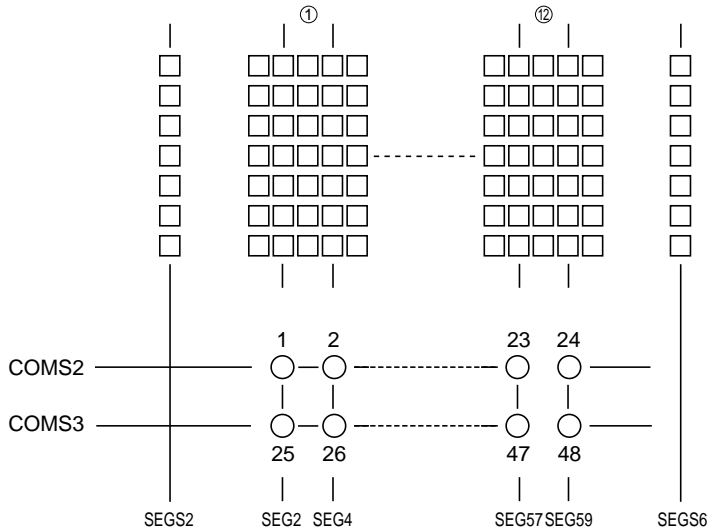
RAM address		Symbol Bits								Bit
		D7						D0		1: Display
70H~7BH	0	*	*	*	25	1	26	2	*	0: Not display
	1	*	*	*	27	3	28	4	*	
	:				:					
	B	*	*	*	47	23	48	24	*	

Notes: 1. We recommend to drive a symbol by dividing it into COMS2 and COMS3 separately if it is larger than other dots for 1.5 times or more.
2. Do not cross a segment (other than those used for symbol display) with COMS2 or COMS3. If segment crossing is required, set the symbol registers of COMS3 to all zeros (0s).

EPSON

ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Power supply voltage (1)		V_{SS}	$-6.0 \sim +0.3$	V
Power supply voltage (2)		V_5	$-16.0 \sim +0.3$	V
Power supply voltage (3)		V_1, V_2, V_3, V_4	$V_5 \sim +0.3$	V
Input voltage		V_{IN}	$V_{SS}-0.3 \sim +0.3$	V
Output voltage		V_O	$V_{SS}-0.3 \sim +0.3$	V
Operating temperature		T_{opr}	$-30 \sim +85$	°C
Storage temperature	TCP	T_{str}	$-55 \sim +100$	°C
	Bare chip		$-65 \sim +125$	

$(V_{CC})\ V_{DD}$ ——————————————— V_{DD}

$(GND)\ V_{SS}$ —————————

——————— V_5
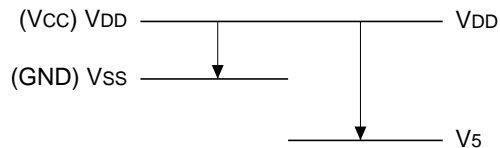
Notes: 1. All the voltage values are based on $V_{DD} = 0$ V.
2. For voltages of V_1, V_2, V_3 and V_4, keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ at all times.
3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction. In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

DC CHARACTERISTICS

V_{DD} = 0 V, V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified.

	Item	Symbol	Condition		min	typ	max	Unit	Applicable pin
Power supply voltage (1)	Recommended operation	V_{SS}			–3.6	–3.0	–2.4	V	V_{SS}
	Operable				–5.5	–3.0	–2.4		*1
Power supply voltage (2)	Recommended operation	V_5			–8.0		–5.0	V	V_5
	Operable				–11.0		–4.5		*2
	Operable	V_1, V_2			$0.6{\times}V_5$		V_{DD}	V	V_1, V_2
	Operable	V_3, V_4			V_{DD}		$0.4{\times}V_5$	V	V_3, V_4
High-level input voltage		V_{IHC}			$0.2{\times}V_{SS}$		V_{DD}	V	*3
Low-level input voltage		V_{ILC}			V_{SS}		$0.8{\times}V_{SS}$	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS} –1.0				1.0	µA	*3
LC driver ON resistance		R_{ON}	Ta=25°C V_5=–7.0V ΔV=0.1V			20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}				0.1	5.0	µA	V_{DD}
Dynamic current consumption		I_{DD}	Display state	V_5 = –7 V without load			100	µA	V_{DD} *5
			Standby state	Oscillation ON, Power OFF			20	µA	V_{DD} *6
			Sleep state	Oscillation OFF, Power OFF			5	µA	V_{DD}
			Access state	f_{cyc}=200KHz			500	µA	V_{DD} *7
Frame frequency		f_{FR}	Ta=25°C V_{SS}=–3.0V		70	100	130	Hz	*11
Input pin capacity		C_{IN}	Ta=25°C f=1MHz			5.0	8.0	pF	*3
Reset time		t_R			1.0			µs	*8
Reset pulse width		t_{RW}			10			µs	*9
Reset start time		t_{RES}			50			ns	*9
Built-in power supply	Input voltage	V_{SS}			–3.6		–2.4	V	*10
	Booster output voltage	V_{OUT}	Double boosting state		–7.2			V	V_{OUT}
			Triple boosting state		–10.8				
	Voltage follower operating voltage	V_5			–11.0		–4.5	V	
	Reference voltage (standard)	V_{REG}	Ta = 25°C		–3.5	–3.1	–2.7	V	*12
	Reference voltage (option)	$V_{REG(VS1)}$	Ta = 25°C		–2.4	–2.1	–1.8	V	*12

*1: A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

*2: The operating voltage range is applicable to the case where an external power supply is used.

*3: D0 ~ D5, D6 (SCL), D7 (SI), A0, RES, $\overline{CS}$ $\overline{WR}$ (E), P/S, IF

*4: This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V_1, V_2, V_3 or V_4). It is specified in the range of operating voltage (2).

R_{ON} = 0.1 V / ΔI

(ΔI: Current flowing when 0.1 V is applied between the power and output)

*5: Character "▦" display. This is applicable to the case where no access is made from the MPU and the built-in power circuit and oscillating circuit are in operation.

*6: This is applicable to the case where the built-in power circuit is OFF and the oscillating circuit is in operation in the standby mode.

*7: Current consumption when data is always written by f_{cyc}.
The current consumption in the access state is almost proportional to the access frequency (f_{cyc}).
When no access is made, only I_{DD} (I) occurs.

*8: t_R (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the SED123✱ usually enters the operating state after t_R.

*9: Specifies the minimum pulse width of the RES signal. It is reset when a signal having the pulse width greater than t_{RW} is entered.

*10: When operating the boosting circuit, the power supply V_{SS} must be used within the input voltage range.

*11: The f_{OSC} frequency of the oscillator circuit for internal circuit drive may differ from the f_{BST} boosting clock on some models. The following provides the relationship between the f_{OSC} frequency, f_{BST} boosting clock, and f_{FR} frame frequency.

f_{OSC} = (No. of digits) × (1/Duty) × f_{FR}
f_{BST} = (1/2) × (1/No. of digits) × f_{OSC}
Example: The SED1230 has 13 digits of display and 1/30 duty.
f_{OSC} = 13 × 30 × 100 = 39 kHz
f_{BST} = (1/2) × (1/13) × 39 K = 1.5 kHz

*12: The V_{REG} reference voltage has the temperature characteristics of approximately –0.17%/°C (standard specifications). An optional model having the temperature characteristics of approximately –0.04%/°C is also available. The CGROM modification rules apply to the optional models.
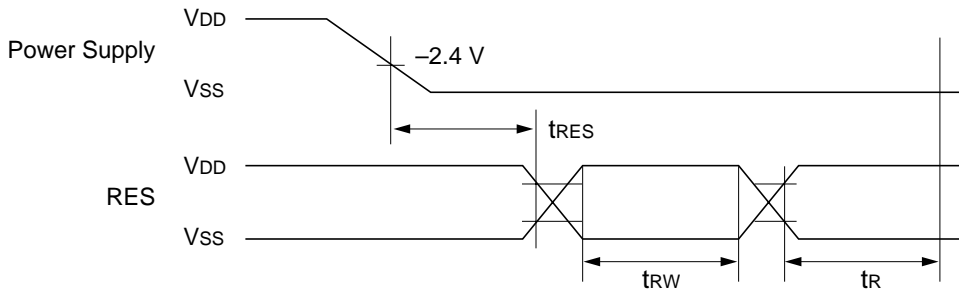
All signal timings are based on 20% and 80% of V_{SS} signals.

TIMING CHARACTERISTICS

(1)   System Bus Write Characteristic I (80 series MPU)
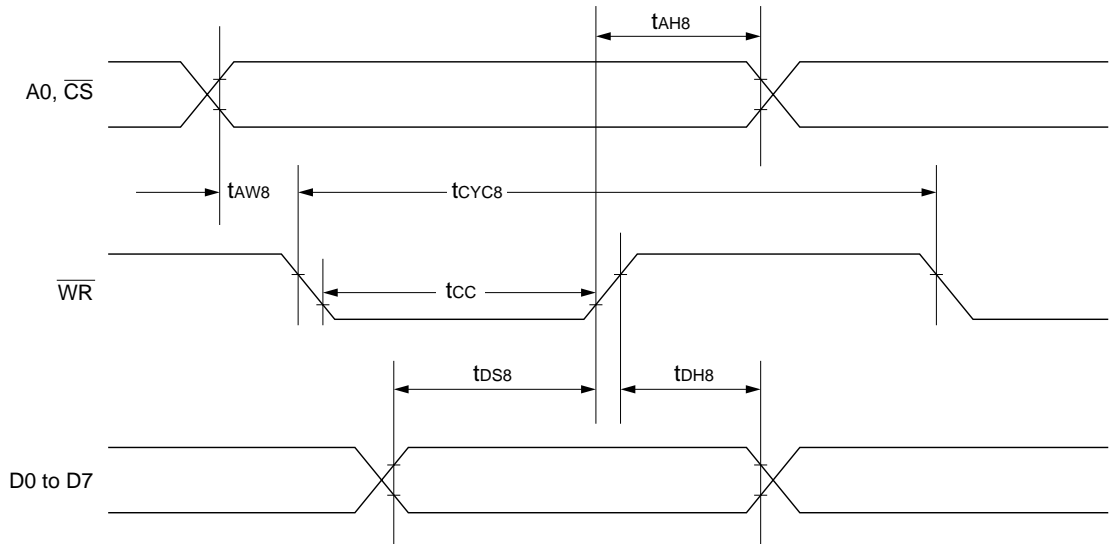
[Vss = −3.6 V to −2.4 V, Ta = −30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{\text{CS}}$	t AH8		30		ns
Address setup time		t AW8		60		ns
System cycle time	$\overline{\text{WR}}$	t CYC8	Vss = −3.0	500		ns
			−2.7	550		
			−2.4	650		
Control pulse width ($\overline{\text{WR}}$)		t CC	Vss = −3.0	100		ns
			−2.7	120		
			−2.4	150		
Data setup time	D0 ~ D7	t DS8		100		ns
Data hold time		t DH8		50		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of Vss.
*3: For A0 and $\overline{\text{CS}}$, the same time is not required. Input signals so that A0 and $\overline{\text{CS}}$ may satisfy tAW8 and tAH8 respectively.

(2) System Bus Write Characteristic II (68 series MPU)

[VSS = −3.6 V to −2.4 V, Ta = −30 to 85°C unless otherwise specified]

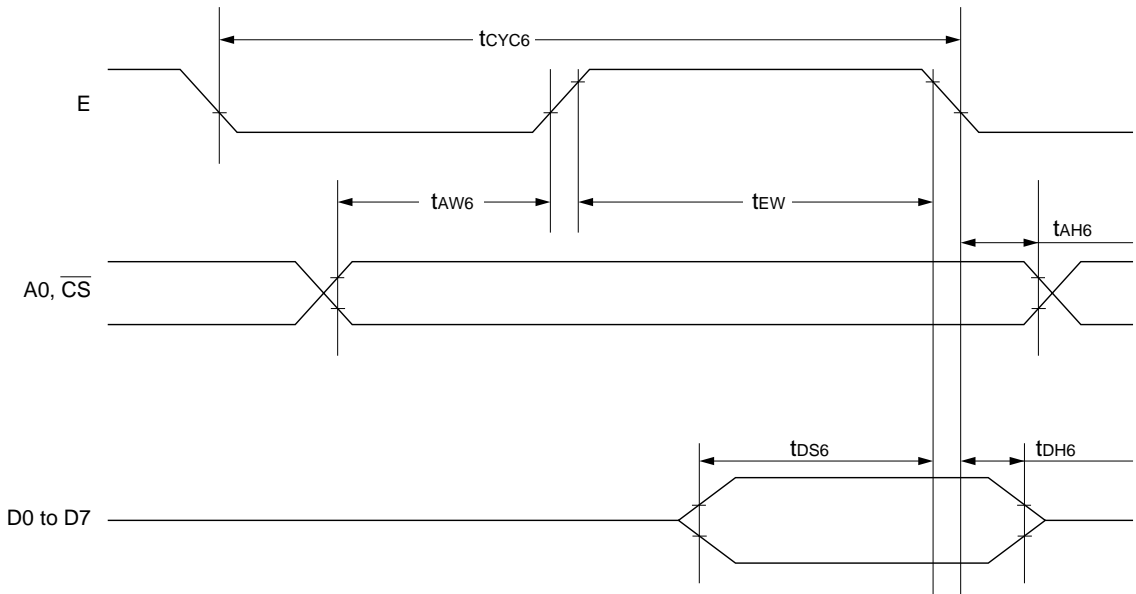| Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, CS	t CYC6	VSS = −3.0	500		ns
			−2.7	550		
			−2.4	650		
Address setup time		t AW6		60		
Address hold time		t AH6		30		ns
Data setup time	D0 ~ D7	t DS6		100		ns
Data hold time		t DH6		50		ns
Enable pulse width	E	t EW	VSS = −3.0	100		ns
			−2.7	120		
			−2.4	150		

*1: tCYC6 denotes the cycle of the E signal in the CS active state. tCYC6 must be reserved after CS becomes active.
*2: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*3: Every timing is specified on the basis of 20% and 80% of VSS.
*4: For A0 and CS, the same timing is not required. Input signals so that A0 and CS may satisfy tAW6 and tAH6 respectively.

(3) Serial Interface
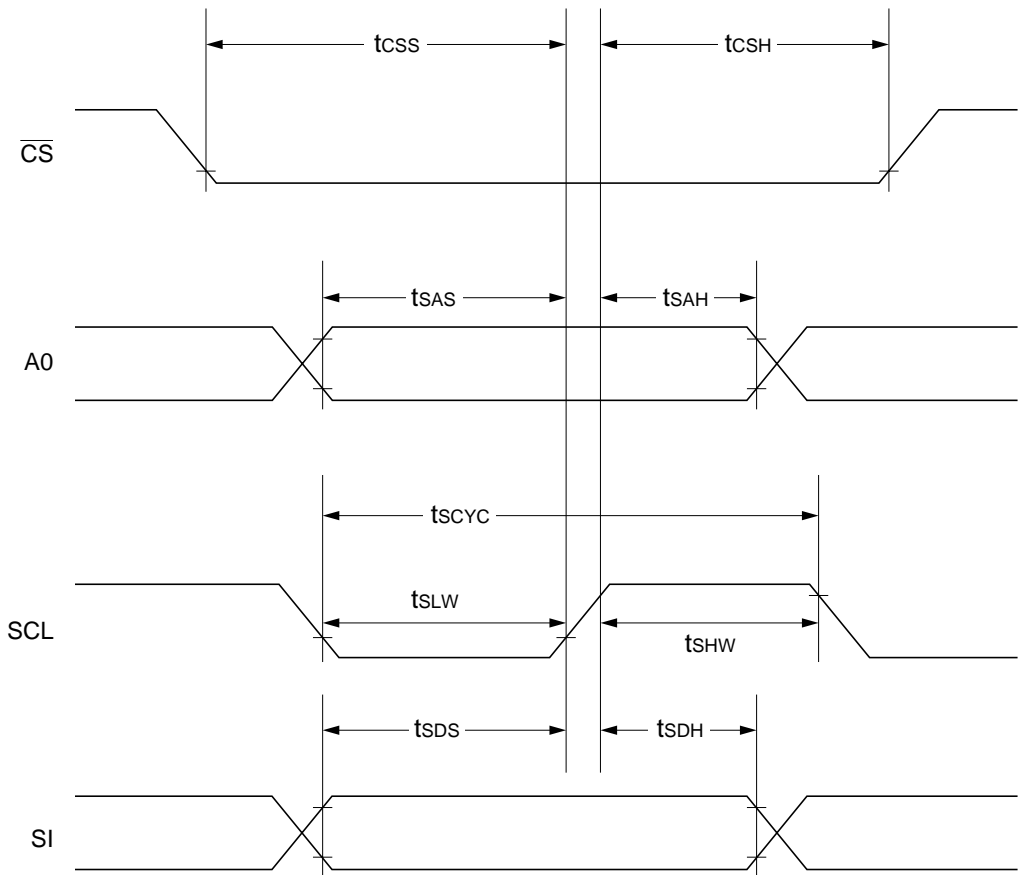
[Vss = −3.6 V to −2.4 V, Ta = −30 to 85°C]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	Vss = −3.0	700		ns
			−2.7	800		ns
			−2.4	1000		ns
SCL "H" pulse width		tSHW		300		ns
SCL "L" pulse width		tSLW		300		ns
Address setup time	A0	tSAS		50		ns
Address hold time		tSAH	Vss = −3.0	350		ns
			−2.7	400		ns
			−2.4	500		ns
Data setup time	SI	tSDS		50		ns
Data hold time		tSDH		50		ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS		150		ns
		tCSH	Vss = −3.0	550		ns
			−2.7	650		ns
			−2.4	700		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of Vss.

EPSON

MPU INTERFACE (REFERENCE EXAMPLES)

The SED1234, 1235 can be connected to the 80 series MPU and 68 series MPU. When an serial interface is used, the SED1234, 1235 Series can be operated by less signal lines.

80 Series MPU
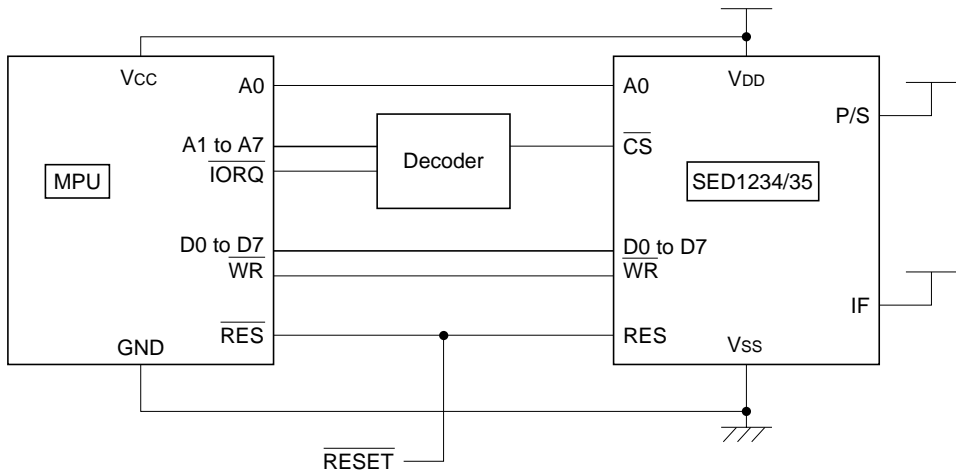
68 Series MPU
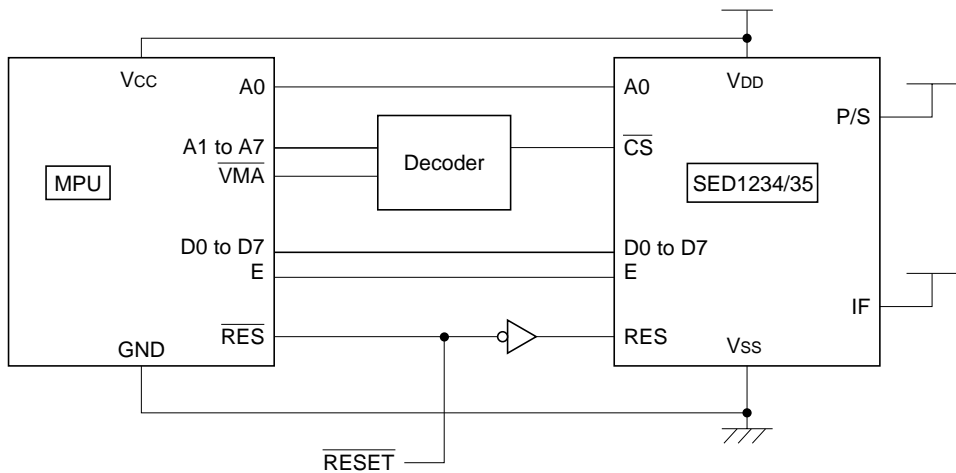
Serial Interface
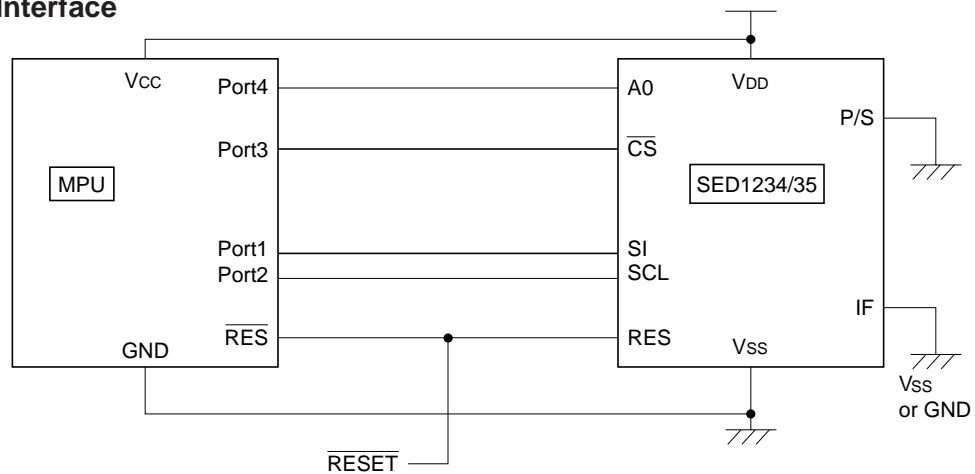
SED1234/35 Series

INTERFACE TO LCD CELLS (REFERENCE)

12 columns by 2 lines, 5×7-dot matrix segments and symbols
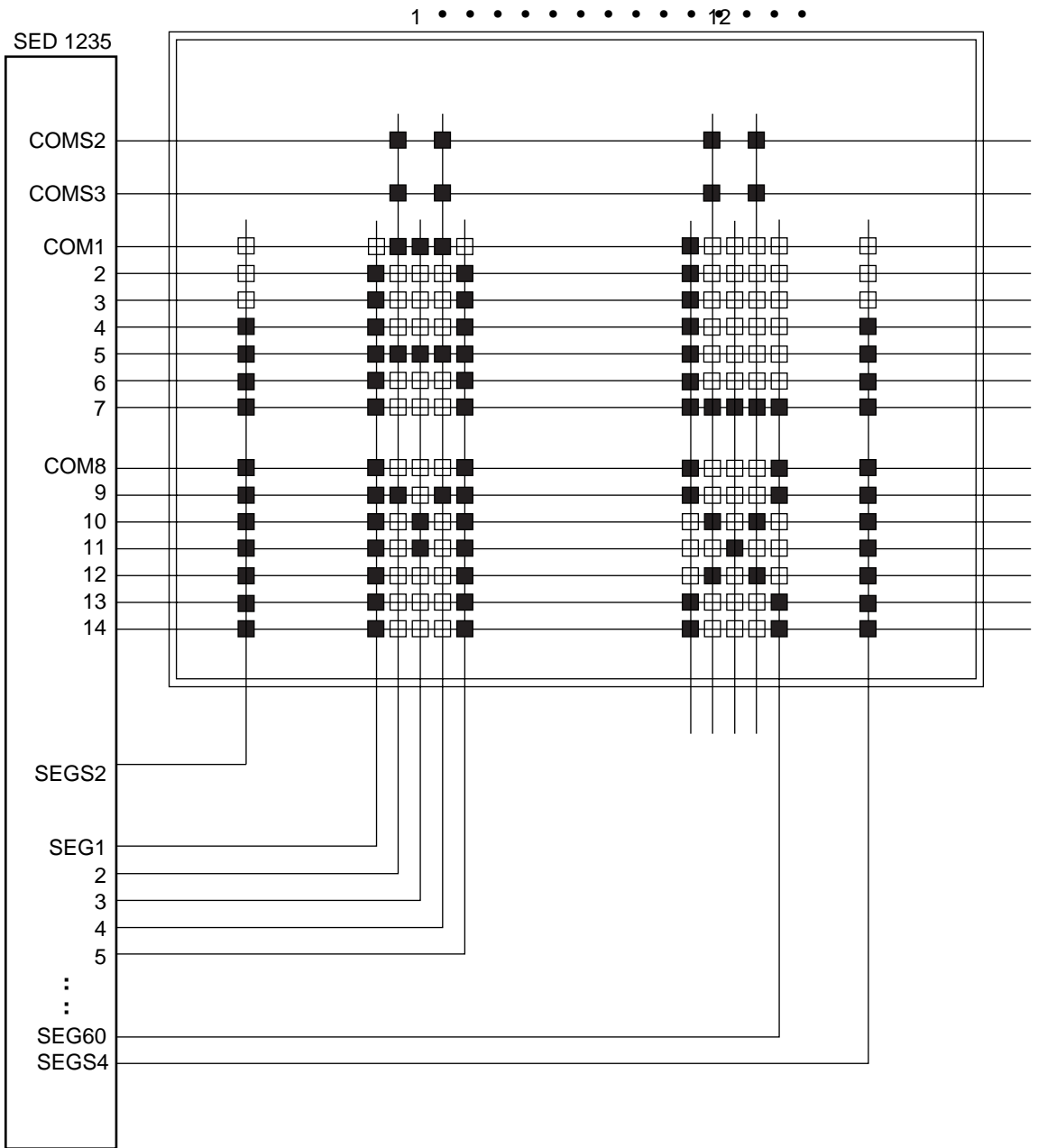
■ **System Setup**

N2	N1
0	0

EPSON

LIQUID CRYSTAL DRIVE WAVEFORMS (B WAVEFORMS)
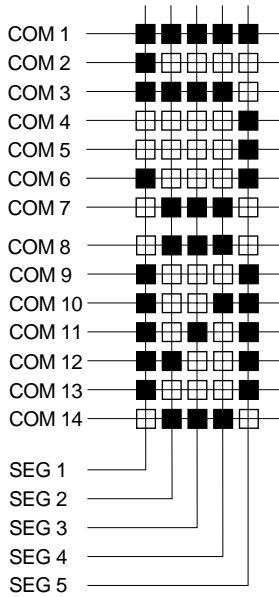
Instruction Setup Example (Reference Only)

(1) Initial setup

VDD-VSS power ON

Power regulation

Input of reset signal

Command status
- Static display control : Off
- Display on/off control : Off
- Power save   : Off
- Power control   : Off
- System reset   : CG=0
- Others are undefined.

Waiting for 10 μsec or more

Command input: (Asterisk indicates any command sequence.)
(1) System setup command
(*) Static display control command
     (Valid in Standby mode only)
(*) Display on/off control command
     • D: On (Display)
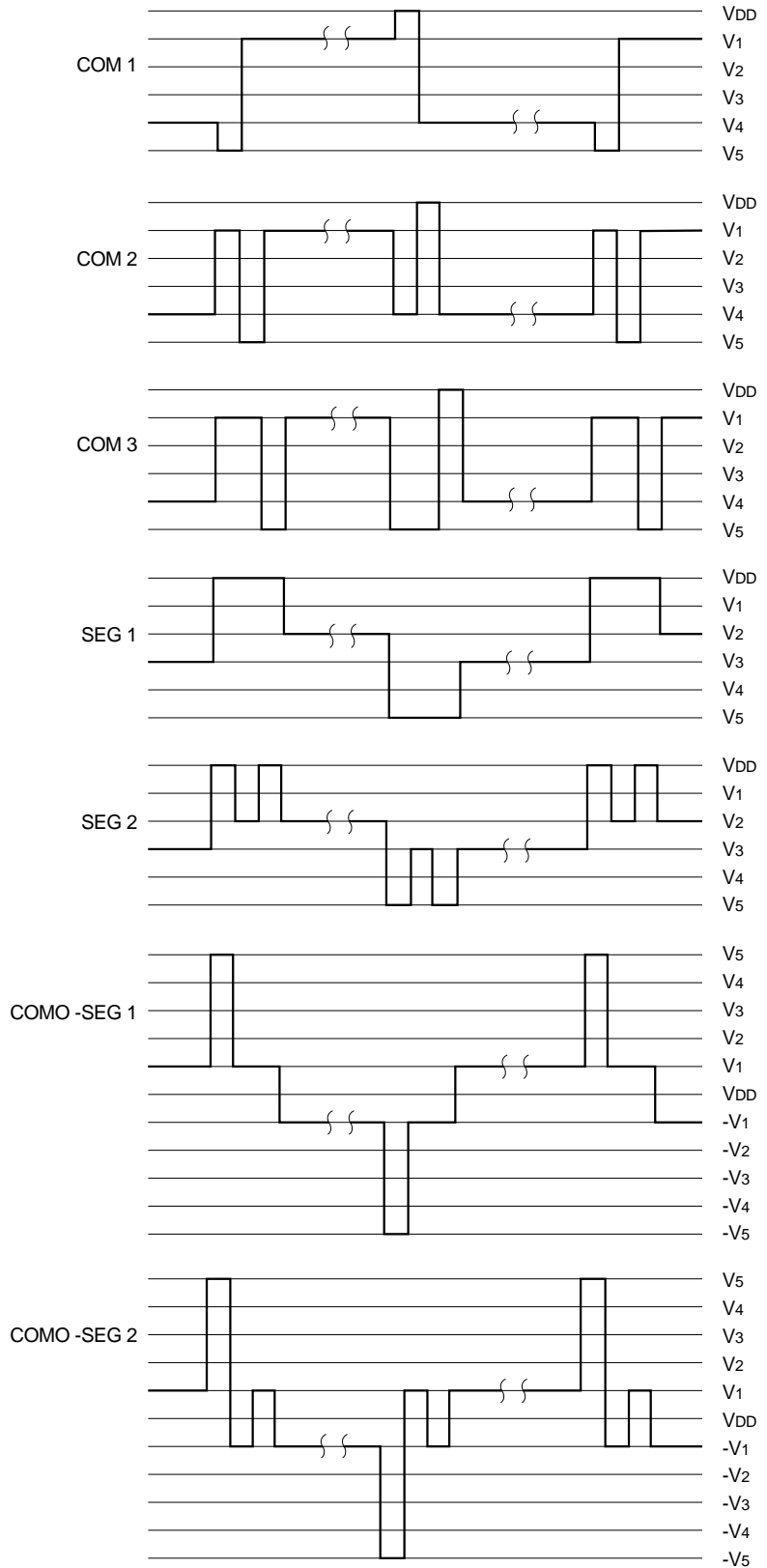(*) Electronic volume register setup
     • Data: (0, 0, 0, 0)
(*) Power save command
     • PS: Off (Power save)
     • O: On (Oscillation)
(6) RAM address setup   (Note 1)
(7) Data writing   (Note 1)

Waiting for 20 msec or more

Command input
(8) Power control commands
     • P, VF, VC: On

Command input:
(9) Electronic volume register setup
     • Data: Appropriate value

End of initialization

(2) Display mode

End of initialization

Input of RAM address setup command

Input of RAM (data) write command

Display of written data

Note 1:   Commands (6) and (7) initialize the RAM. The display contents must first be set. The non-display area must satisfy the following conditions (for RAM clear).
- DDRAM: Write the 20H data (character code).
- CGRAM: Write the 00H data (null data).
- Symbol register: Write the 00H data (null data).

As the RAM data is unstable during reset signal input (after power-on), null data must be written. If not, unexpected display may result.

EPSON

(3-1) Selecting the Standby mode

End of initialization

Normal operation (Power Save is released and oscillator circuit is turned ON.)

Command input:
(1) Display on/off control command   (Note 2)
    • D: Off (Display)
(2) Power save command   (Note 2)
    • PS: On (Power save)
    • O: On (Oscillation)
(3) Power control commands
    • P, VF, VC: Off

Standby status

Static display control commands can be used.
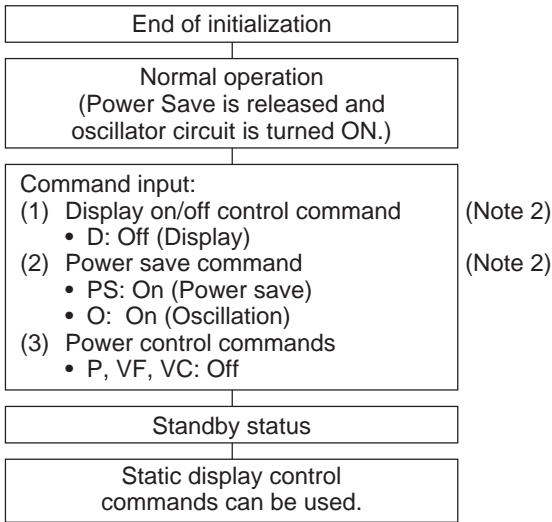
(3-2) Releasing the Standby mode

Standby mode

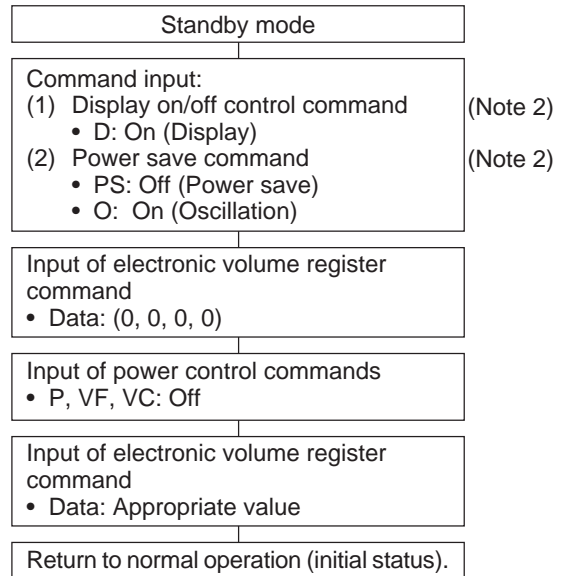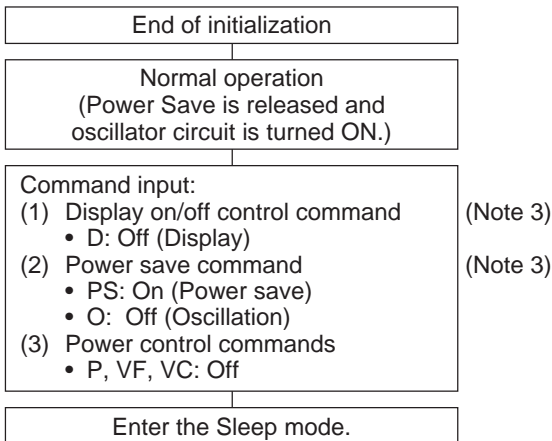| Command input:
(1) Display on/off control command   (Note 2)
    • D: On (Display)
(2) Power save command   (Note 2)
    • PS: Off (Power save)
    • O: On (Oscillation) |
| --- |

Input of electronic volume register command • Data: (0, 0, 0, 0)

Input of power control commands • P, VF, VC: Off

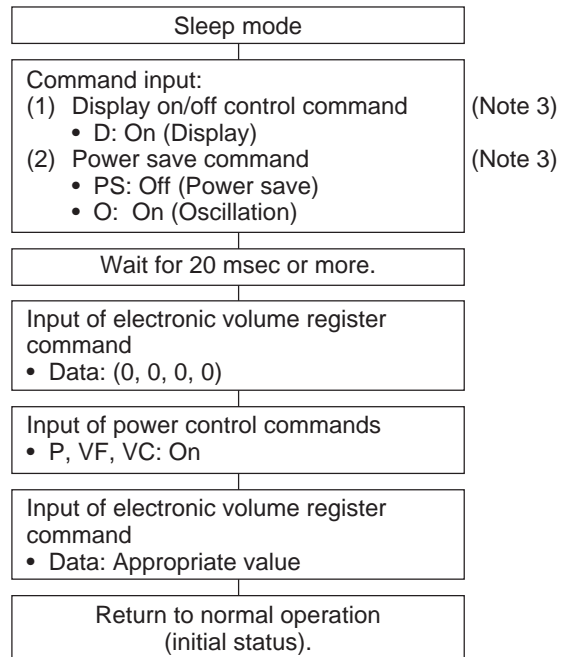| Input of electronic volume register
command
• Data: Appropriate value |
| --- |

Return to normal operation (initial status).

Note 2:   Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

(4-1) Selecting the Sleep mode

End of initialization

Normal operation (Power Save is released and oscillator circuit is turned ON.)

Command input:
(1) Display on/off control command   (Note 3)
    • D: Off (Display)
(2) Power save command   (Note 3)
    • PS: On (Power save)
    • O: Off (Oscillation)
(3) Power control commands
    • P, VF, VC: Off

Enter the Sleep mode.

(4-2) Releasing the Sleep mode

Sleep mode

Command input:
(1) Display on/off control command   (Note 3)
    • D: On (Display)
(2) Power save command   (Note 3)
    • PS: Off (Power save)
    • O: On (Oscillation)

Wait for 20 msec or more.

Input of electronic volume register command • Data: (0, 0, 0, 0)

Input of power control commands • P, VF, VC: On

Input of electronic volume register command • Data: Appropriate value

Return to normal operation (initial status).

Note 3:   Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

**SED1234/35
Series**