

# SED1330F

## Graphic LCD Controller

- For Medium-scale LCD
- Simplified External Circuits
- Virtual Screen Display RAM
- Enhanced Control Function

### DESCRIPTION

The SED1330F is a graphics and character display controller for use with medium scale dot matrix LCDs. The SED1330F generates all the signals required by the display memory and LCD drivers, and incorporates a character generator ROM, so that flexible, low power, display systems can be designed with a minimum number of external components.

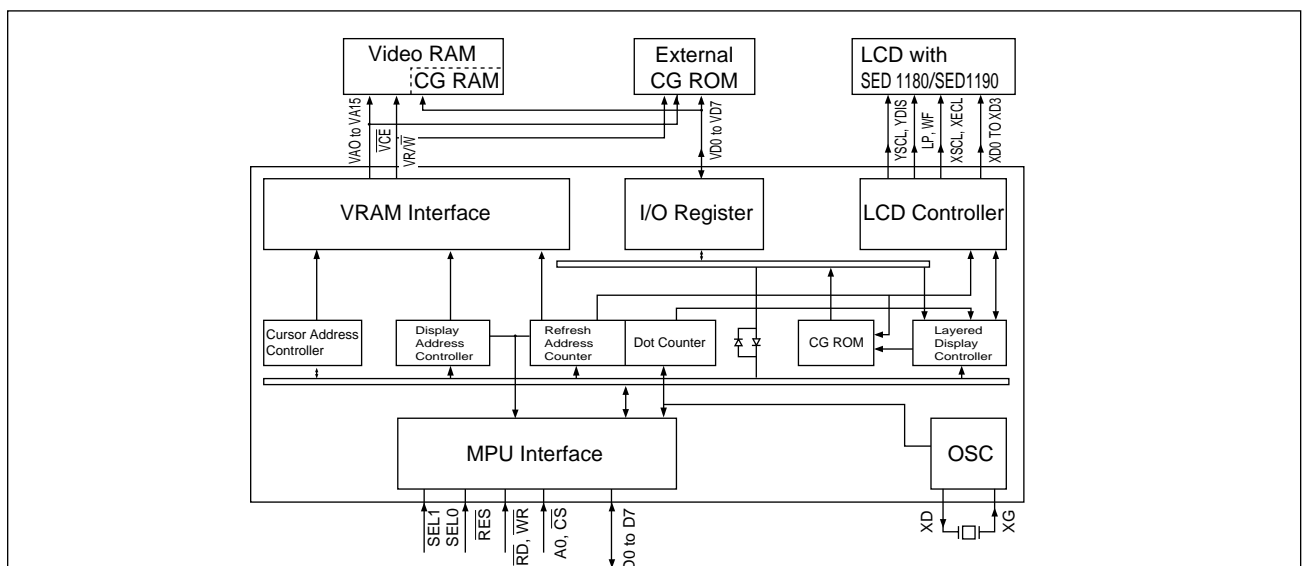
The SED1330F's high speed MPU interface can be configured for both 6800 family and 8080 family processors, and the rich command set allows the user to create a layered display of characters and graphics, scroll the display, and assign display attributes to selected areas of the screen with a minimum of MPU intervention. The controller also functions as a pipeline buffer between the MPU and display memory so that low cost, medium speed SRAM can be used.

The SED1330F character generator system supports user defined characters, which can be used alone, or in conjunction with the on board character set.

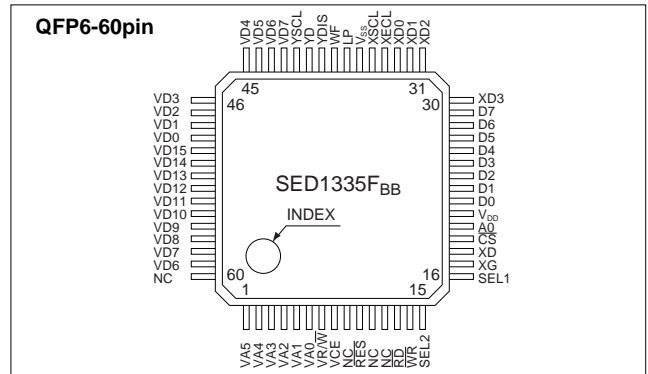
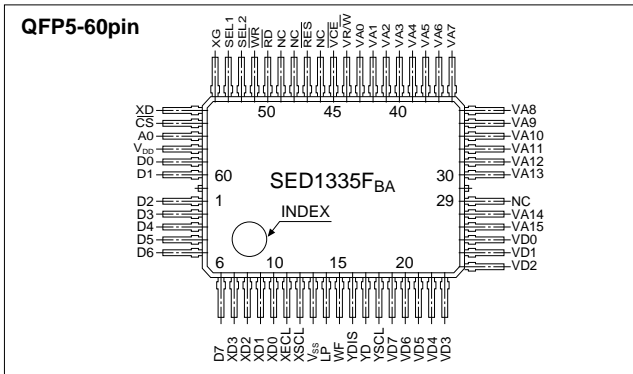
### FEATURES

- 6800 and 8080 family compatibility, 2-pin programmable
- Programmable cursor movement
- Flexible scrolling
  - ...Scrolling in both horizontal and vertical directions
  - ...Scrolling of selected areas of the display
- Multimode display
  - ...Up to 2 layers of mixed character and graphics
  - ...Up to 3 layers of graphics
- Selectable display synthesis
  - ...Display attributes (reverse video, flashing, etc.) for selected areas of the display
  - ...Simple animation
- Supports 64K bytes of memory
  - ....4K bytes of user definable characters
  - ....60K bytes of display memory
- 160 JIS 5×7 pixel characters internal
- Supports external character ROM or RAM
  - ....8×8 or 8×16 pixel characters
  - ....Allows mixing of ROM RAM character sets
- Variable LCD duty cycle, from 1/2 to 1/256
- Low power CMOS fabrication
  - ....5mA (typical)
  - ....0.05µA (typical), standby
- Single 5V supply
- Package...SED1330F<sub>BA</sub> QFP5-60pin (plastic)  
SED1330F<sub>BB</sub> QFP5-60pin (plastic)

### BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin Name	Pin No.		I/O	Function	Pin Name	Pin No.		I/O	Function
	SED1330F <sub>BA</sub>	SED1330F <sub>BB</sub>				SED1330F <sub>BA</sub>	SED1330F <sub>BB</sub>		
XG	54	17	I	Oscillator terminal	VD7 to VD0	19 to 26	42 to 49	I/O	VRAM data bus
XD	55	18	O	Oscillator terminal	VR/W	44	7	O	VRAM R/W signal
VDD	58	21	+5V	Power supply	VCE	45	8	O	Memory control signal
VSS	13	36	GND(0V)	Power supply	XD3 to XD0	7 to 10	30 to 33	O	Dot data output bus to X driver
SEL1,2	53*52	16*15	I	MPU interface format selection	XSCL	12	35	O	Dot data shift clock for X driver
D0 to D7	59 to 60 1 to 6	22 to 29	I/O	Data bus	LP	11	34	O	Chip enable shift clock for X driver
A0	57	20	I	Data type selection	WF	14	37	O	Dot data latch pulse
RD	50	13	I	80 series Read strobe signal 68 series "E" clock	YSCL	15	38	O	Frame signal
WR	51	14	I	80 series Write strobe signal 68 series R/ W signal	YD	18	41	O	Scan data shift clock for Y driver
CS	56	19	I	Chip select	YDIS	17	40	O	Scan data output
RES	47	10	I	Reset		16	39	O	Power down signal when display OFF
VA15 to VA0	27*28 30 to 43	1 to 6 50 to 59	O	VRAM address bus					

NC : Non Connection

■ ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0V)

Rating	Symbol	Value	Unit
Supply voltage	V <sub>DD</sub>	-0.3 to 7.0	V
Input voltage	V <sub>I</sub>	-0.5 to V <sub>DD</sub> +0.5	V
Power dissipation	P <sub>D</sub>	300	mW
Operating temperature	T <sub>opr</sub>	-20 to 75	°C
Storage temperature	T <sub>stg</sub>	-60 to 150	°C
Soldering temperature and time	T <sub>sol</sub>	260°C, 10s (at lead)	—

■ ELECTRICAL CHARACTERISTICS

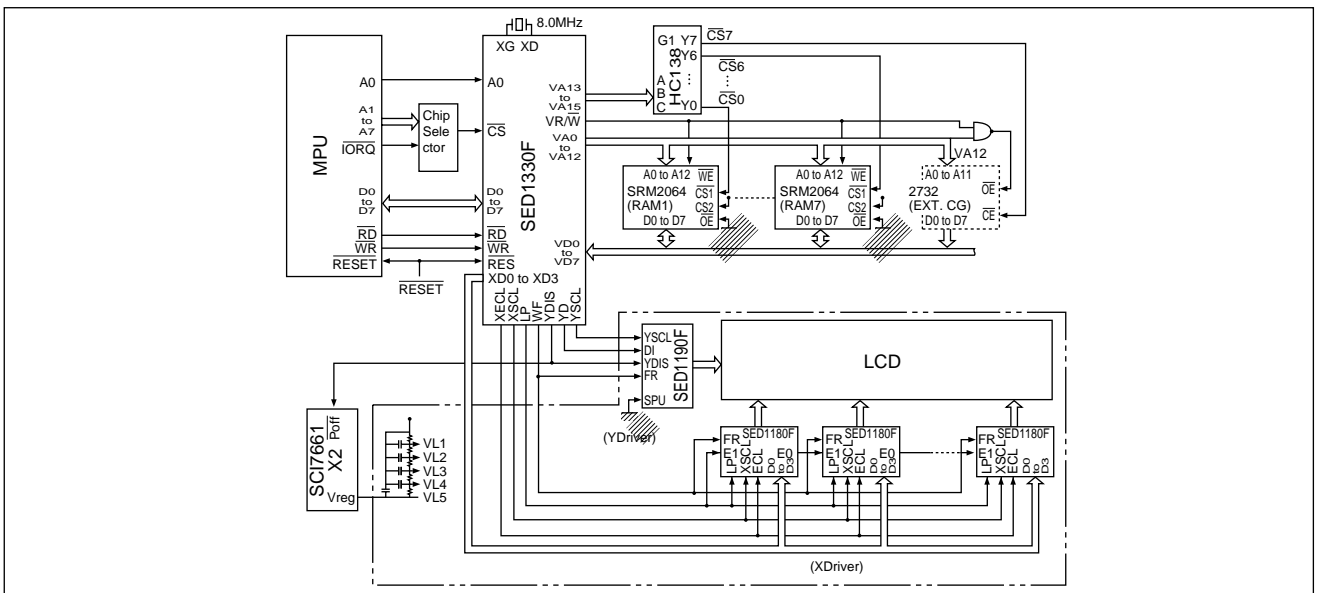
(V<sub>DD</sub> = 5V±10%, V<sub>SS</sub> = 0V, Ta = -20 to 75°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V <sub>DD</sub>		4.5	5.0	5.5	V
Register data retention voltage	V <sub>OH</sub>		2.0	—	6.0	V
TTL	High level input voltage	V <sub>IHT</sub>	2.2	—	V <sub>DD</sub> +0.3	V
	Low level input voltage	V <sub>ILT</sub>	-0.3	—	0.8	V
	High level output voltage	V <sub>OHT</sub>	2.4	—	—	V
	Low level output voltage	V <sub>OLT</sub>	—	—	0.4	V

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
CMOS	High level input voltage	$V_{IH}$	$I_{OH} = 1.6\text{mA}, I_{OL} = -1.6\text{mA}$	$0.8V_{DD}$	—	—	V
	Low level input voltage	$V_{IL}$	SEL1,2, SYNC, YD, XD0 to XD3, XSCL, XECL, LP, FR, YSCL, YDIS, OSC1, OSC2	—	—	$0.2V_{DD}$	V
	High level output voltage	$V_{OH}$		$V_{DD}-0.4$	—	—	V
	Low level output voltage	$V_{OL}$		—	—	0.4	V
+5V	Positive trigger threshold voltage	$V_{T+}$	RES*	$0.5V_{DD}$	$0.7V_{DD}$	$0.8V_{DD}$	V
	Negative trigger threshold voltage	$V_{T-}$		$0.2V_{DD}$	$0.3V_{DD}$	$0.5V_{DD}$	V
Input leakage current		$I_{LI}$	$V_I = V_{DD} \text{ or } V_{SS}$	—	0.05	2.0	$\mu\text{A}$
Output leakage current		$I_{LO}$		—	0.10	5.0	$\mu\text{A}$
Average operating current		$I_{DDA}$	$f_{OSC} = 10\text{MHz}$ , No load (No external V-RAM)	—	8	12	mA
Standby current		$I_{DDS}$	$XG = CS = V_{DD}$	—	0.05	20	$\mu\text{A}$
Oscillation frequency		$f_{OSC}$	AT X' tal XG, XD	1.0	—	10.0	MHz
External clock frequency		$f_{CLK}$		—	—	10.0	MHz
Feed back resistance		$R_f$		0.5	1.0	5.0	$\text{M}\Omega$

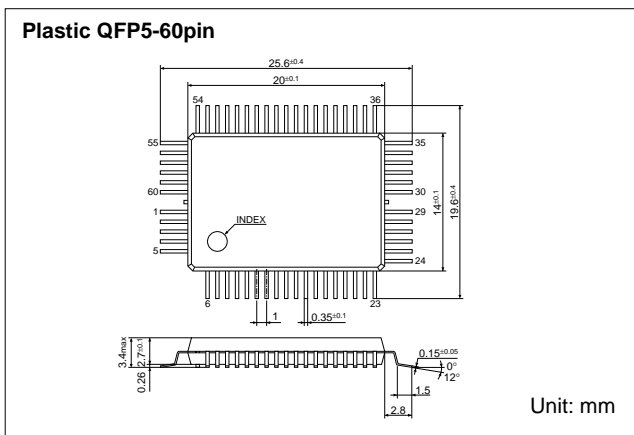
\* RES input pulse should be longer than 1.0ms.  
 $V_{LS}$  should be OFF when RES is "L"

■ MPU AND LCD PANEL CONNECTION EXAMPLE

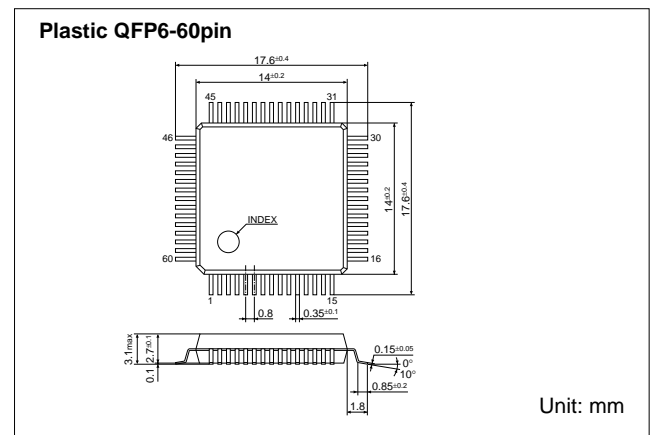


■ PACKAGE DIMENSIONS

● SED1330FBA



● SED1330FBB



■ CHARACTER CODE TABLE (BUILT-IN CHARACTER GENERATOR)

		Lower 4bit (D0 to D3) of Character Code (Hexadecimal)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Upper 4bit (D4 to D7) of Character Code (Hexadecimal)	2		!	"	#	\$	%	&	'	(	)	*	+	,	-	.	/
	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
	6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
	7	p	q	r	s	t	u	v	w	x	y	z	{		}	~	
	A																
	B	—															
	C																
	D																
1																	

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