EPSON

SED1330F

Graphic LCD Controller

- **For Medium-scale LCD**
- **Simplified External Circuits**
- **Virtual Screen Display RAM**
- **Enhanced Control Function**

■ DESCRIPTION

The SED1330F is a graphics and character display controller for use with medium scale dot matrix LCDs. The SED1330F generates all the signals required by the display memory and LCD drivers, and incorporates a character generator ROM, so that flexible, low power, display systems can be designed with a minimum number of external components.

The SED1330F's high speed MPU interface can be configured for both 6800 family and 8080 family processors, and the rich command set allows the user to create a layered display of characters and graphics, scroll the display, and assign display attributes to selected areas of the screen with a minimum of MPU intervention.

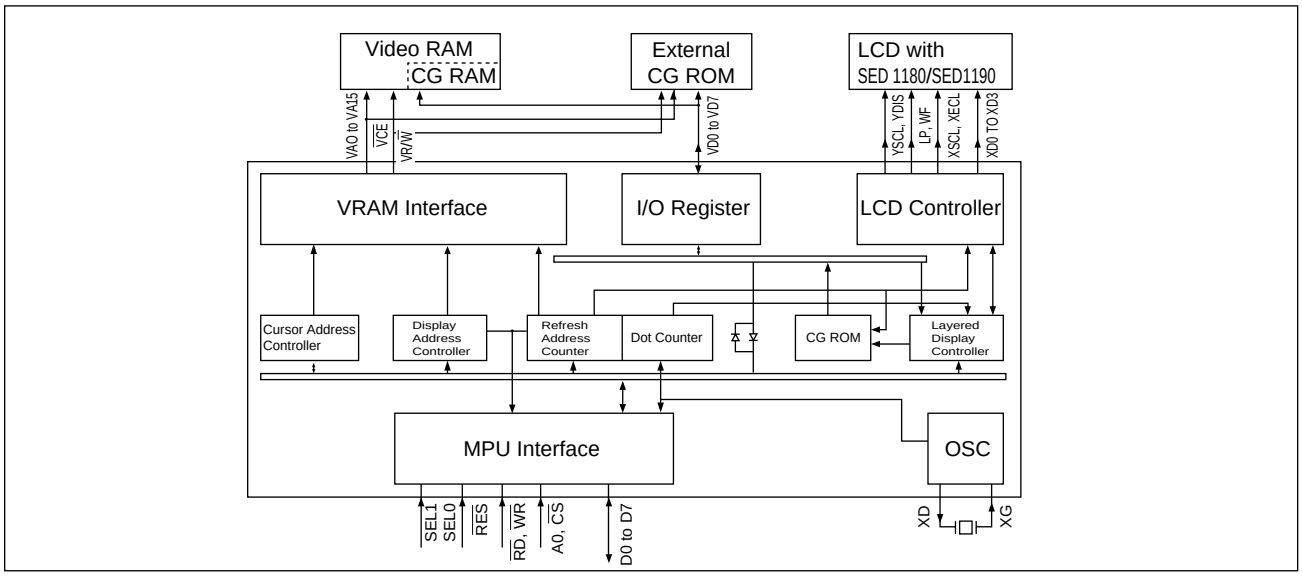
The controller also functions as a pipline buffer between the MPU and display memory so that low cost, mediunm speed SRAM can be used.

The SED1330F character generator system supports user defined characters, which can be used alone, or in conjunction with the on board character set.

■ FEATURES

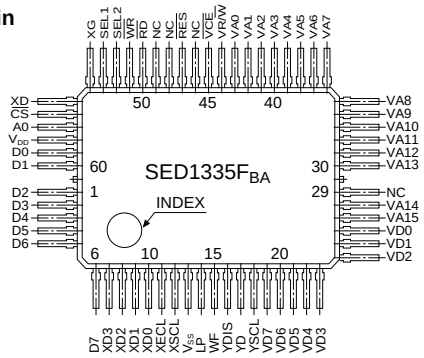
- 6800 and 8080 family compatibility, 2-pin programmable
- Programmable cursor movement
- Flexible scrolling
  ...Scrolling in both horizontal and vertical directions
  ...Scrolling of selected areas of the display
- Multimode display
  ...Up to 2 layers of mixed character and graphics
  ...Up to 3 layers of graphics
- Selectable display synthesis
  ...Display attributes (reverse video, flashing, etc.) for selected areas of the display
  ...Simple animation
- Supports 64K bytes of memory
  ....4K bytes of user definable characters
  ....60K bytes of display memory
- 160 JIS 5×7 pixel characters internal
- Supports external character ROM or RAM
  ....8×8 or 8×16 pixel characters
  ....Allows mixing of ROM RAM character sets
- Variable LCD duty cycle, from 1/2 to 1/256
- Low power CMOS fabrication
  ....5mA (typical)
  ....0.05µA (typical), standby
- Single 5V supply
- Package...SED1330F$_{BA}$ QFP5-60pin (plastic)
  SED1330F$_{BB}$ QFP5-60pin (plastic)

■ BLOCK DIAGRAM

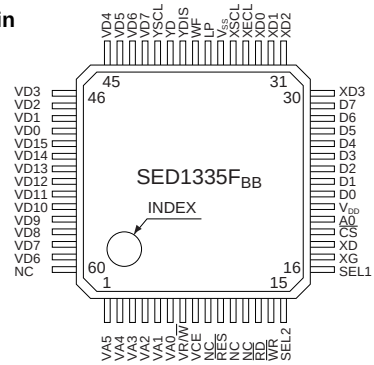


■ PIN CONFIGURATION

QFP5-60pin



QFP6-60pin



■ PIN DESCRIPTION

Pin Name	PIn No.		I/O	Function
	SED1330F$_{BA}$	SED1330F$_{BB}$		
XG	54	17	I	Oscillator terminal
XD	55	18	O	Oscillator terminal
V_{DD}	58	21	+5V	Power supply
V_{SS}	13	36	GND(0V)	Power supply
SEL1,2	53•52	16•15	I	MPU interface format selection
D0 to D7	59 to 60 1 to 6	22 to 29	I/O	Data bus
A0	57	20	I	Data type selection
RD	50	13	I	80 series Read strobe signal 68 series "E" clock
WR	51	14	I	80 series Write strobe signal 68 series R/ W signal
CS	56	19	I	Chip select
RES	47	10	I	Reset
VA15 to VA0	27•28 30 to 43	1 to 6 50 to 59	O	VRAM address bus

Pin Name	Pin No.		I/O	Function
	SED1330F$_{BA}$	SED1330F$_{BB}$		
VD7 to VD0	19 to 26	42 to 49	I/O	VRAM data bus
VR/$\overline{W}$	44	7	O	VRAM R/$\overline{W}$ signal
$\overline{VCE}$	45	8	O	Memory control signal
XD3 to XD0	7 to 10	30 to 33	O	Dot data output bus to X driver
XSCL	12	35	O	Dot data shift clock for X driver
LP	11	34	O	Chip enable shift clock for X driver
WF	14	37	O	Dot data latch pulse
YSCL	15	38	O	Frame signal
YD	18	41	O	Scan data shift clock for Y driver
YDIS	17	40	O	Scan data output
	16	39	O	Power down signal when display OFF

NC : Non Connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 7.0	V
Input voltage	V_I	–0.5 to V_{DD}+0.5	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–60 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■ ELECTRICAL CHARACTERISTICS

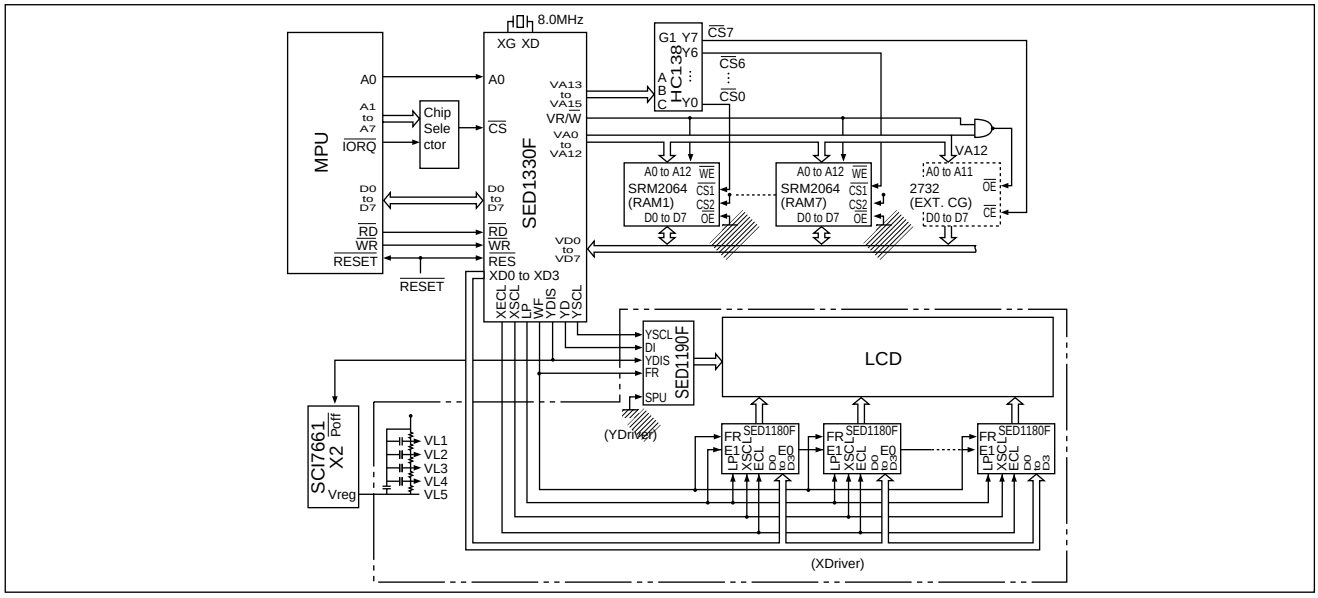
(V_{DD} = 5V±10%, V_{SS} = 0V, Ta = –20 to 75°C)

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage		V_{DD}		4.5	5.0	5.5	V
Register data retention voltage		V_{OH}		2.0	—	6.0	V
TTL	High level input voltage	V_{IHT}	D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, I_{OH} = –5.0mA, I_{OL} = 5.0mA, VR/ $\overline{W}$, $\overline{VCE}$, $\overline{REF}$	2.2	—	V_{DD}+0.3	V
	Low level input voltage	V_{ILT}		–0.3	—	0.8	V
	High level output voltage	V_{OHT}		2.4	—	—	V
	Low level output voltage	V_{OLT}		—	—	0.4	V

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
CMOS	High level input voltage	V_{IHC}	I_{OH} = 1.6mA, I_{OL} = –1.6mA, SEL1,2, SYNC, YD, XD0 to XD3, XSCL, XECL, LP, FR, YSCL, YDIS, OSC1, OSC2	$0.8V_{DD}$	—	—	V
	Low level input voltage	V_{ILC}		—	—	$0.2V_{DD}$	V
	Hight level output voltage	V_{OHC}		V_{DD}—0.4	—	—	V
	Low level output voltage	V_{OLC}		—	—	0.4	V
SCHMITT	Positive trigger threshold voltage	V_{T+}	$\overline{RES}$*	$0.5V_{DD}$	$0.7V_{DD}$	$0.8V_{DD}$	V
	Negative trigger threshold voltage	V_{T-}		$0.2V_{DD}$	$0.3V_{DD}$	$0.5V_{DD}$	V
Input leakage current		I_{LI}	$V_I = V_{DD}$ or V_{SS}	—	0.05	2.0	µA
Output leakage current		I_{LO}		—	0.10	5.0	µA
Average operating current		I_{DDA}	f_{OSC} = 10MHz, No load (No external V-RAM) XG = $\overline{CS}$ = V_{DD}	—	8	12	mA
Standby current		I_{DDS}		—	0.05	20	µA
Oscillation fraquency		f_{OSC}	AT X' tal XG, XD	1.0	—	10.0	MHz
External clock frequency		f_{CLK}		—	—	10.0	MHz
Feed back resistance		R_f		0.5	1.0	5.0	MΩ

* $\overline{RES}$ input pulse should be longer than 1.0ms.
V_{LS} should be OFF when $\overline{RES}$ is " L"

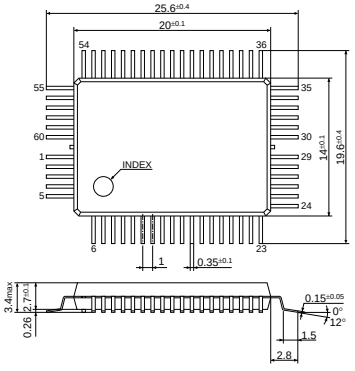
■ MPU AND LCD PANEL CONNECTION EXAMPLE



■ PACKAGE DIMENSIONS

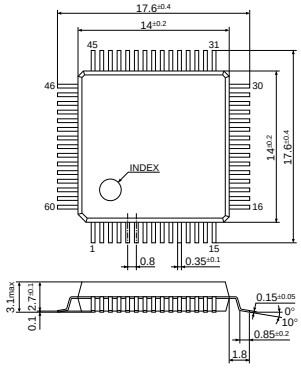
● SED1330F$_{BA}$

Plastic QFP5-60pin

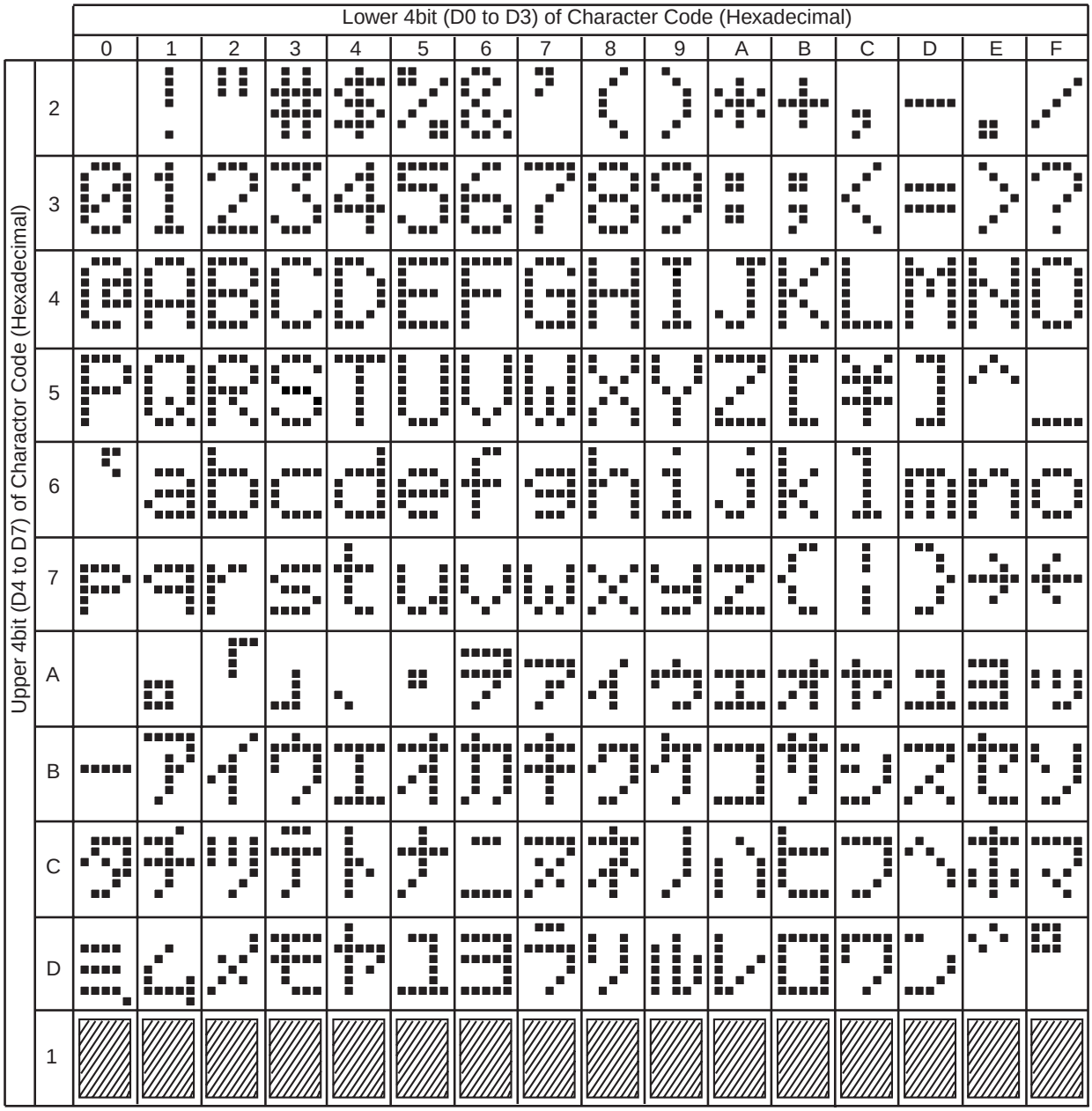


● SED1330F$_{BB}$

Plastic QFP6-60pin



■ CHARACTER CODE TABLE (BUILT-IN CHARACTER GENERATOR)



NOTICE

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Electric Device Information of EPSON WWW server

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