

SED1335

CMOS GRAPHIC LCD CONTROLLER

- For Medium-Scale LCD
- Low Operating Voltage 2.7 to 5.0V
- On-Chip Character Generator ROM

■ DESCRIPTION

The SED1335 is a CMOS low-power dot matrix liquid crystal graphic display controller. The device stores in external RAM display data sent by an 8-bit microcomputer, and generates all the signals required by the LCD drivers. The LSI incorporates an internal character generator ROM which supports user-defined characters (also an external CGROM can be supported).

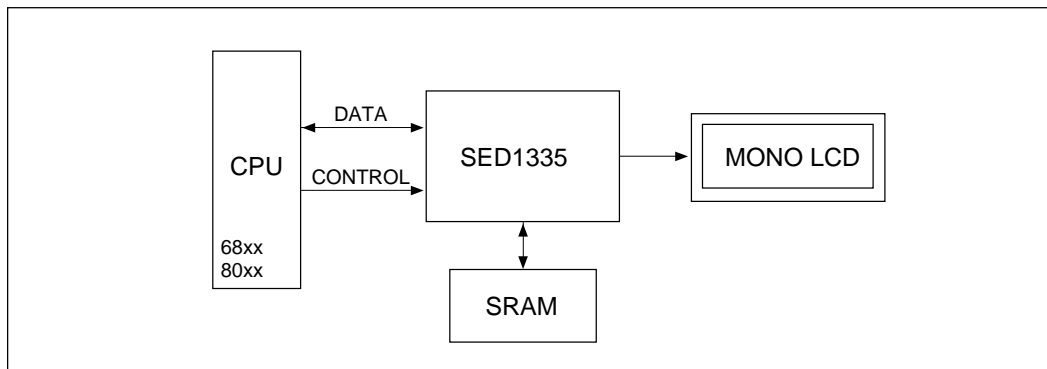
The SED1335 can be interfaced to high-speed microprocessors such as the Intel family or Motorola family. The controller supports a set of rich commands that will allow the user to create a layered display of characters and graphics.

Also, the controller functions as a pipeline buffer between the MPU and display memory so that low-cost, medium-speed SRAM can be used.

■ FEATURES

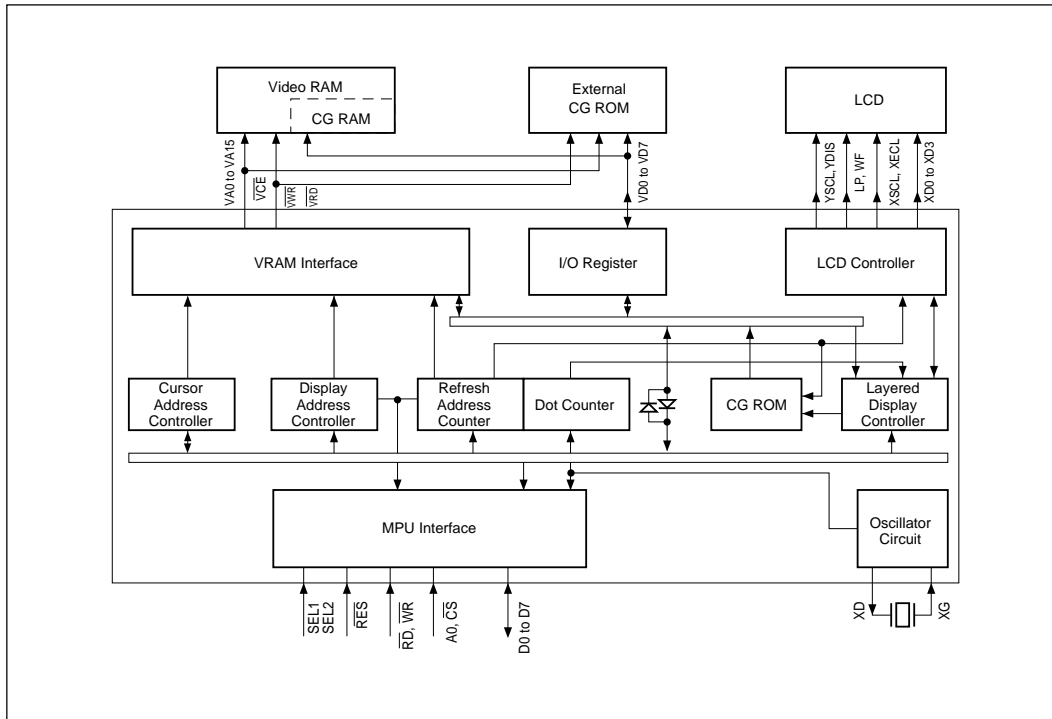
- CMOS low-power graphic and character display controller
- Selectable MPU interface is compatible with both the Intel family and the Motorola family
- Smooth scrolling support:
 - Horizontal and vertical scroll
 - Scrolling of selected areas of the display
- Multimode display:
 - 2 layers of overlapping characters and graphics
 - 3 layers of overlapping graphics
- Selectable display synthesis:
 - Inverse video
 - Flashing display, cursor on/off/blink
 - Under and bar cursor, block cursor
 - Simple animation
- Programmable cursor
- Internal character generator ROM
- Supports external character generator ROM:
 - 8 × 8 or 8 × 16 pixel characters
 - Allowing mixing of ROM and RAM character sets
- Supports 64K bytes of memory:
 - 4K bytes of user-definable characters
 - 60K bytes of display memory
 - in 2 of 32K × 8 100ns SRAM
 - or in 8 of 8K × 8 100ns SRAM
- Display duty 1/2 to 1/256
- Low power dissipation
 - 5mA (typical)
 - 0.05μA (typical), standby
- Logic power supply 2.7 to 5.5V
- Package: Plastic QFP5-60 pin (F0A)
Plastic QFP6-60 pin (F0B)

■ SYSTEM BLOCK DIAGRAM

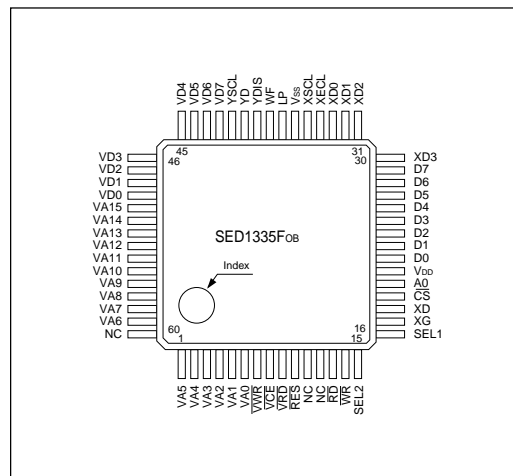
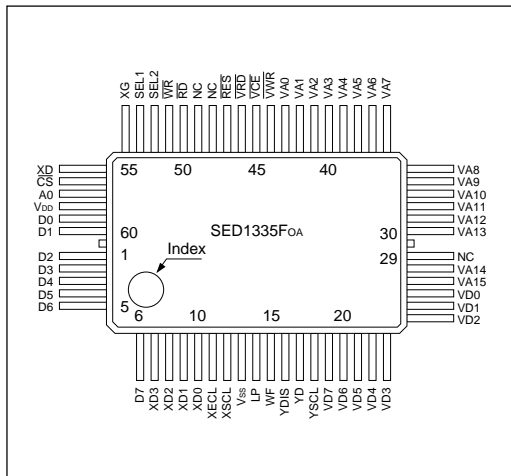


SED1335

■ BLOCK DIAGRAM



■ PINOUT



■ PIN DESCRIPTION

| Pin Name | Pin No. | | I/O | Functions |
|------------------|-------------------|------------------|---------|---|
| | SED1335FOA | SED1335FOB | | |
| XG | 54 | 17 | I | Oscillator terminal |
| XD | 55 | 18 | O | Oscillator terminal |
| V _{DD} | 58 | 21 | +5V | Power supply |
| V _{SS} | 13 | 36 | GND(0V) | Power supply |
| SEL1,2 | 53 • 52 | 16 • 15 | I | MPU interface format selection |
| D0 to D7 | 59 to 60, 1 to 6 | 22 to 29 | I/O | Data bus |
| A0 | 57 | 20 | I | Data type selection |
| \overline{RD} | 50 | 13 | I | 80 series Read strobe signal 68 series "E" clock |
| \overline{WR} | 51 | 14 | I | 80 series Write strobe signal 68 series R/W signal |
| \overline{CS} | 56 | 19 | I | Chip select |
| \overline{RES} | 47 | 10 | I | Reset |
| VA15 to VA0 | 27 • 28, 30 to 43 | 1 to 6, 50 to 59 | O | VRAM address bus |
| VD7 to VD0 | 19 to 26 | 42 to 49 | I/O | VRAM data bus |
| \overline{VWR} | 44 | 7 | O | VRAM write signal |
| \overline{VRD} | 46 | 9 | O | VRAM read signal |
| VCE | 45 | 8 | O | VRAM chip enable |
| XD3 to XD0 | 7 to 10 | 30 to 33 | O | Dot data output bus to X driver |
| XSCL | 12 | 35 | O | Dot data shift clock for X driver |
| XECL | 11 | 34 | O | Chip enable shift clock for X driver |
| LP | 14 | 37 | O | Dot data latch pulse |
| WF | 15 | 38 | O | Frame signal |
| YSCL | 18 | 41 | O | Scan data shift clock for Y driver |
| YD | 17 | 40 | O | Scan data output |
| YDIS | 16 | 39 | O | Power down signal when display is OFF |

NC: No Connection

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

| Parameter | Symbol | Ratings | Unit |
|--------------------------------|------------------|------------------------------|------|
| Supply voltage | V _{DD} | -0.3 to 7.0 | V |
| Input voltage | V _{IN} | -0.3 to V _{DD} +0.3 | V |
| Power dissipation | P _D | 300 | mW |
| Operating temperature | T _{opr} | -20 to 75 | °C |
| Storage temperature | T _{stg} | -60 to 150 | °C |
| Soldering temperature and time | T _{sol} | 260°C, 10s (at lead) | — |

● DC Electrical Characteristics (1)

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_a = -20 to 75°C)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | Terminal |
|--------------------------------------|------------------------------------|--|--------------------------|----------------------|---------------------|----------------------|---|
| Operating voltage | V _{DD} | | 4.5 | 5.0 | 5.5 | V | V _{DD} |
| Register data retention voltage | V _{OH} | | 2.0 | — | 6.0 | V | |
| T T L | High level input voltage | V _{IHT} | 0.5xV _{DD} | — | V _{DD} | V | D0 to D7, A0, CS, RD, WR, VD0 to VD7, VA0 to VA15, VCE, VRD, VWR |
| | Low level input voltage | V _{I LT} | V _{SS} | — | 0.2xV _{DD} | V | |
| | High level output voltage | V _{OHT} | I _{OH} = -5.0mA | 2.4 | — | V | |
| | Low level output voltage | V _{OLT} | I _{OL} = 5.0mA | — | — | V _{SS} +0.4 | |
| C M O S | High level input voltage | V _{IHC} | 0.8xV _{DD} | — | V _{DD} | V | SEL1, SEL2, YD, XD0 to XD3, XSCL, YDIS, LP, WF, CL0, XECL, YSCL |
| | Low level input voltage | V _{I LC} | V _{SS} | — | 0.2xV _{DD} | V | |
| | High level output voltage | V _{OHC} | I _{OH} = -2.0mA | V _{DD} -0.4 | — | V | |
| | Low level output voltage | V _{OLC} | I _{OL} = 2.0mA | — | — | V _{SS} +0.4 | |
| T T R I G G E R | Positive trigger threshold voltage | V _{T+} | 0.5V _{DD} | 0.7V _{DD} | 0.8V _{DD} | V | RES |
| | Negative trigger threshold voltage | V _{T-} | 0.2V _{DD} | 0.3V _{DD} | 0.5V _{DD} | V | |
| Input leakage current | I _{LI} | V _{IN} = V _{DD} /V _{SS} | — | 0.05 | 2.0 | μA | |
| Output leakage current | I _{LO} | | — | 0.10 | 5.0 | μA | |
| Average operating current | I _{opr} | f _{osc} = 10MHz, No-load 256 × 200 dot | — | 11 | 15 | mA | V _{DD} |
| Standby current | I _Q | Sleep X _G , CS, RD = V _{DD} | — | 0.05 | 20 | μA | V _{DD} |
| Oscillation frequency | f _{osc} | AT X'tal | 1.0 | — | 10.0 | MHz | X _G , X _D |
| External clock frequency | f _{CL} | Duty 47.5% | 1.0 | — | 10.0 | MHz | |
| Feed back resistance | R _f | | 0.5 | 1.0 | 3.0 | MΩ | |

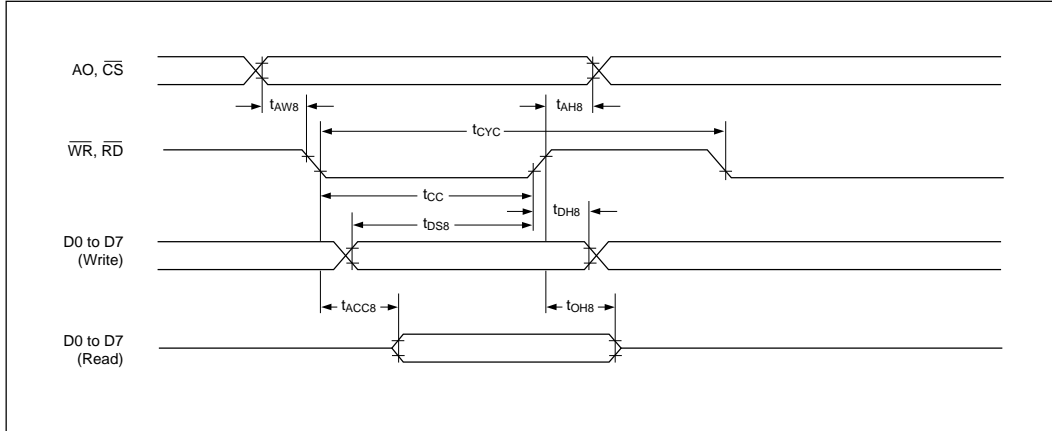
● DC Electrical Characteristics (2)

(V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = -20 to 75°C)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | Terminal | |
|---------------------------------|------------------------------------|---|--------------------------|--------------------------------|---------------------|----------------------|---|---|
| Operating voltage | V _{DD} | | 2.7 | 3.5 | 4.5 | V | V _{DD} | |
| Register data retention voltage | V _{OH} | | 2.0 | — | 6.0 | V | | |
| T T L | High level input voltage | V _{IHT} | 0.8xV _{DD} | — | V _{DD} | V | D0 to D7, A0, CS, RD, WR, VD0 to VD7, VA0 to VA15, VCE, VRD, VWR | |
| | Low level input voltage | V _{ILT} | V _{SS} | — | 0.2xV _{DD} | V | | |
| | High level output voltage | V _{OHT} | I _{OH} = -3.0mA | V _{DD} -0.4 | — | — | | V |
| | Low level output voltage | V _{OLT} | I _{OL} = 3.0mA | — | — | V _{SS} +0.4 | | V |
| C M O S | High level input voltage | V _{IHC} | 0.8xV _{DD} | — | V _{DD} | V | SEL1, SEL2, YD, XD0 to XD3, XSCL, YDIS, LP, WF, CL0, XECL, YSCL | |
| | Low level input voltage | V _{ILC} | V _{SS} | — | 0.2xV _{DD} | V | | |
| | High level output voltage | V _{OHC} | I _{OH} = -1.0mA | V _{DD} -0.4 | — | — | | V |
| | Low level output voltage | V _{OLC} | I _{OL} = 1.0mA | — | — | V _{SS} +0.4 | | V |
| — | Positive trigger threshold voltage | V _{T+} | 0.5V _{DD} | 0.7V _{DD} | 0.8V _{DD} | V | RES | |
| | Negative trigger threshold voltage | V _{T-} | 0.2V _{DD} | 0.3V _{DD} | 0.5V _{DD} | V | | |
| Input leakage current | I _{LI} | V _{IN} = V _{DD} /V _{SS} | — | 0.05 | 2.0 | μA | | |
| Output leakage current | I _{LO} | | — | 0.10 | 5.0 | μA | | |
| Average operating current | I _{opr} | f _{osc} = 6.1MHz, No-load 256 × 200 dot | — | 3.5 (V _{DD} =3.5V) | 7.0 | mA | V _{DD} | |
| Standby current | I _q | Sleep XG, CS, RD = V _{DD} | — | 0.05 | 20 | μA | V _{DD} | |
| Oscillation frequency | f _{osc} | AT X'tal | 1.0 | — | 8.0 | MHz | XG, XD | |
| External clock frequency | f _{CL} | Duty 47.5% | 1.0 | — | 8.0 | MHz | | |
| Feed back resistance | R _f | | 0.7 | — | 4.0 | MΩ | | |

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- Timing Diagrams
 - 8080-Family Interface Timing



$T_a = -20$ to 75°C

| Signal | Symbol | Parameter | $V_{DD} = 4.5$ to 5.5V | | $V_{DD} = 2.7$ to 4.5V | | Unit | Condition |
|----------------------------|------------|------------------------------------|---------------------------------|-----|---------------------------------|-----|------|-------------|
| | | | min | max | min | max | | |
| A0, $\overline{\text{CS}}$ | t_{AH8} | Address hold time | 10 | — | 10 | — | ns | CL = 100 pF |
| | t_{AW8} | Address setup time | 0 | — | 0 | — | ns | |
| WR, $\overline{\text{RD}}$ | t_{CYC} | System cycle time | See note | — | See note | — | ns | |
| | t_{CC} | Strobe pulsewidth | 120 | — | 150 | — | ns | |
| D0 to D7 | t_{DS8} | Data setup time | 120 | — | 120 | — | ns | |
| | t_{DH8} | Data hold time | 5 | — | 5 | — | ns | |
| | t_{ACC8} | $\overline{\text{RD}}$ access time | — | 50 | — | 80 | ns | |
| | t_{OH8} | Output disable time | 10 | 50 | 10 | 55 | ns | |

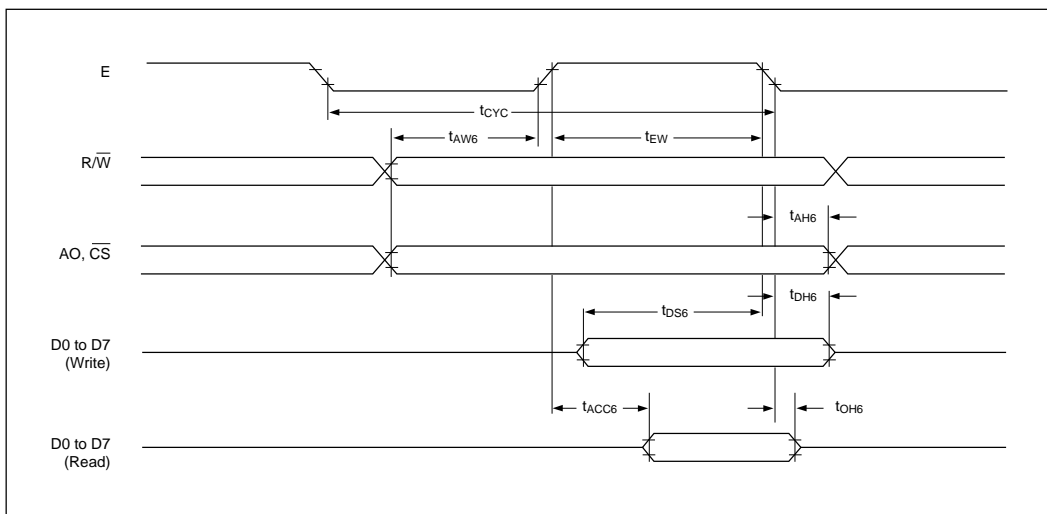
Note: For memory control and system control commands:

$$t_{CYC8} = 2t_c + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$$

For all other commands:

$$t_{CYC8} = 4t_c + t_{CC} + 30$$

o 6800-Family Interface Timing



Note: t_{CYC6} indicates the interval during which \overline{CS} is LOW and E is HIGH.

$T_a = -20$ to 75°C

| Signal | Symbol | Parameter | $V_{DD} = 4.5$ to 5.5V | | $V_{DD} = 2.7$ to 4.5V | | Unit | Condition |
|---------------------------|------------|---------------------|---------------------------------|-----|---------------------------------|-----|------|-------------|
| | | | min | max | min | max | | |
| A0, \overline{CS} , R/W | t_{CYC6} | System cycle time | See note | — | See note | — | ns | CL = 100 pF |
| | t_{AW6} | Address setup time | 0 | — | 10 | — | ns | |
| | t_{AH6} | Address hold time | 0 | — | 0 | — | ns | |
| D0 to D7 | t_{DS6} | Data setup time | 100 | — | 120 | — | ns | |
| | t_{DH6} | Data hold time | 0 | — | 0 | — | ns | |
| | t_{OH6} | Output disable time | 10 | 50 | 10 | 75 | ns | |
| | t_{ACC6} | Access time | — | 85 | — | 130 | ns | |
| E | t_{EW} | Enable pulsewidth | 120 | — | 150 | — | ns | |

Note: For memory control and system control commands:

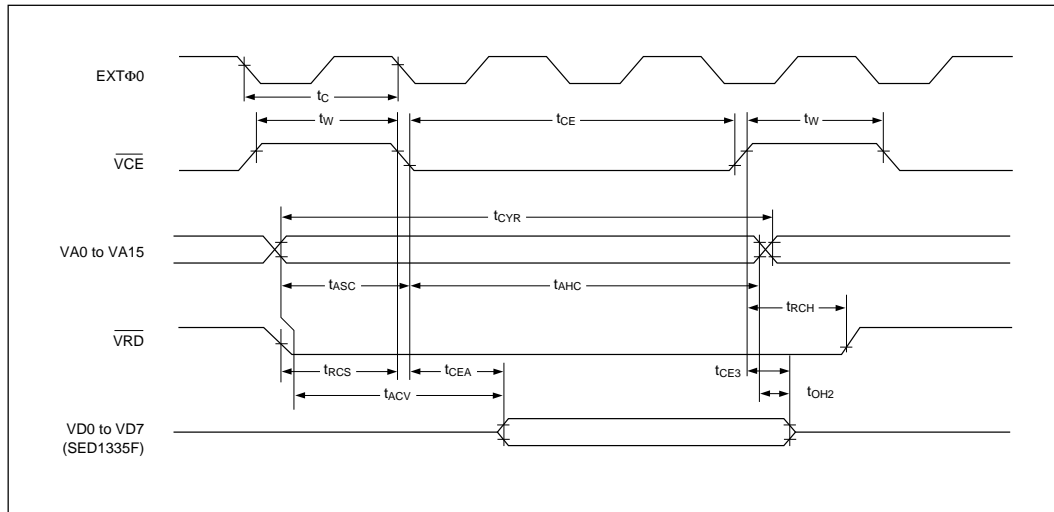
$$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$$

For all other commands:

$$t_{CYC6} = 4t_C + t_{EW} + 30$$

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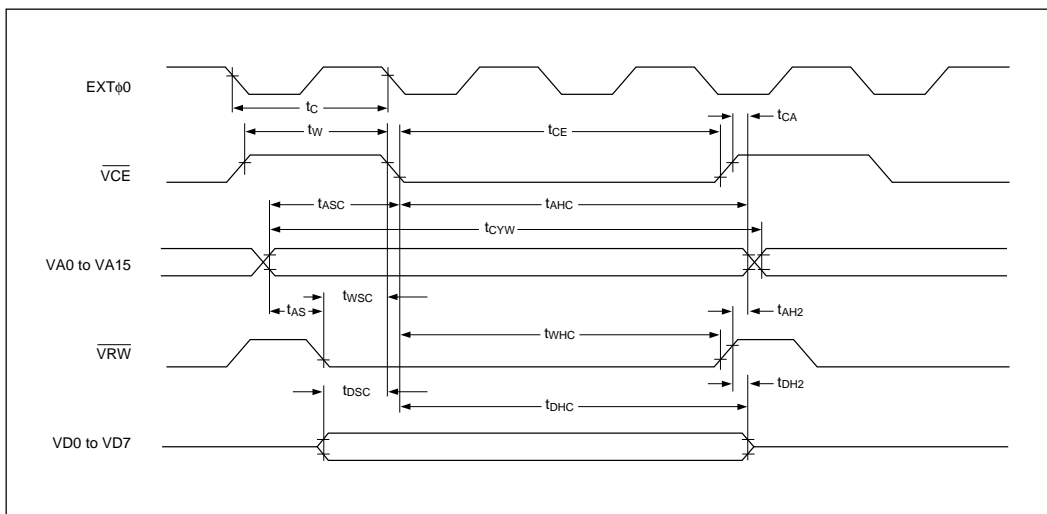
Display Memory Read Timing



$T_a = -20 \text{ to } 75^\circ\text{C}$

| Signal | Symbol | Parameter | $V_{DD} = 4.5 \text{ to } 5.5\text{V}$ | | $V_{DD} = 2.7 \text{ to } 4.5\text{V}$ | | Unit | Condition |
|------------------|-----------|---|--|--------------|--|--------------|------|-------------|
| | | | min | max | min | max | | |
| EXT ϕ_0 | t_c | Clock period | 100 | — | 125 | — | ns | CL = 100 pF |
| \overline{VCE} | t_w | \overline{VCE} HIGH-level pulsewidth | $t_c - 50$ | — | $t_c - 50$ | — | ns | |
| | t_{ce} | \overline{VCE} LOW-level pulsewidth | $2t_c - 30$ | — | $2t_c - 30$ | — | ns | |
| VA0 to VA15 | t_{CYR} | Read cycle time | $3t_c$ | — | $3t_c$ | — | ns | |
| | t_{ASC} | Address setup time to falling edge of \overline{VCE} | $t_c - 70$ | — | $t_c - 100$ | — | ns | |
| | t_{AHC} | Address hold time from falling edge of \overline{VCE} | $2t_c - 30$ | — | $2t_c - 40$ | — | ns | |
| \overline{VRD} | t_{RCS} | Read cycle setup time to falling edge of \overline{VCE} | $t_c - 45$ | — | $t_c - 60$ | — | ns | |
| | t_{RCH} | Read cycle hold time from rising edge of \overline{VCE} | $0.5t_c$ | — | $0.5t_c$ | — | ns | |
| VD0 to VD7 | t_{ACV} | Address access time | — | $3t_c - 100$ | — | $3t_c - 115$ | ns | |
| | t_{CEA} | \overline{VCE} access time | — | $2t_c - 80$ | — | $2t_c - 90$ | ns | |
| | t_{OH2} | Output data hold time | 0 | — | 0 | — | ns | |
| | t_{CE3} | \overline{VCE} to data off time | 0 | — | 0 | — | ns | |

o Display Memory Write Timing

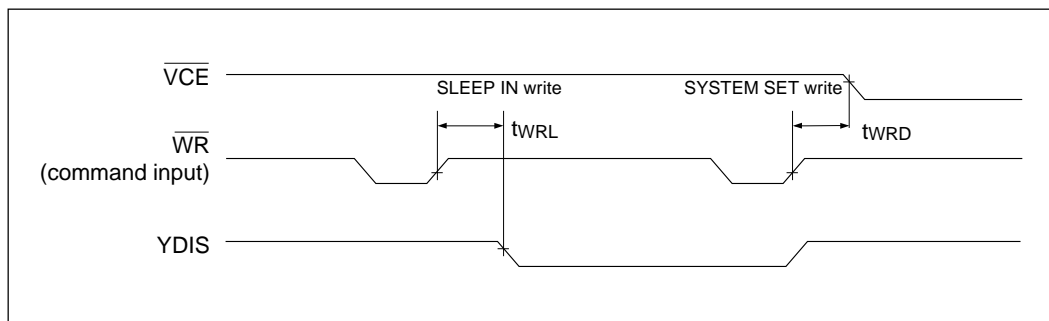


Ta = -20 to 75°C

| Signal | Symbol | Parameter | VDD = 4.5 to 5.5V | | VDD = 2.7 to 4.5V | | Unit | Condition |
|-------------|--------|---|-------------------|-----|-------------------|-----|------|-------------|
| | | | min | max | min | max | | |
| EXT φ0 | tc | Clock period | 100 | — | 125 | — | ns | CL = 100 pF |
| VCE | tw | VCE HIGH-level pulse-width | tc - 50 | — | tc - 50 | — | ns | |
| | tce | VCE LOW-level pulse-width | 2tc - 30 | — | 2tc - 30 | — | ns | |
| VA0 to VA15 | tcyw | Write cycle time | 3tc | — | 3tc | — | ns | |
| | tahc | Address hold time from falling edge of VCE | 2tc - 30 | — | 2tc - 40 | — | ns | |
| | tasc | Address setup time to falling edge of VCE | tc - 70 | — | tc - 110 | — | ns | |
| | tca | Address hold time from rising edge of VCE | 0 | — | 0 | — | ns | |
| | tas | Address setup time to falling edge of VWR | 0 | — | 0 | — | ns | |
| | tah2 | Address hold time from rising edge of VWR | 10 | — | 10 | — | ns | |
| VWR | tawc | Write setup time to falling edge of VCE | tc - 80 | — | tc - 115 | — | ns | |
| | tawh | Write hold time from falling edge of VCE | 2tc - 20 | — | 2tc - 20 | — | ns | |
| VD0 to VD7 | tdsc | Data input setup time to falling edge of VCE | tc - 85 | — | tc - 125 | — | ns | |
| | tdhc | Data input hold time from falling edge of VCE | 2tc - 30 | — | 2tc - 30 | — | ns | |
| | tdh2 | Data hold time from rising edge of VWR | 5 | 50 | 5 | 50 | ns | |

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

○ SLEEP IN Command Timing



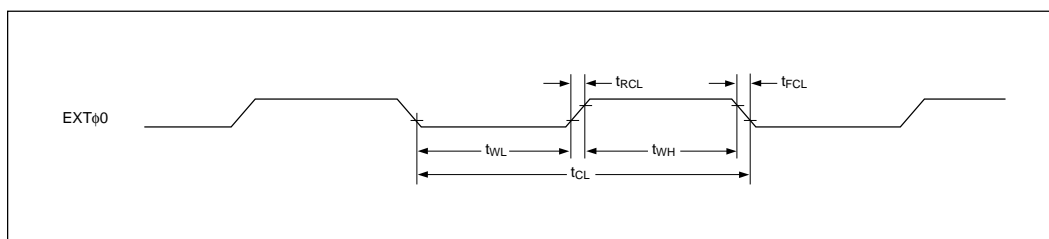
T_a = -20 to 75°C

| Signal | Symbol | Parameter | V _{DD} = 4.5 to 5.5V | | V _{DD} = 2.7 to 4.5V | | Unit | Condition |
|--------|--------|------------------------------|-------------------------------|-----|-------------------------------|-----|------|-------------|
| | | | min | max | min | max | | |
| WR | tWRD | VCE falling-edge delay time | *1 | — | *1 | — | ns | CL = 100 pF |
| | tWRL | YDIS falling-edge delay time | — | *2 | — | *2 | ns | |

Notes:

1. tWRD = 18tc + toss + 40 (toss is the time delay from the sleep state until stable operation)
2. tWRL = 36tc × [TC/R] × [L/F] + 70

● External Oscillator Signal Timing



T_a = -20 to 75°C

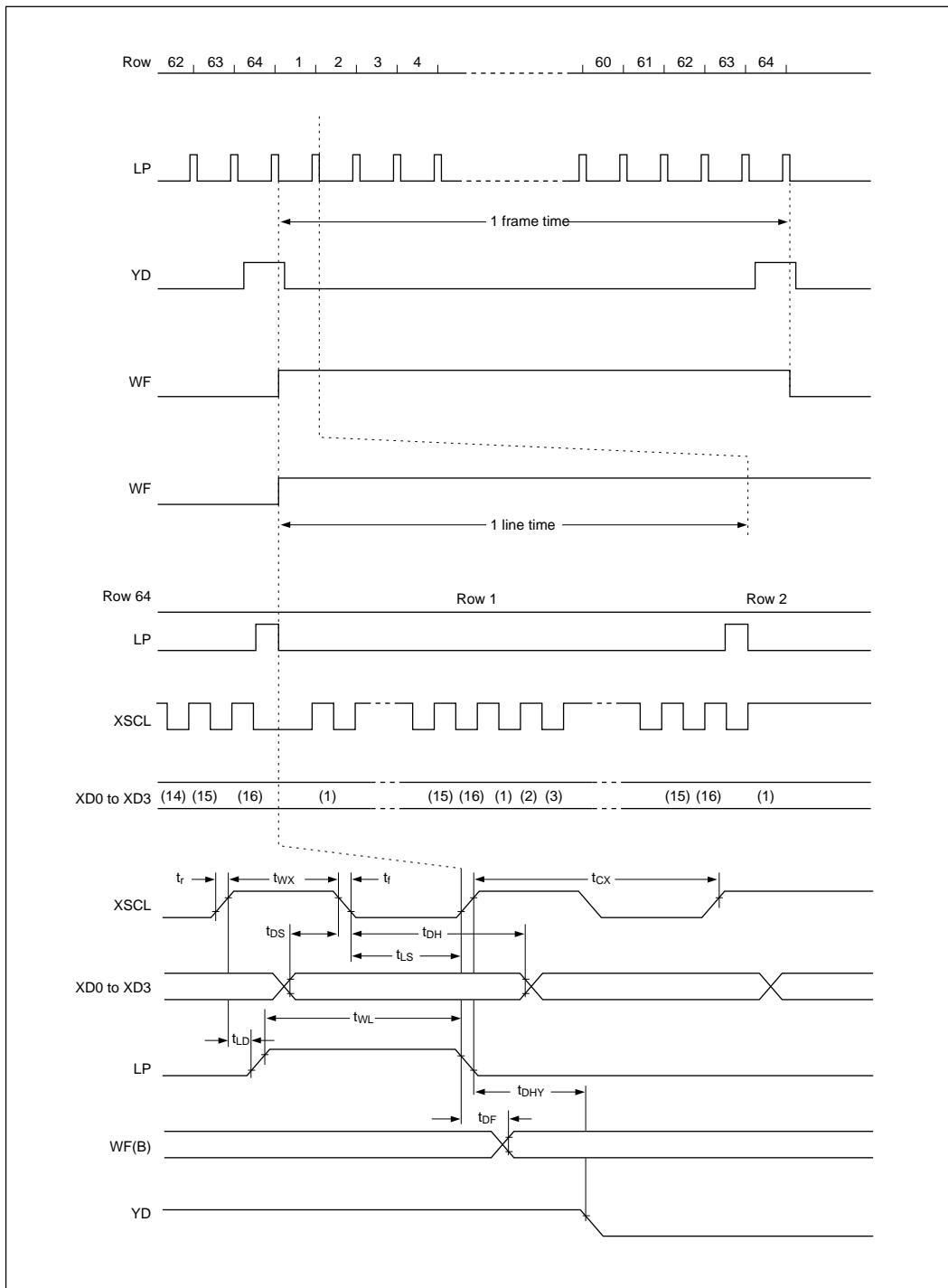
| Signal | Symbol | Parameter | V _{DD} = 4.5 to 5.5V | | V _{DD} = 2.7 to 4.5V | | Unit | Condition |
|--------|--------|--------------------------------------|-------------------------------|-----|-------------------------------|-----|------|-----------|
| | | | min | max | min | max | | |
| EXT φ0 | tRCL | External clock rise time | — | 15 | — | 15 | ns | |
| | tFCL | External clock fall time | — | 15 | — | 15 | ns | |
| | tWH | External clock HIGH-level pulsewidth | *1 | *2 | *1 | *2 | ns | |
| | tWL | External clock LOW-level pulsewidth | *1 | *2 | *1 | *2 | ns | |
| | tc | External clock period | 100 | — | 125 | — | ns | |

Notes:

1. $(tc - t_{RCL} - t_{FCL}) \times \frac{475}{1000} < t_{WH}, t_{WL}$
2. $(tc - t_{RCL} - t_{FCL}) \times \frac{525}{1000} > t_{WH}, t_{WL}$

o **LCD Output Timing**

The following characteristics are for a 1/64 duty cycle.

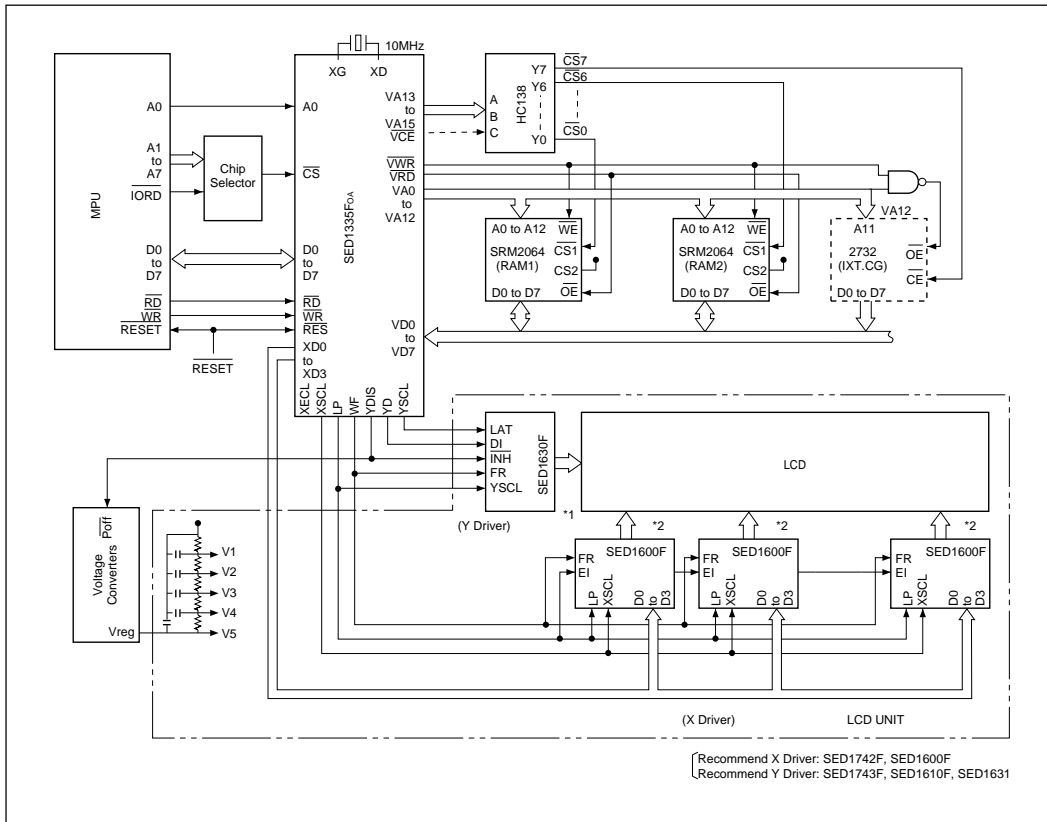


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 $T_a = -20 \text{ to } 75^\circ\text{C}$

| Signal | Symbol | Parameter | V _{DD} = 4.5 to 5.5V | | V _{DD} = 2.7 to 4.5V | | Unit | Condition |
|------------|----------------|-------------------------|-------------------------------|-----|-------------------------------|-----|------|------------|
| | | | min | max | min | max | | |
| | t _r | Rise time | — | 30 | — | 40 | ns | CL = 100pF |
| | t _f | Fall time | — | 30 | — | 40 | ns | |
| XSCL | tcX | Shift clock cycle time | 4tc | — | 4tc | — | ns | |
| | twX | XSCL clock pulsewidth | 2tc – 60 | — | 2tc – 60 | — | ns | |
| XD0 to XD3 | tdH | X data hold time | 2tc – 50 | — | 2tc – 50 | — | ns | |
| | tDS | X data setup time | 2tc – 100 | — | 2tc – 105 | — | ns | |
| LP | tLS | Latch data setup time | 2tc – 50 | — | 2tc – 50 | — | ns | |
| | tWL | LP pulsewidth | 4tc – 80 | — | 4tc – 120 | — | ns | |
| | tLD | LP delay time from XSCL | 0 | — | 0 | — | ns | |
| WF | tDF | Permitted WF delay | — | 50 | — | 50 | ns | |
| YD | tdHY | Y data hold time | 2tc – 20 | — | 2tc – 20 | — | ns | |

Note: The SED1335F reads display memory data from the address of the top left corner of the display screen, then scans horizontally until it reaches the address for the bottom right corner of the display screen. Therefore, each line of X-driver data is sent starting from the left side of the display line.

■ EXAMPLE OF APPLICATION



■ CHARACTER CODE TABLE (Built-in Character Generator)

| | | Lower 4-bit (D0 to D3) of Character Code (Hexadecimal) | | | | | | | | | | | | | | | |
|---|---|--|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| Higher 4-bit (D4 to D7) of Character Code (Hexadecimal) | 2 | | ! | " | # | \$ | % | & | ' | (|) | * | + | , | - | . | / |
| | 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : | ; | < | = | > | ? |
| | 4 | @ | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O |
| | 5 | P | Q | R | S | T | U | V | W | X | Y | Z | [| \ |] | ^ | _ |
| | 6 | ` | a | b | c | d | e | f | g | h | i | j | k | l | m | n | o |
| | 7 | p | q | r | s | t | u | v | w | x | y | z | { | | } | ~ | |
| | A | | ^ | _ | ` | a | b | c | d | e | f | g | h | i | j | k | l |
| | B | | ~ | { | | } | ~ | { | | } | ~ | { | | } | ~ | { | |
| | C | | ~ | { | | } | ~ | { | | } | ~ | { | | } | ~ | { | |
| | D | | ~ | { | | } | ~ | { | | } | ~ | { | | } | ~ | { | |
| | 1 | | | | | | | | | | | | | | | | |