EPSON

SED1335F

Graphic LCD Controller

Wide Voltage Operation Products

- **For Medium-scale LCD**
- **Wide Operating Voltage 2.7 to 5.0V**
- **On Chip Character Generator ROM**

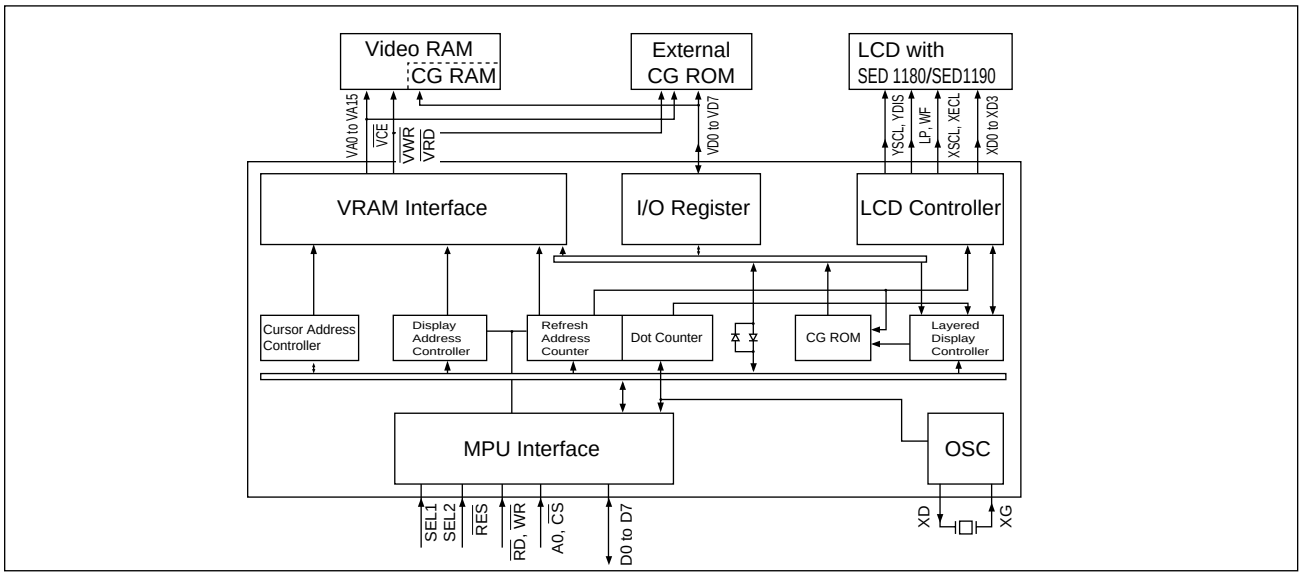
■ DESCRIPTION

The SED1335F is a graphics and character display controller for use with medium scale dot matrix LCDs.
The SED1335F generates all the signals required by the display memory and LCD drivers, and incorporates a character generator ROM, so that flexible, low power, display systems can be designed with a minimum number of external components.
The SED1335F's high speed MPU interface can be configured for both 6800 family and 8080 family processors, and the rich command set allows the user to create a layered display of characters and graphics, scroll the display, and assign display attributes to selected areas of the screen with a minimum of MPU intervention.
The controller also functions as a pipline buffer between the MPU and display memory so that low cost, medium speed SRAM can be used.
The SED1335F character generator system supports user defined characters, which can be used alone, or in conjunction with the on board character set.

■ FEATURES

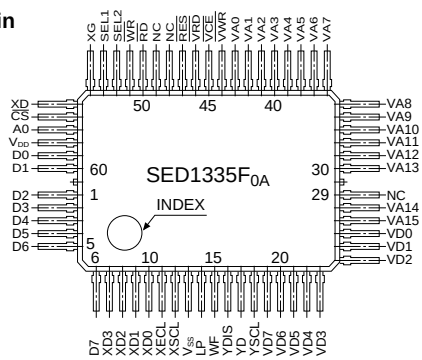
- 6800 and 8080 family compatibility, 2-pin programmable
- Software compatible with SED1330 and SED1336
- Programmable cursor movement
- Flexible scrolling
  ....Scrolling in both horizontal and vertical directions
  ....Scrolling of selected areas of the display
- Multimode display
  ....Up to 2 layers of mixed character and graphics
  ....Up to 3 layers of graphics
- Selectable display synthesis
  ....Display attributes (reverse video, flashing, etc.)for selected areas of the display
  ....Simple animation
- Supports 64K bytes of memory
  ....4K bytes of user definable characters
  ....60K bytes of display memory
- 160 JIS 5×7 pixel characters internal
- Supports external character ROM or RAM
  ....8×8 or 8×16 pixel characters
  ....Allows mixing of ROM RAM character sets
- Variable LCD duty cycle, from 1/2 to 1/256
- Low power CMOS fabrication
  ....5mA (typical)
  ....0.05μA(typical), standby
- Supply voltage 2.7 to 5.5V
- Package ..SED1335F$_{OA}$: QFP5-60pin (plastic)
  SED1335F$_{OB}$: QFP6-60pin (plastic)

■ BLOCK DIAGRAM

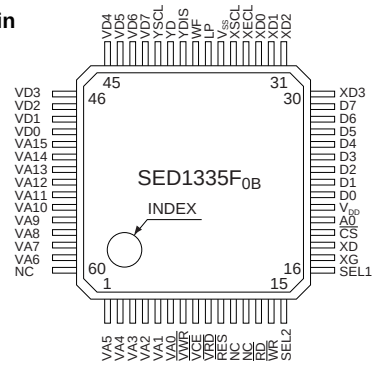


■ PIN CONFIGURATION

QFP5-60pin



QFP6-60pin



■ PIN DESCRIPTION

Pin Name	PIn No.		I/O	Function
	SED1335F$_{0A}$	SED1335F$_{0B}$		
XG	54	17	I	Oscillator terminal
XD	55	18	O	Oscillator terminal
V_{DD}	58	21	+5V	Power supply
V_{SS}	13	36	GND(0V)	Power supply
SEL1, 2	53•52	16•15	I	MPU interface format selection
D0 to D7	59 to 60 1 to 6	22 to 29	I/O	Data bus
A0	57	20	I	Data type selection
$\overline{RD}$	50	13	I	80 series Read strobe signal 68 series "E" clock
$\overline{WR}$	51	14	I	80 series Write strobe signal 68 series R/$\overline{W}$ signal
$\overline{CS}$	56	19	I	Chip select
$\overline{RES}$	47	10	I	Reset
VA15 to VA0	27•28 30 to 43	1 to 6 50 to 59	O	VRAM address bus
VD7 to VD0	19 to 26	42 to 49	I/O	VRAM data bus

Pin Name	Pin No.		I/O	Function
	SED1335F$_{0A}$	SED1335F$_{0B}$		
$\overline{VWR}$	44	7	O	VRAM write signal
$\overline{VRD}$	46	9	O	VRAM read signal
$\overline{VCE}$	45	8	O	VRAM chip enable
XD3 to XD0	7 to 10	30 to 33	O	Dot data output bus to X driver
XSCL	12	35	O	Dot data shift clock for X driver
XECL	11	34	O	Chip enable shift clock for X driver
LP	14	37	O	Dot data latch pulse
WF	15	38	O	Frame signal
YSCL	18	41	O	Scan data shift clock for Y driver
YD	17	40	O	Scan data output
YDIS	16	39	O	Power down signal when display OFF

NC : Non Connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 7.0	V
Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–60 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics (1)

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, Ta = –20 to 75°C)

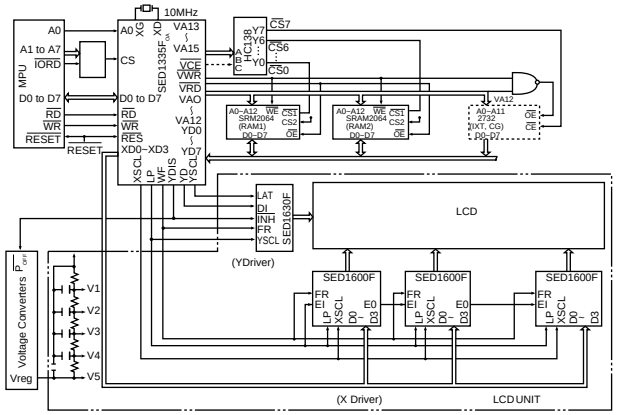
Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin
Operating voltage		V_{DD}		4.5	—	5.5	V	V_{DD}
Register data retention voltage		V_{OH}		2.0	—	6.0	V	
TTL	High level input voltage	V_{IHT}		0.5×$_{DD}$	—	V_{DD}	V	D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, VA0 to VA15, $\overline{VCE}$ $\overline{VRD}$, $\overline{VWR}$
	Low level input voltage	V_{ILT}		V_{SS}	—	0.2×V_{DD}	V	
	High level output voltage	V_{OHT}	I_{OH} = –5.0mA	2.4	—	—	V	
	Low level output voltage	V_{OLT}	I_{OL} = 5.0mA	—	—	V_{SS}+0.4	V	
CMOS	High level input voltage	V_{IHC}		0.8×V_{DD}	—	V_{DD}	V	SEL1, SEL2, YD, XD0 to XD3, XSCL, YDIS, LP, WF, CL0, XECL, YSCL
	Low level input voltage	V_{ILC}		V_{SS}	—	0.2×V_{DD}	V	
	High level output voltage	V_{OHC}	I_{OH} = –2.0mA	V_{DD}—0.4	—	—	V	
	Low level output voltage	V_{OLC}	I_{OL} = 2.0mA	—	—	V_{SS}+0.4	V	
Schmitt	Positive trigger threshold voltage	V_{T+}		0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V	$\overline{RES}$
	Negative trigger threshold voltage	V_{T-}		0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V	
Input leakage current		I_{LI}	V_{IN} = V_{DD}/V_{SS}	—	0.05	2.0	µA	
Output leakage current		I_{LO}		—	0.10	5.0	µA	
Average operating current		I_{opr}	f_{OSC} = 10MHz, No-load 256×200dot	—	11	15	mA	V_{DD}
Standby current		I_Q	Sleep X_G, $\overline{CS}$, $\overline{RD}$ = V_{DD}	—	0.05	20	µA	V_{DD}
Oscillation frequency		f_{OSC}	AT X'tal	1.0	—	10.0	MHz	XG, XD
External clock frequency		f_{CL}	Duty 47.5%	1.0	—	10.0	MHz	
Feed back resistance		R_f		0.5	1.0	3.0	MΩ	

● DC Electrical Characteristics (2)

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, Ta = –20 to 75°C)

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin
Operating voltage		V_{DD}		2.7	3.5	4.5	V	V_{DD}
Register data retention voltage		V_{OH}		2.0	—	6.0	V	
TTL	High level input voltage	V_{IHT}		0.8×V_{DD}	—	V_{DD}	V	D0 to D7 A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ VD0 to VD7 VA0 to VA15, $\overline{VCE}$,$\overline{VRD}$, $\overline{VWR}$
	Low level input voltage	V_{ILT}		V_{SS}	—	0.2×V_{DD}	V	
	High level output voltage	V_{OHT}	I_{OH} = –3.0mA	V_{DD}—0.4	—	—	V	
	Low level output voltage	V_{OLT}	I_{OL} = 3.0mA	—	—	V_{SS}+0.4	V	
CMOS	High level input voltage	V_{IHC}		0.8×V_{DD}	—	V_{DD}	V	SEL1, SEL2, YD XD0 to XD3, XSCL, YDIS LP, WF, CL0, XECL, YSCL
	Low level input voltage	V_{ILC}		V_{SS}	—	0.2×V_{DD}	V	
	High level output voltage	V_{OHC}	I_{OH} = –1.0mA	V_{DD}—0.4	—	—	V	
	Low level output voltage	V_{OLC}	I_{OL} = 1.0mA	—	—	V_{SS}+0.4	V	
Schmitt	Positive trigger threshold voltage	V_{T+}		0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V	$\overline{RES}$
	Negative trigger threshold voltage	V_{T-}		0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V	
Input leakage current		I_{LI}	V_{IN} = V_{DD}/V_{SS}	—	0.05	2.0	µA	
Output leakage current		I_{LO}		—	0.10	5.0	µA	
Average operating current		I_{opr}	f_{OSC} = 6.1MHz, No-load 256×200dot	—	3.5 V_{DD} = 3.5V	7.0	mA	V_{DD}
Standby current		I_Q	Sleep X_G, $\overline{CS}$, $\overline{RD}$ = V_{DD}	—	0.05	20	µA	V_{DD}
Oscillation frequency		f_{OSC}	AT X'tal	1.0	—	8.0	MHz	XG, XD
External clock frequency		f_{CL}	Duty 47.5%	1.0	—	8.0	MHz	
Feed back resistance		R_f		0.7	1.0	4.0	MΩ	

■ MPU AND LCD PANEL CONNECTION EXAMPLE

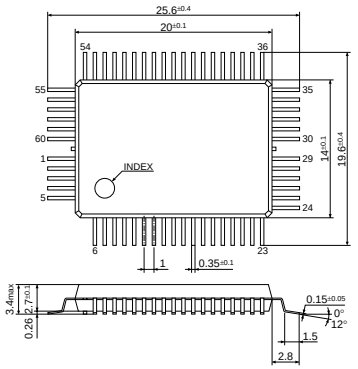


Recommend X Driver: SED1742F, SED1600F
Recommend Y Driver: SED1743F, SED1610F, SED1631

■ PACKAGE DIMENSIONS

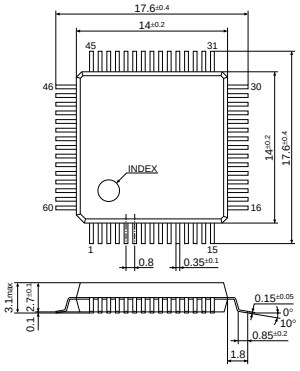
● SED1335F$_{OA}$

Plastic QFP5-60pin

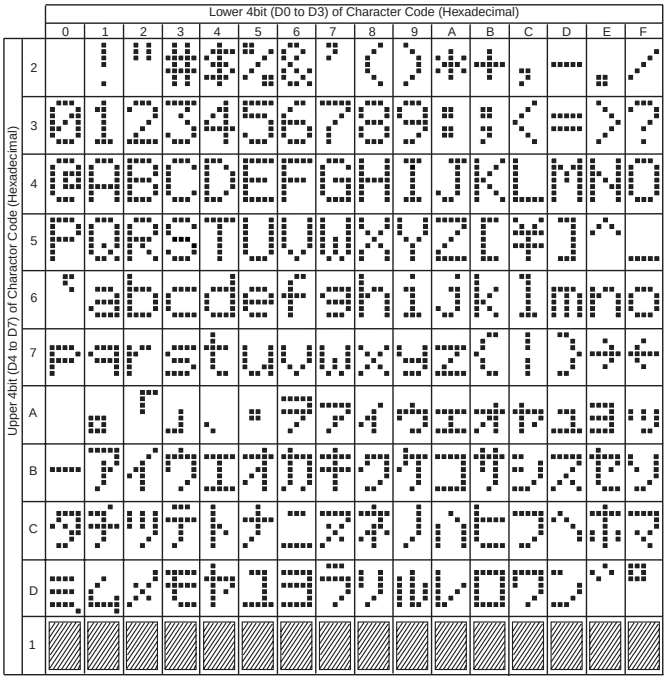


● SED1335F$_{OB}$

Plastic QFP6-60pin



■ CHARACTER CODE TABLE (BUILT-IN CHARACTER GENERATOR)



Note : ▨ means all dots of 6×8 matrix are on.

NOTICE

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