1. SED1510 Series

Contents

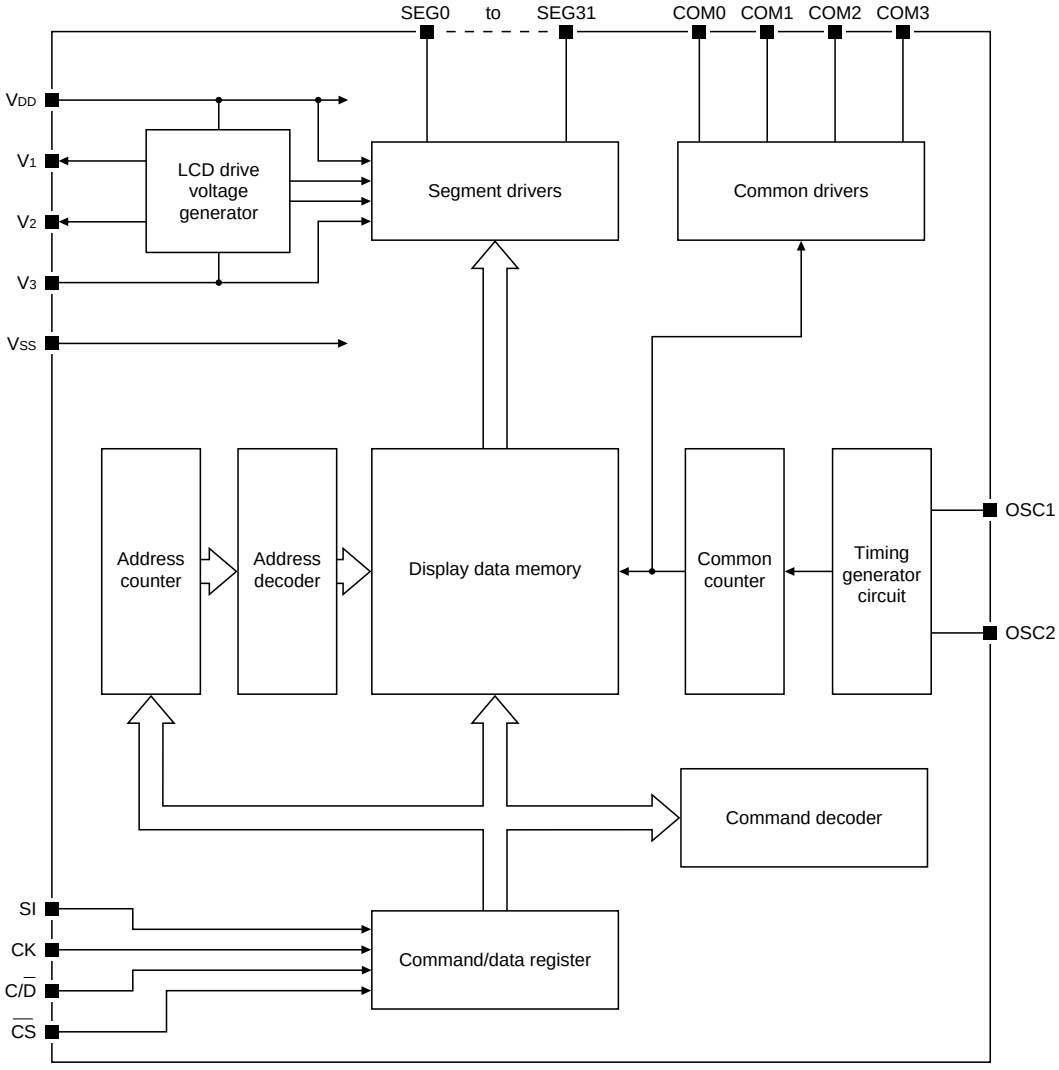
OVERVIEW

The SED1510Series is a segment driver IC for 1/4-duty LCD panels. It features 150 µW maximum power dissipation and a wide operating supply voltage range, making it ideal for use in battery-powered devices. The SED1510 series incorporates an LCD driving power circuit and allows simple configuration of the interface with a microcomputer, achieving a handy type unit at low cost.

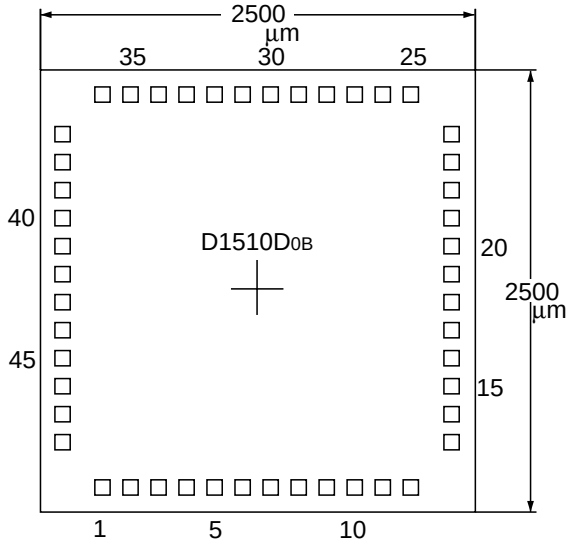
FEATURES

- 1/4-duty LCD segment driver
- 150 µW maximum power dissipation
- Serial data interface
- 128 bits of display data RAM
- On-chip oscillator
- LCD drive voltage generator
- Four common driver outputs
- 32 segment driver outputs
- 0.9 to 6.0 V supply for logic circuitry operation
- 1.8 to 6.0 V supply for LCD driver operation
- Series specification
  SED1510 D0C : chip (Al pad)
  SED1510 F0C : QFP12-48pin

BLOCK DIAGRAM

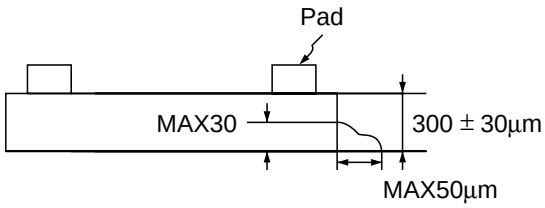


PAD LAYOUT AND COORDINATES (SED1510D0C)

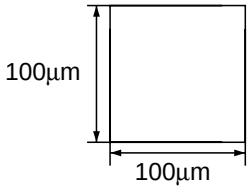


Chip size: 2500µm × 2500µm
Chip pitch: 525µm

Sectional dimensions



Size of pad opening



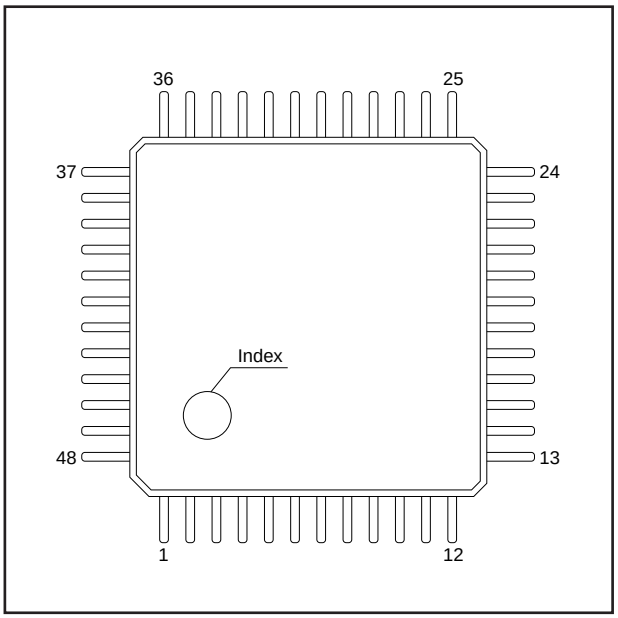
Pad coordinates

Unit: µm

No.	Pin name	X coordinate	Y coordinate	No.	Pin name	X coordinate	Y coordinate
1	OSC1	-898	-1091	25	SEG 8	898	1091
2	OSC2	-738	-1091	26	SEG 9	738	1091
3	V1	-578	-1091	27	SEG 10	578	1091
4	V2	-418	-1091	28	SEG 11	418	1091
5	V3	-258	-1091	29	SEG 12	258	1091
6	V_{SS}	-98	-1091	30	SEG 13	98	1091
7	V_{DD}	63	-1091	31	SEG 14	-63	1091
8	CK	223	-1091	32	SEG 15	-223	1091
9	$\overline{SI}$	383	-1091	33	SEG 16	-383	1091
10	$\overline{CS}$	543	-1091	34	SEG 17	-543	1091
11	C/$\overline{D}$	703	-1091	35	SEG 18	-703	1091
12	COM0	863	-1091	36	SEG 19	-863	1091
13	COM1	1091	-898	37	SEG 20	-1091	898
14	COM2	1091	-738	38	SEG 21	-1091	738
15	COM3	1091	-578	39	SEG 22	-1091	578
16	V_{REG}	1091	-418	40	SEG 23	-1091	418
17	SEG 0	1091	-258	41	SEG 24	-1091	258
18	SEG 1	1091	-98	42	SEG 25	-1091	98
19	SEG 2	1091	63	43	SEG 26	-1091	-63
20	SEG 3	1091	224	44	SEG 27	-1091	-223
21	SEG 4	1091	383	45	SEG 28	-1091	-383
22	SEG 5	1091	543	46	SEG 29	-1091	-543
23	SEG 6	1091	703	47	SEG 30	-1091	-703
24	SEG 7	1091	863	48	SEG 31	-1091	-863

Origin: Center of the chip
Chip size: 2,500 × 2,500

PINOUT (SED1510F0C)



No.	Name	No.	Name	No.	Name
1	OSC1	17	SEG0	33	SEG16
2	OSC2	18	SEG1	34	SEG17
3	V_1	19	SEG2	35	SEG18
4	V_2	20	SEG3	36	SEG19
5	V_3	21	SEG4	37	SEG20
6	V_{SS}	22	SEG5	38	SEG21
7	V_{DD}	23	SEG6	39	SEG22
8	CK	24	SEG7	40	SEG23
9	SI	25	SEG8	41	SEG24
10	$\overline{CS}$	26	SEG9	42	SEG25
11	C/$\overline{D}$	27	SEG10	43	SEG26
12	COM0	28	SEG11	44	SEG27
13	COM1	29	SEG12	45	SEG28
14	COM2	30	SEG13	46	SEG29
15	COM3	31	SEG14	47	SEG30
16	V_{REG}	32	SEG15	48	SEG31

PIN DESCRIPTION

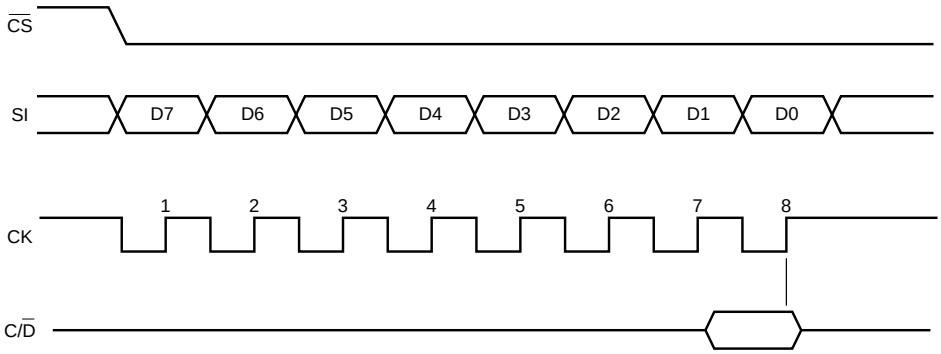
Pin Name	I/O	Description	Q'ty
V_{DD}	Power supply	Plus power terminal. Common to the microcomputer power terminal V_{CC}.	1
V_{SS}	Power supply	Minus power supply. A 0V terminal to be connected to the system GND.	1
V_1 V_2	O	Power level monitor terminal for liquid crystal drive. The levels $V_1 = 1/3 \times V_3$ and $V_2 = 2/3 \times V_3$ are generated from the inside of SED1510F0C.	2
V_3	Power supply	Power terminal for liquid crystal drive. Potential relations: $V_{DD} > V_3$.	1
SI	I	Serial data input. Input of display data and of commands to control operation of SED1510F0C. When display data is input, the relations between display data input and segment ON/OFF are as follows: SI input "0" $\rightarrow$ OFF, SI input "1" $\rightarrow$ ON	1
CK	I	Shift clock input of serial data (SI input). SI input data is read bit by bit in the serial register at the CK input leading edge.	1
C/$\overline{D}$	I	Identification of SI input as data or command (in case of SED1510F0C only). The "L" level indicates data, and the "H" level does commands.	1
$\overline{CS}$	I	Chip select signal input (in case of SED1510F0C only). When $\overline{CS}$ input is changed from the "H" level to the "L" level, SED1510F0C can accept SI inputs. The CK counter is set to the initial state when the $\overline{CS}$ input is changed from the "H" level to the "L" level.	1
OSC1 OSC2	I O	Oscillation resistance connection terminal	2
SEG0 to SEG31	O	Segment signal for liquid crystal drive	32
COM0 to COM3	O	Common signal for liquid crystal drive	4
V_{REG}	O	Test terminal. Keep it open.	1

Total 48

FUNCTIONAL DESCRIPTION

Command/Data Register

◊ The command/data register consists of an 8-bit serial register and a 3-bit CK counter.
◊ When $\overline{CS}$ input changes from the "H" level to the "L" level, SED1510 comes to accept SI inputs. Also, the CK counter is initialized when $\overline{CS}$ input changes from the "H" level to the "L" level. SED1510 always accepts SI inputs. When the built-in timing generator (CR oscillator) starts oscillating, the CK counter is initialized.
◊ The serial register takes in serial data D7, D6, ... D0 in this order from the SI terminal on the rising edge of the CK. At the same time, the CK counter starts counting the serial clock. The CK counter, when counting 8 on the serial clock, returns to the initial state.
◊ So, serial data is taken in to the serial register in 8 bits and is processed.
◊ When the CK counter counts 8 of shift clock input (CK input) (reads the input 8-bit serial data), the serial data taken in the command/data register is output to the display data memory (RAM) if the input serial data is a display data, or is output to the command decoder if it is a command data.
◊ SED1510 identifies input serial data (SI input) as display data or command data judging from C/$\overline{D}$ input. It displays display data when C/$\overline{D}$ input is "L" level or command data when the input is "H" level.
◊ SED1510 reads and identifies C/$\overline{D}$ input at the timing on the rising edge of 8xn of shift clock input (CK input) from the $\overline{CS}$ = "L" level. (n=1, 2, 3, ...)

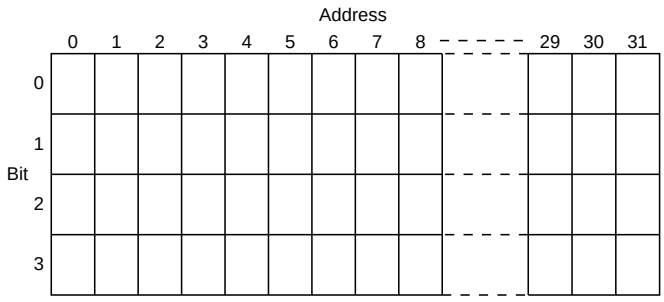


Command Decoder

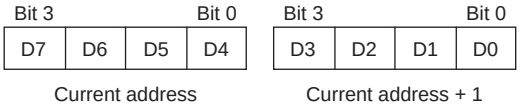
◊ When the command/data register data specifies any command (when C/$\overline{D}$ input is "H" level when serial data is input), the command decoder takes in and decode the data of the command/data register to control SED1510F0C.

Display Data Memory

The format of the 32 × 4-bit memory is shown in the following figure.



Each 8-bit display data byte loaded from the command/data register is stored in two consecutive addresses as shown in the following figure. The upper four bits are stored at the location specified by the address counter, and the lower four bits, at the next location. The address counter is automatically incremented by two.



A single 4-bit word can be written to memory using the Data Memory Write command as shown in the following figure. The lower four bits are stored at the location specified by the address counter. The address counter is automatically incremented by one.

1	0	0	X	D3	D2	D1	D0

Bit 3 Bit 0

D3	D2	D1	D0

Address = n

Note

× = don't care

◊ The display data memory address is automatically incremented by 2 when a 8-bit display data (C/$\overline{D}$ = "L" level) is stored, or incremented by 1 when a 4-bit data is stored by the display data re-write command.

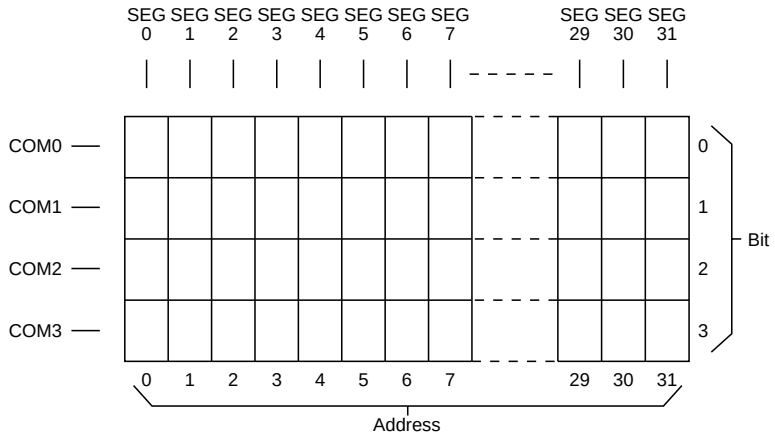
◊ After the display data is written in the RAM, the RAM address is held as shown below unless the address is reset:

After writing a 8-bit display data ...
the final write address is incremented by 2.

After rewriting a 4-bit display data ...
the final rewrite address is incremented by 1.

◊ Data in the display data memory synchronizes with the COM0 to COM3 signals and is output in 32 bits to the segment driver.

The relations of the display data memory, the segment terminal and common signal selection timing are as follows:



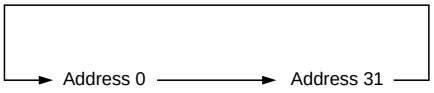
Address Counter

◊ The address counter is a presettable type to give 5-bit addresses to the display data memory.

◊ In case of SED1510, any address can be set when the address set command is used.

◊ In case of SED1510, set addresses are automatically incremented by 2 when an 8-bit display data is stored (C/$\overline{D}$ = "L" level), or incremented by 1 when a 4-bit data is stored by the display data memory rewrite command.

◊ The address decoder, after counting Address 31, counts 0 at the next counting and repeats as follows:

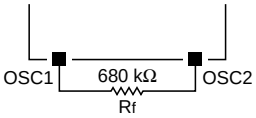


Address Decoder

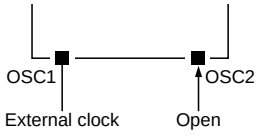
The address decoder sets addresses 0 to 31 of the display data memory where the display data of address counter is written.

Timing Generator

A low-power oscillator can be constructed using an external feedback resistor as shown in the following figure.



Alternatively, an 18 kHz external clock can be input on OSC1, and OSC2 left open, as shown in the following figure.

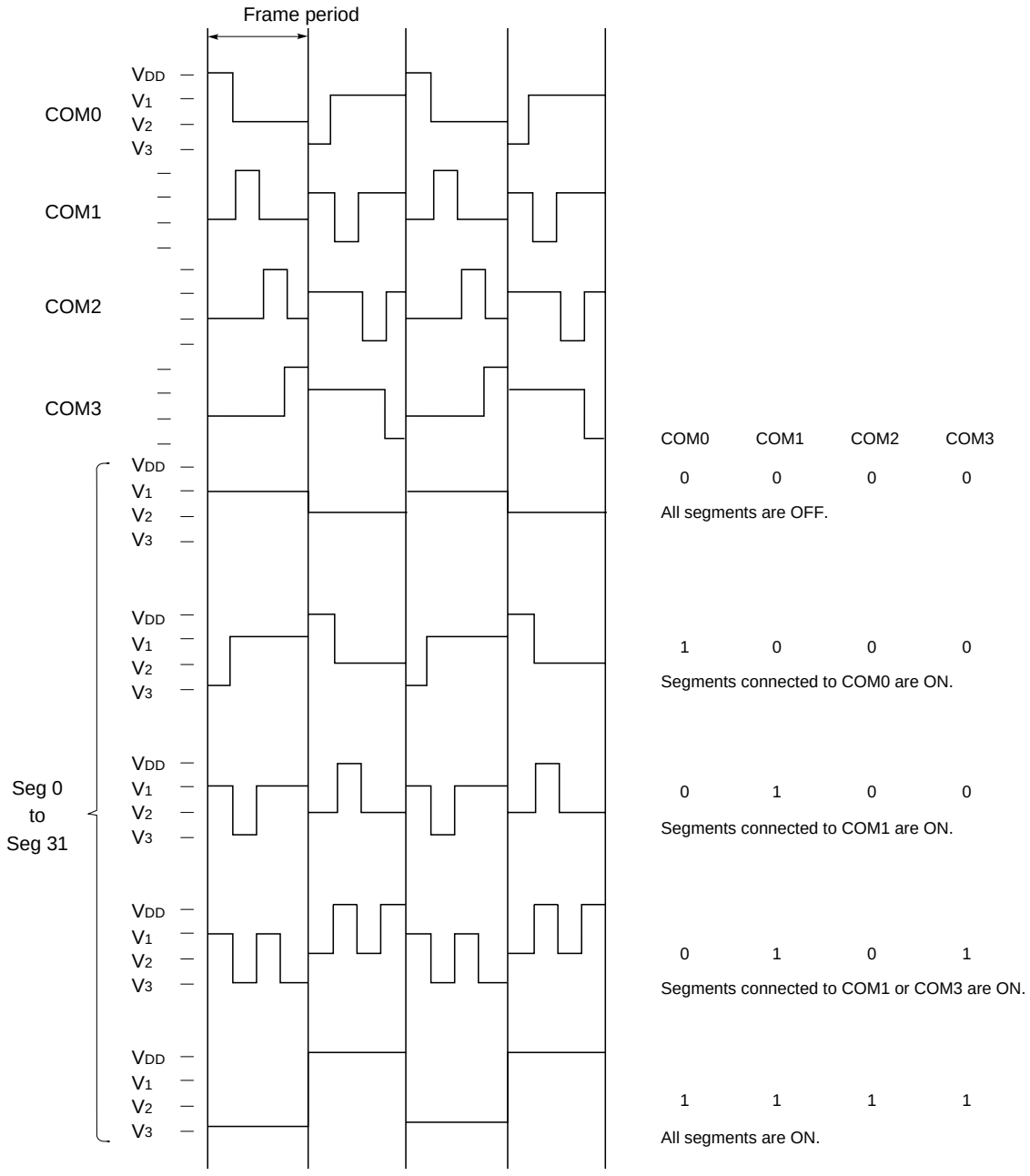


Common Counter

The timing generator clock signal is frequency-divided by the common counter to generate both the common drive timing and the alternating frame timing.

Segment and Common Drivers

The 32 segment drivers and the four common drivers are 4-level outputs that switch between V_{DD} and the V1, V2 and V3 LCD driver voltage levels.
The output states are determined by the display data values and the common counter as shown in the following figure. The outputs are used to drive a 1/3-bias, 1/4-duty LCD panel.



Commands

The SED1510F0C samples C/$\overline{D}$ on every eighth rising edge of CK. If C/$\overline{D}$ is HIGH, the command/data register contents are latched into the command decoder. The command decoder executes the following six commands.

Address Set

Set the address counter to the value specified by D0 to D4.

0	0	0	D4	D3	D2	D1	D0

Addresses are incremented by 2 each time a display data (8-bit) is input. The relations between D4 to D0 and addresses are as follows:

D4	D3	D2	D1	D0	Address
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

Display ON

Turn all LCD segments ON. The display memory data is not affected.

0	0	1	×	×	×	×	×

Note: × = don't care

Display OFF

Turn all LCD segments OFF. The display memory data is not affected.

0	1	0	×	×	×	×	×

Note: × = don't care

Display Start

Return to normal display mode. The display memory data is output to the display.

0	1	1	×	×	×	×	×

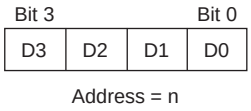
Note: × = don't care

Memory Write

Store the data D0 to D3 at the location specified by the address counter. The address counter is automatically incremented by one. The other display memory locations are not affected.

1	0	0	×	D3	D2	D1	D0

Data are allocated to each bit of the display data memory as follows:



Note: × = don't care

Reset

Reset the SED1510FOC. The SED1510FOC then enters normal operating mode, and the display turns OFF.

1	1	0	×	×	×	×	×

Note: × = don't care

APPLICATION NOTE

Supply Voltages

In addition to V_{DD}, there are three LCD supply voltages: V_1, V_2 and V_3. V_3 is supplied externally, whereas V_1 and V_2 are generated internally. V_1, V_2 and V_3 are given by the following equations.

$V_1 = V_{DD} - 1/3V_{LCD}$

$V_2 = V_{DD} - 2/3V_{LCD}$

$V_3 = V_{DD} - V_{LCD}$

where V_{LCD} is the LCD drive voltage. The voltages must be such that

$V_{DD} \geq V_1 \geq V_2 \geq V_3$

LCD supply voltage connections when the LCD drive supply is connected to V_{SS} are shown in figure 1, and the connections when the drive supply is independent of V_{SS}, in Figure 2.

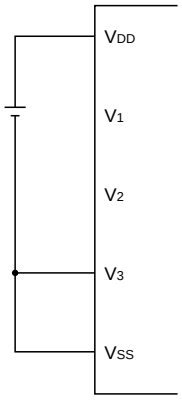


Figure 1. LCD drive supply connected to V_{SS}

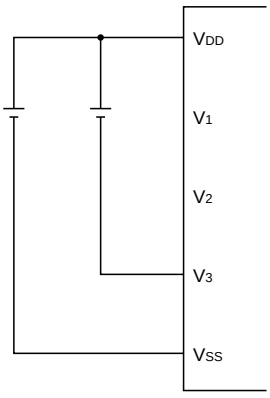
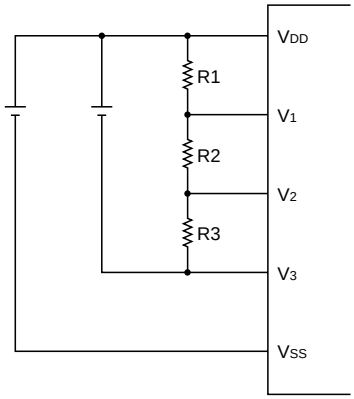


Figure 2. LCD drive supply not connected to V_{SS}

When there is a lot of distortion in the LCD drive waveforms, connect bleeder resistors as shown in the following figure.



SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{SS}	–7.0 to 0.3	V
LCD supply voltage range	V_3	–7.0 to 0.3	V
Input voltage range	V_I	V_{SS} –0.3 to 0.3	V
Output voltage range	V_O	V_{SS} –0.3 to 0.3	V
Power dissipation	P_D	250	mW
Operating temperature range	T_{opg}	–20 to 75	deg.C
Storage temperature range	T_{stg}	–65 to 150	deg.C
Soldering temperature (10 sec at leads)	T_{sol}	260	deg.C
Heat resistance		400 • 10	°C•Min

Note: All voltages shown are specified on a V_{DD} = 0 V basis.

DC Electrical Characteristics

V_{DD} = 0V, V_{SS} = –5.0 ±0.5 V, Ta = –20 to 75 °C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Supply voltage	V_{SS}		–6.0	—	–0.9	V
LCD supply voltages	V_1		—	1/3 × V3	—	V
	V_2		—	2/3 × V3	—	
	V_3		–6.0	—	–1.8	
Quiescent supply current	I_{DDQ}	V_{SS} = –6.0 V, V_{IN} = V_{DD}	—	0.05	1.0	µA
Supply current	I_{DD1}	Display mode, R_f = 680 KΩ, V_{SS} = –5.0 V	—	20.0	30.0	µA
	I_{DD2}	Input mode, V_{SS} = –5.0 V, f_{ck} = 200 kHz	—	100	250	
LOW-level input voltage	V_{IL}		V_{SS}	—	0.8 V_{SS}	V
HIGH-level input voltage	V_{IH}		0.2 V_{SS}	—	V_{DD}	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	—	0.05	2.0	µA
SEG0 to SEG31 and COM0 to COM3 LOW-level output voltage	V_{OL}	I_{OL} = 0.1 mA	—	—	V_{SS}+ 0.4	V
SEG0 to SEG31 and COM0 to COM3 HIGH-level output voltage	V_{OH}	I_{OH} = –0.1 mA	–0.4	—	—	V
Output leakage current	I_{LO}	$V_{SS} \le V_{OUT} \le V_{DD}$	—	0.05	5.0	µA
Oscillator frequency	f_{OSC}	V_{SS} = –5.0 V, R_f = 680 ±2% kΩ	—	18	—	kHz
		V_{SS} = –3.0 V, R_f =680 ±2% kΩ	—	16	—	
Input terminal capacity	C_I	Ta = 25°C, f = 1 MHz	—	5.0	8.0	pF
SEG0 to SEG31 and COM0 to COM3 ON resistance *1	R_{ON}	V_3 = –5.0 V, I ΔVON I = 0.1 V, Ta = 25 deg C	—	5.0	7.5	kΩ
		V_3 = –0.3 V, I ΔVON I = 0.1 V, Ta = 25 deg.C	—	10.0	50.	

*1 The internal power impedance is not included in the LCD driver on resistance (R_{ON}).

AC Electrical Characteristics

V_{DD} = 0 V, V_{SS} = –5.0 ±0.5 V, Ta = –20 to 75 °C

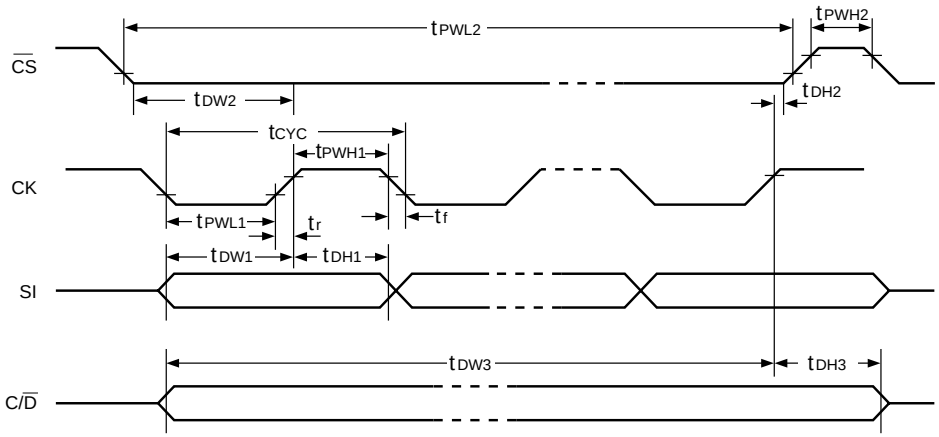
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CK period	t_{CYC}		900	—	—	ns
CK LOW-level pulsewidth	t_{PWL1}		400	—	—	ns
CK HIGH-level pulsewidth	t_{PWH1}		400	—	—	ns
SI to CK setup time	t_{DW1}		100	—	—	ns
CK to SI hold time	t_{DH1}		200	—	—	ns
$\overline{CS}$ LOW-level puisewidth	t_{PWL2}	$t_{PWL2} \geq 8t_{CYC}$	7200*1	—	—	ns
$\overline{CS}$ HIGH-level pulsewidth	t_{PWH2}		400	—	—	ns
$\overline{CS}$ to CK setup time	t_{DW2}	Referenced to the rising edge of the first CK cycle.	100	—	—	ns
CK to $\overline{CS}$ hold time	t_{DH2}	Referenced to the rising edge of the eighth CK cycle.	200	—	—	ns
C/$\overline{D}$ to CK setup time	t_{DW3}	Referenced to the rising edge of the eighth CK cycle.	9	—	—	µs
CK to C/$\overline{D}$ hold time	t_{DH3}	Referenced to the rising edge of the eighth CK cycle.	1	—	—	µs
Rise time	t_r		—	—	50	ns
Fall time	t_f		—	—	50	ns

*1 $t_{CYC} \times 8$

V_{DD} = 0 V, V_{SS} = –6.0 to –1.5 V, Ta = –20 to 75 °C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CK period	t_{CYC}		10	—	—	µs
CK LOW-level puisewidth	t_{PWL1}		4.5	—	—	µs
CK HIGH-level pulsewidth	t_{PWH1}		4.5	—	—	µs
SI to CK setup time	t_{DW1}		1.2	—	—	µs
CK to SI hold time	t_{DH1}		2.3	—	—	µs
$\overline{CS}$ LOW-level pulsewidth	t_{PWL2}	$t_{PWL2} \geq 8t_{CYC}$	80*1	—	—	µs
$\overline{CS}$ HIGH-level pulsewidth	t_{PWH2}		4.5	—	—	µs
$\overline{CS}$ to CK setup time	t_{DW2}	Referenced to the rising edge of the first CK cycle.	1.2	—	—	µs
CK to $\overline{CS}$ hold time	t_{DH2}	Referenced to the rising edge of the eighth CK cycle.	2.3	—	—	µs
C/$\overline{D}$ to CK setup time	t_{DW3}	Referenced to the rising edge of the eighth CK cycle.	100	—	—	µs
CK to C/$\overline{D}$ hold time	t_{DH3}	Referenced to the rising edge of the eighth CK cycle.	11	—	—	µs
Rise time	t_r		—	—	50	ns
Fall time	t_f		—	—	50	ns

*1 $t_{CYC} \times 8$



Timing measurement