SED1520
CMOS Dot Matrix LCD Driver
Data Sheet and Design Guide

S-MOS SYSTEMS, INC.

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1.0
Overview

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1.0 Overview

1.1 Description

The SED1520 is a dot matrix LCD driver LSI intended for display of characters and graphics. It generates LCD driving signals based on bit image display data supplied from an 8-bit or 16-bit microcomputer and stored in the on-chip display data RAM.

The SED1520 incorporates innovative circuit design strategies to assure very low current dissipation and a wide range of operating voltages. With these features, the SED1520 permits the user to implement high-performance handy systems operating from a miniature battery.

In order for the user to adaptively configure his system, the SED1520 family offers two application forms. One form allows an LCD display of 12 characters × 2 lines with an indicator with a single chip. The other is dedicated to driving a total of 80 segments, enabling a medium-size display to be achieved by using a minimum number of drivers.

1.2 Features

- Direct display of data read from display data RAM

  RAM bit data: '0' — LCD off
  '1' — LCD on

- Fast 8-bit MPU interface; direct interface with 80- or 68-family microcomputer
- On-chip LCD driving circuits — 80 (segment + common) driver sets
- Duty ratios to choose from:

  Command setup 1/16, 1/32 (SED1520F)
  External input sync 1/8 to 1/32 (SED1521F)

- A variety of command functions, including:

  Read/Write Display Data, Display ON/OFF, Set Address, Set Display Start Line, Set Column Address, Read Status, Static Drive ON/OFF, Select Duty, Read Modify Write, Select Segment Driving Selection, Save Power, etc.

- Very low power dissipation — 30 μW maximum (External clock operation: 2 kHz)
- Wide spectrum of supply voltages

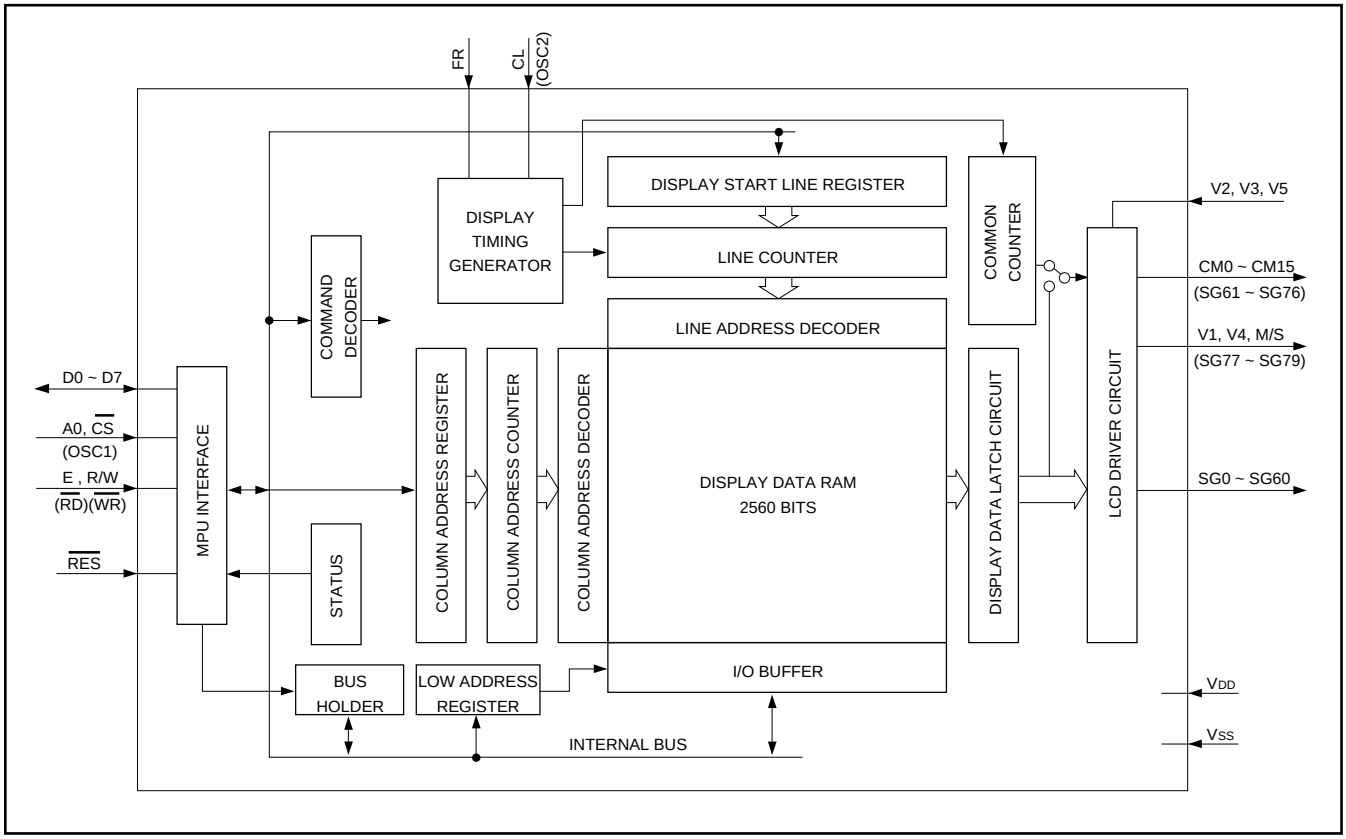
  $V_{DD} - V_{SS}$ –2.4V to –7.0V
  $V_{DD} - V5$ –3.5V to –13.0V

- CMOS process

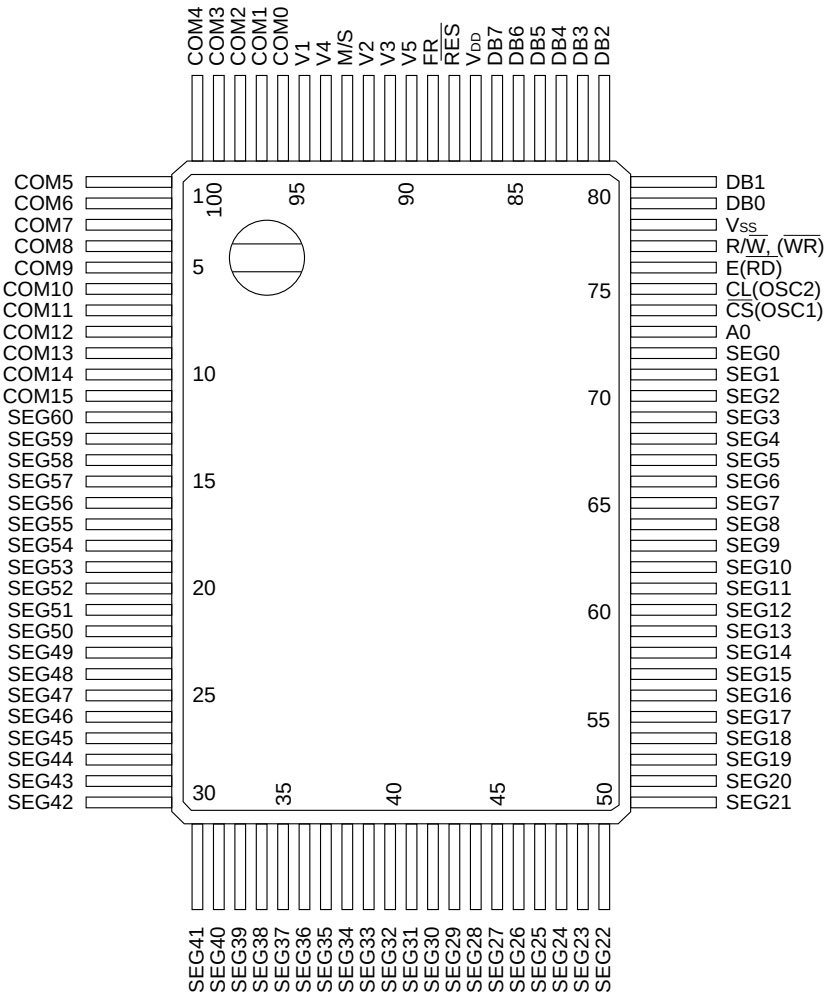
1.2.1 SED1520 family specifications

Product Name	Clock Frequency		Applicable Driver	No. of SEG Drivers	No. of COM Drivers
	On-chip	External			
SED1520F0A	18 kHz	18 kHz	SED1520F0A, SED1521F0A	61	16
SED1521F0A	—	18 kHz		80	0
SED1520FAA	—	2 kHz	SED1520FAA, SED1521FAA, HD44103CH	61	16
SED1521FAA	—	2 kHz		80	0

1.3 Block Diagram



1.4 Package



* The pin configuration on the SED1520F is shown here.

1.4.1 Pin Configuration Table

Product Name	Pin Number					
	74	75	96 ~ 100, 1 – 1j	93	94	95
SED1520F0A	OSC1	OSC2	COM0 ~ COM15	M/S	V4	V1
SED1521F0A	$\overline{CS}$	CL	SEG76 ~ SEG61	SEG79	SEG78	SEG77
SED1520FAA	$\overline{CS}$	CL	COM0 ~ COM15*	M/S	V4	V1
SED1521FAA	$\overline{CS}$	CL	SEG76 ~ SEG61	SEG79	SEG78	SEG77

* Master LSI common outputs COM0 — COM15 correspond to slave LSI outputs COM31 — COM16.

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2.0
Pin Description

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2.0 Pin Description

2.1 Power Signals

- **V_{DD}**

  Connected to +5V power. Common to MPU power pin V_{CC}.

- **V_{SS}**

  0V, connected to system GND.

- **V1 – V5**

  Multi-level power used to drive LCDs. Voltage specified to each LCD cell is divided by resistors or impedance-converted by an operational amplifier before being applied. Each voltage to be applied must be based on V_{DD}, while fulfilling the following conditions:

  $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

2.2 System Bus Interface Signals

- **D7 – D0**

  8-bit, tri-state, bi-directional I/O bus. Normally, connected to the data bus of an 8-/16-bit standard microcomputer.

- **A0**

  Input pin. Normally, the LSB of the MPU address bus is connected to this input pin to provide data/command selection.

  0 : Display control data on D0 — D7

  1 : Display data on D0 — D7

- **$\overline{RES}$**

  Input pin. The SED1520 can be reset or initialized by setting $\overline{RES}$ to low level (if it is interfaced with a 68-family MPU) or high level (if with an 80-family MPU). This reset operation occurs when an edge of the $\overline{RES}$ signal is sensed. The level input selects the type of interface with the 68- or 80-family MPU:

  High level : Interface with 68-family MPU

  Low level : Interface with 80-family MPU

- **$\overline{CS}$**

  Chip Select input signal which is normally obtained by decoding an address bus signal. Effective with “L” active and a chip operating with external clocks. For a chip containing an oscillator, $\overline{CS}$ works as an oscillation amplifier input pin to which an oscillation resistor (R_f) is connected. In this case, $\overline{RD}$, $\overline{WR}$ and E must be a signal ANDed with $\overline{CS}$.

- **E ($\overline{RD}$)**
  - **Chip interfaced with 68-family MPU:**

    Enable Clock signal input for the 68-family MPU.
  - **Chip interfaced with 80-family MPU:**

    “L” active input pin to which the 80-family MPU $\overline{RD}$ signal is connected. With this signal held at “L”, the SED1520 data bus works as output.

- **R/$\overline{W}$ ($\overline{WR}$)**
  - **Chip interface with 68-family MPU:**

    Read/write control signal input pin.

    R/$\overline{W}$ = “H” : Read

    R/$\overline{W}$ = “L” : Write
  - **Chip interfaced with 80-family MPU:**

    “L” active input pin to which the 80-family $\overline{WR}$ is connected. The signal on the data bus is fetched by the leading edge of $\overline{WR}$.

2.3 LCD Drive Circuit Signals

- **CL**

  Input signal effective with a chip using external clocks. This display data latch signal increments the line counter (at the trailing edge) or the common counter (at the leading edge). CL is connected to CL2 of the common driver. For a chip containing an oscillator, this pin works as the oscillation amplifier output pin to which an oscillation resistor (R_f) is connected.

- **FR**

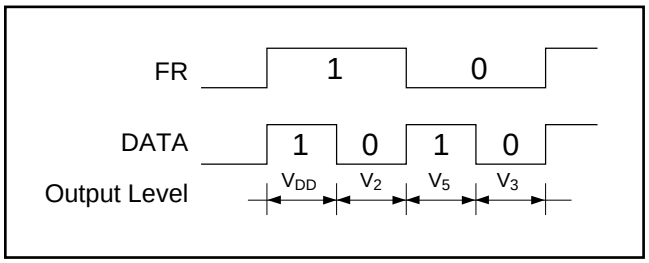
  LCD AC signal I/O pin. Connected to pin M of the common driver.

  - **I/O selection:**

    Chip containing commons M/S = 1: Output
    M/S = 0: Input
    Chip containing segments alone : Input

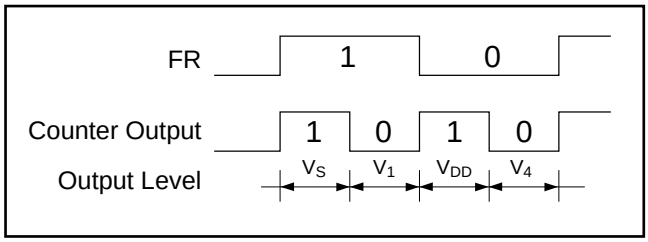
- **SEG0 – SEG79**

  LCD column (segment) driving output. One of the V_{DD}, V2, V3 and V5 levels is selected by a combination of the content of display RAM and the FR signal.



- **COM0 – COM15 (COM31 – COM16)**

  LCD common (row) driving output. One of the V_{DD}, V1, V4 and V5 levels is selected by a combination of the output of the common counter and the FR signal. The common (row) scanning order for the slave LSI is reverse to that for the master LSI.



- **M/S (SEG79)**

  Input signal which selects the master or slave LSI. Connected to V_{DD} or V_{SS}.

  M/S = V_{DD} : Master

  M/S = V_{SS} : Slave

  M/S selection changes the function of pins FR, COM0 – COM15, OSC1 ($\overline{CS}$) and OSC2 (CL):

M/S	FR	COM output	OSC1	OSC2
V_{DD}	Output	COM0 – COM15	Input	Output
V_{SS}	Input	COM31 – COM16	NC	Input

* The common scanning order for the slave driver is reverse to that for master.

3.0
Description of Circuit Blocks

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3.0 Description of Circuit Blocks

3.1 MPU Interface

3.1.1 Selection of Interface Type

The SED1520 Series uses 8 bits of bi-directional data bus (D0 – D7) to transfer data. The reset pin is capable of selecting MPU interface; setting the polarity of $\overline{RES}$ to either "H" or "L" can provide direct interface of the SED1520 with a 68- or 80-family MPU (see Table 3.1 below).

With $\overline{CS}$ at high level, the SED1520 is independent from the MPU bus and stays in standby mode. In this mode, however, the reset signal is input independently of the internal status.

Table 3.1

Polarity of $\overline{RES}$	Type	A0	R	R/W	$\overline{CS}$	D0 – D7
"L" active	68 MPU	↑	↑	↑	↑	↑
"H" active	80 MPU	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

3.1.2 Identification of Data Bus Signals

The SED1520 uses a combination of A0, E, R/W, ($\overline{RD}$, $\overline{WR}$) to identify a data bus signal.

Table 3.2

Common	68 MPU	80 MPU		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

3.1.3 Access to Display Data RAM and Internal Register

In order to make matching of operating frequencies between the MPU and the display data RAM or internal register, the SED1520 performs a sort of LSI-LSI pipelining via the bus holder attached to the internal data bus. Consider the case where the MPU reads the content of the display data RAM. In the first data read cycle (dummy), the data is stored on the bus holder. In the next data read cycle, the data is read from the bus holder to the system bus. Also consider the case where the MPU writes data to the display data RAM. In the first data write cycle, the data is held on the bus holder. The data is written to the display data RAM before the next data write cycle begins. Therefore, MPU's access to the SED1520 is affected not by display data RAM access time (t ACC, t DS) but by cycle time (t CYC). This leads to faster transfer of data to and from the MPU. If the cycle time requirement is not met, the MPU has only to execute the NOP instruction and this is apparently equivalent to execution of a waiting operation. However, there is a restriction on the read sequence of the display data RAM; when an address is set, its data is output not to the first read instruction (immediately following the address setting operation) but to the second read instruction. Thus, one dummy read cycle is necessary after an address set or write cycle. This relation is shown in Figure 3.1.

3.2 Busy Flag

Busy flag being "1" means that the SED1520 is performing its internal operation and any instruction other than Read Status is disabled. The busy flag is output to pin D7 by a Read Status instruction. As long as the cycle time (t CYC) requirement is met, the flag need not be checked before each command and this dramatically improves the MPU performance.

3.3 Display Start Line Register

This register is a pointer which determines the start line corresponding to COM0 (normally, the uppermost line of display) for display of data in the display data RAM. It is used for scrolling the display or changing the page from one to another.

Executing the Set Display Start Line command sets 5 bits of display start address in this register. Its content is preset in the line counter at each timing the FR signal changes. The line counter is incremented synchronously to a CL input, thus, generating a line address for sequential reading of 80 bits of data from the display data RAM to the LCD driver circuit.

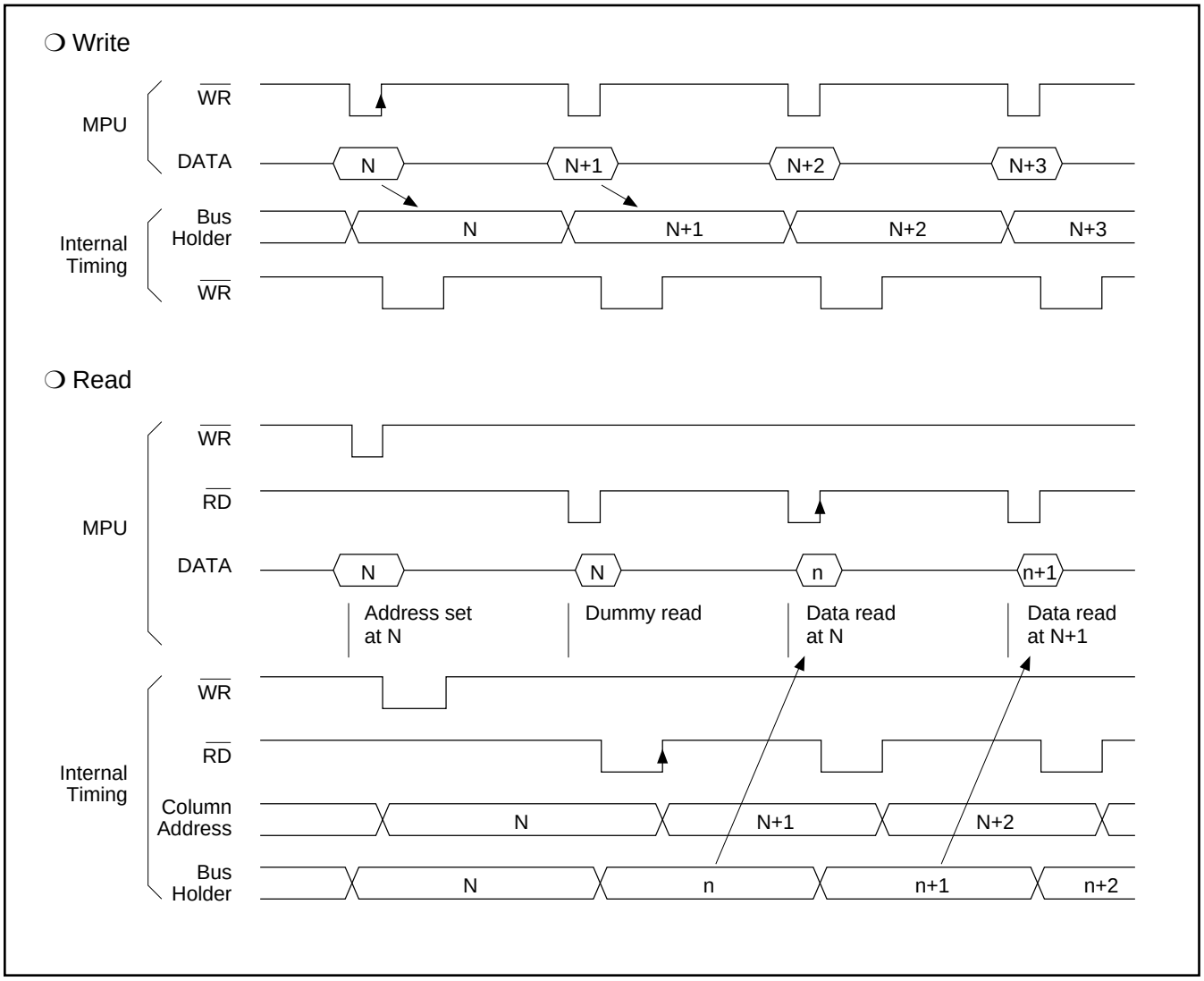


Figure 3.1

3.4 Column Address Counter

The column address counter is a 7-bit presettable counter which gives column addresses of the display data RAM as shown in Figure 3.3. When a Read/Write Display Data command comes in, the counter is incremented by 1. For any nonexisting address over 50H, the counter is locked and not incremented.

The column address counter is independent from the page register.

3.5 Page Register

This register gives a page address of the display data RAM as shown in Figure 3.3. The Set Page Address command permits the MPU to access a new page of the display data RAM.

3.6 Display Data RAM

Dot data for display is stored in this RAM. Since the MPU and LCD driver circuit operate independently of each other, data can be changed asynchronously without adverse effect on the display.

One bit of the display data RAM is assigned to one bit of LCD:

LCD on = "1"

LCD off = "0"

The ADC command inverts the assignment relationship between a display data RAM column address and a segment output (see Figure 3.3).

3.7 Common Timing Generator

This circuit generates common timing and frame (FR) signals from the basic clock (CL). The Select Duty command selects a duty of 1/16 or 1/32. The 1/32 duty is achieved by a two-chip (master and slave) configuration (common multi-chip system).

3.8 Display Data Latch Circuit

The display data latch circuit temporarily stores the data which will be output from the display data RAM to the LCD driver circuit at one-common intervals. The Display ON/OFF and Static Driver ON/OFF commands control the latched data so that the data in the display data RAM remains unchanged.

3.9 LCD Driver Circuit

This circuit generates 80 sets of multiplexer that generate quartet levels for LCD driving. Display data in the display data latch, common timing generator output and FR signal are combined to output an LCD driving waveform.

3.10 Display Timing Generator

This circuit generates an internal display timing signal from the basic clock (CL) and frame signal (FR).

The frame signal FR makes the LCD driver circuit generate a dual frame AC driving waveform (type B) to drive LCD, while making both the line counter and common timing generator synchronized to the FR signal output LSI (dedicated common driver or the SED1520 master LSI). To achieve these functions, the FR signal must be a clock with a duty of 50% which is synchronized to the frame period. The clock CL is a clock used to operate the line counter. For a system in which both the SED1520 and SED1521F coexist, they should be of LSI types having the same clock frequency to be applied to pin CL.

3.11 Oscillation Circuit

This circuit is a low-power CR oscillator which uses an oscillation resistor R_f alone to adjust the oscillation frequency. It generates display timing signals. The SED1520 is available in two LSI types if classified by oscillation: one LSI type contains an oscillation circuit and the other uses an externally provided clock.

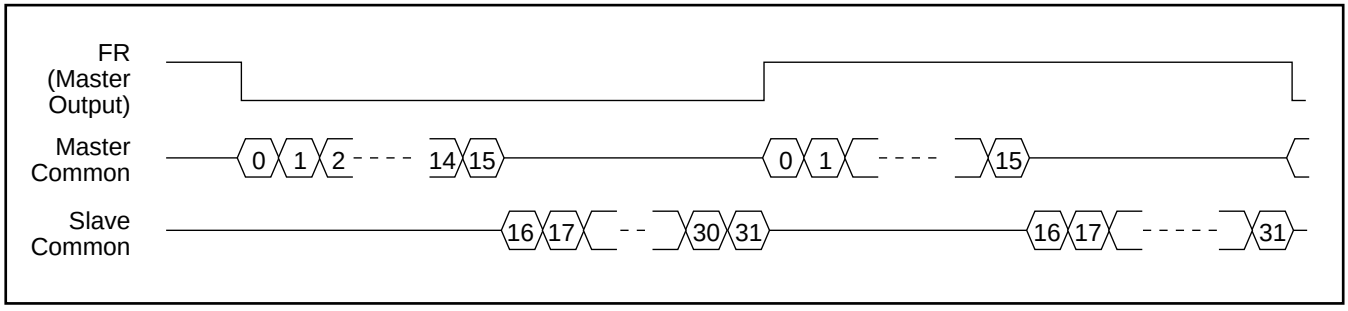


Figure 3.2

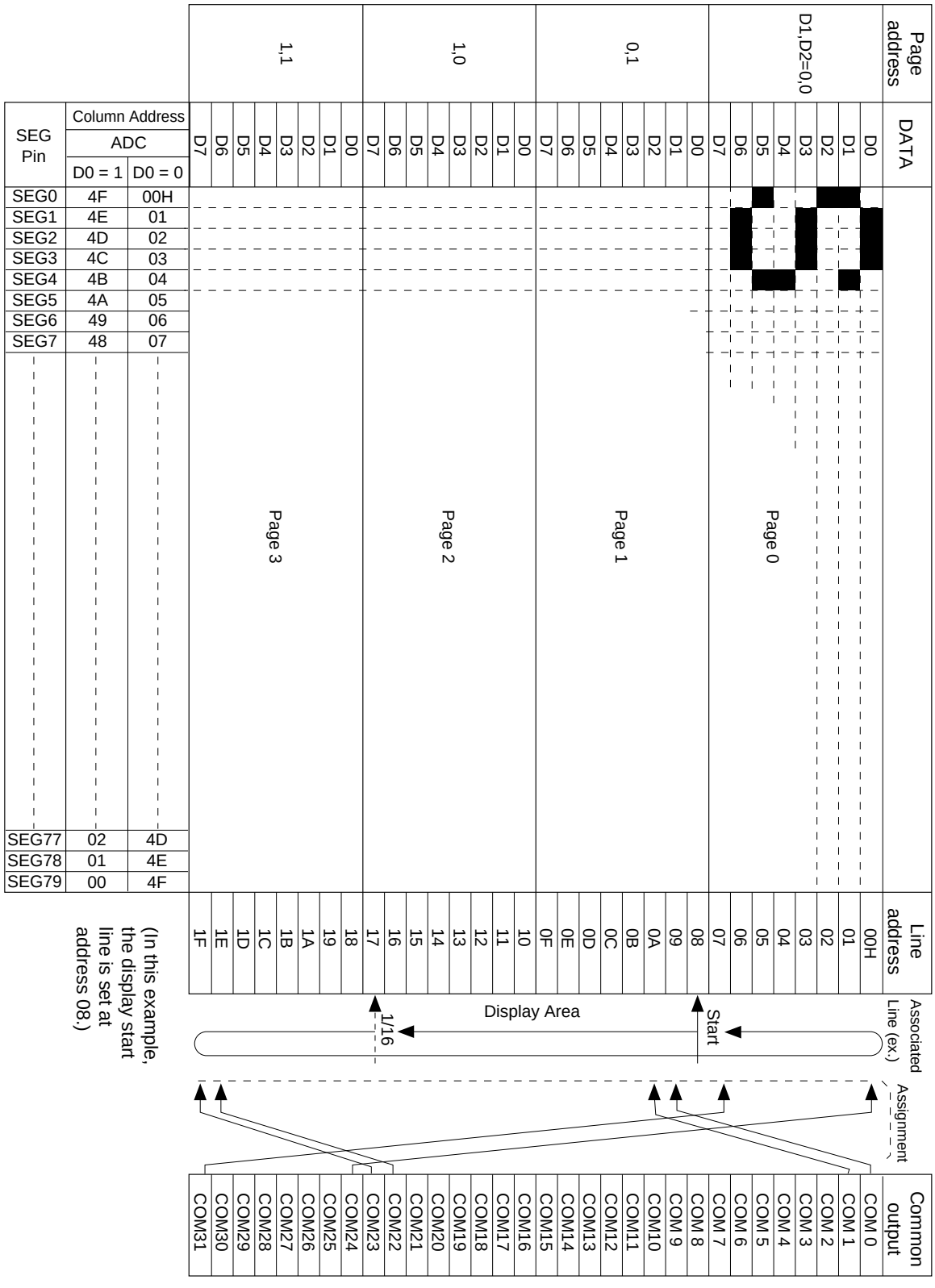
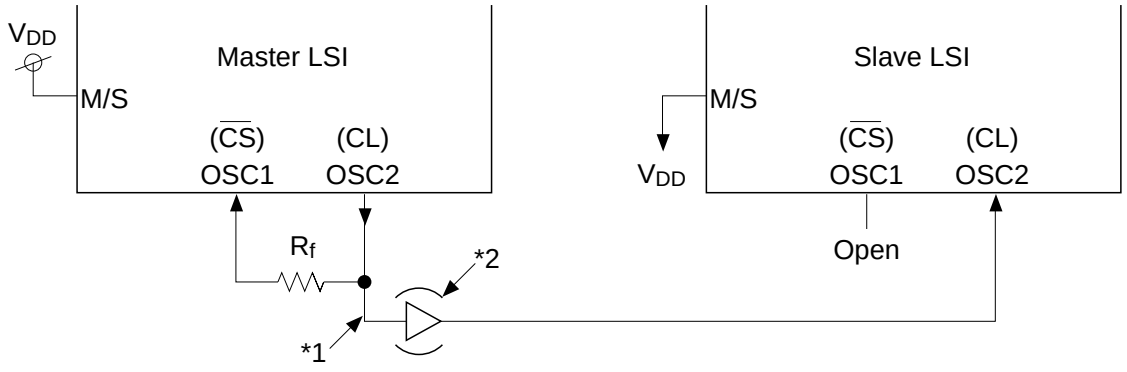


Figure 3.3. Relationship between Display Data RAM Locations and Addresses (Display Start Line: 08)



*1 As the parasitic capacitance in this portion increases, the oscillation frequency will shift to a lower level. The Rf must have a smaller value than the specification.

*2 For a system having two or more slave LSIs, a CMOS buffer is necessary.

Figure 3.4. LSI containing oscillator

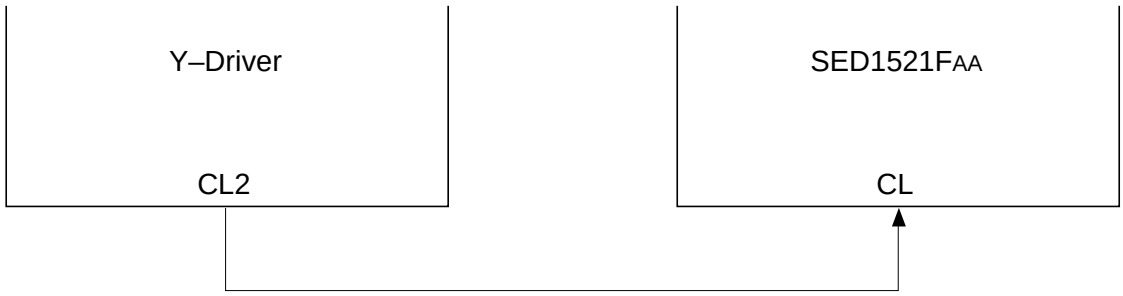


Figure 3.5. LSI operating with external clock

The oscillation resistor R_f is connected as shown below. Where an LSI containing an oscillation circuit is operated with an external clock, it is necessary to input the clock with the same phase as OSC2 of the master LSI to OSC2 of the slave LSI.

3.12 Reset Circuit

This circuit senses the leading edge or trailing edge of $\overline{RES}$ and initializes the system when its power is switched on.

Initialization:

(a) Display off
(b) Display start line register: First line
(c) Static drive off
(d) Column address counter: Address 0
(e) Page address register: Page 0
(f) Select duty: 1/32
(g) Select ADC: Forward (ADC command D0 = "0", ADC status flag = "1")
(h) Read modify write off

The input at pin $\overline{RES}$ is level-sensed to select an MPU interface mode as shown in Table 3.1. For interfacing with an 80-family MPU, an "H" active reset signal is input to pin $\overline{RES}$. For interfacing with a 68-family MPU, an "L" active reset signal is input to the pin (see Figure 6.1).

As exemplified in chapter 6.0, "Interface with MPU," pin $\overline{RES}$ is connected to the MPU reset pin. Thus, the SED1520 and the MPU are initialized at the same time. If system is initialized by pin $\overline{RES}$ at power-on, it may no longer be reset.

The Reset command causes initialization (b), (d) and (e).

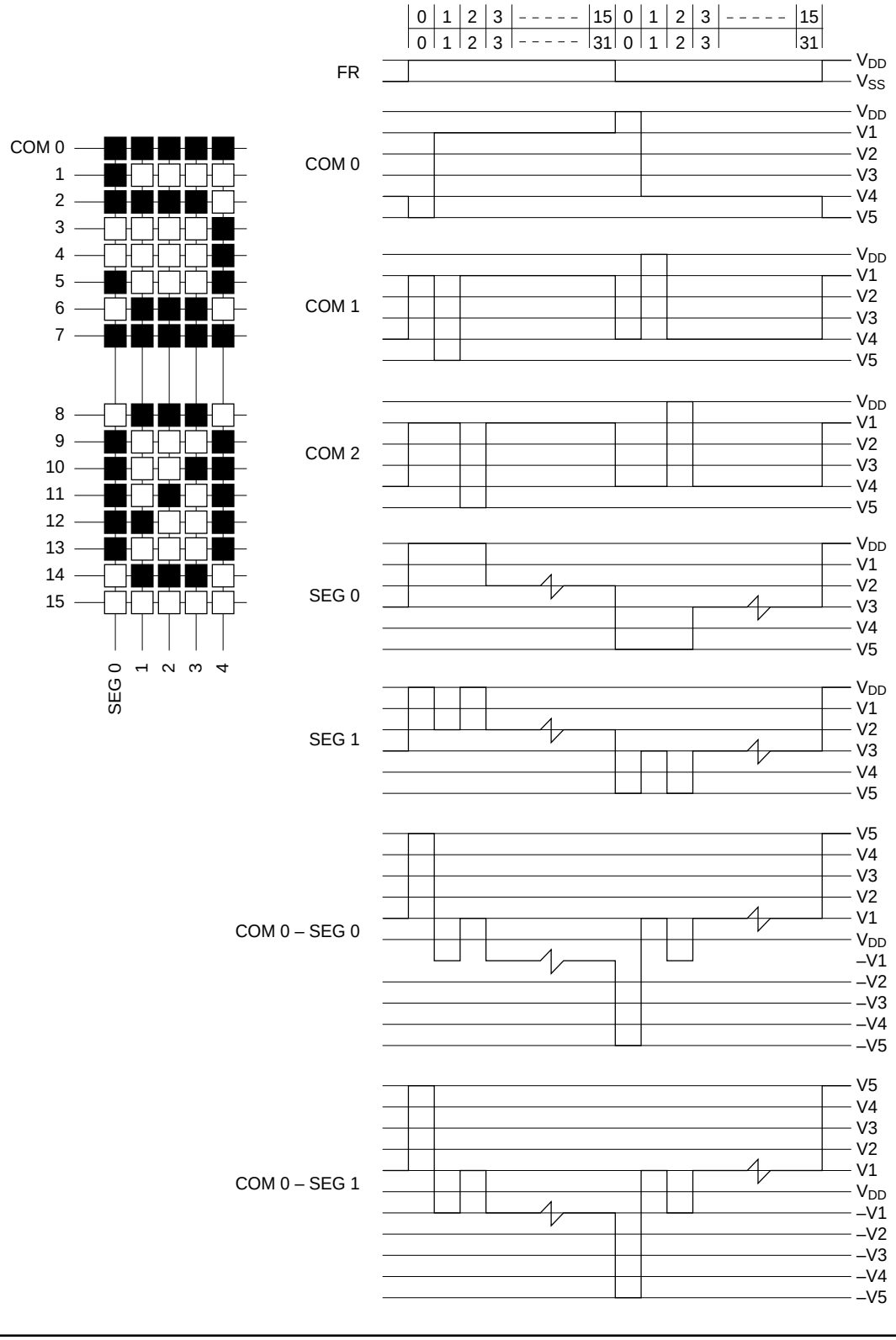


Figure 3.6. Examples of LCD Driving Waveform

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4.0
Commands

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4.0 Commands

Table 4.1 lists the commands used with the SED1520. This LSI uses a combination of A0, R/W, ($\overline{RD}$, $\overline{WR}$) to identify a data bus signal. Interpretation and execution of a command depends not on external clock but on internal timing alone. Therefore, a command can be executed so fast that no busy check is needed.

Table 4.1. Commands

	Command	Code											Function
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns all display on or off, independently of display RAM data or internal status. 1: ON 0: OFF (Power-saving mode with static drive on)*
(2)	Display Start Line	0	1	0	1	1	0	Display Start Address (0 – 31)					Specifies RAM line corresponding to uppermost line (COM0) of display.
(3)	Set Page Address	0	1	0	1	0	1	1	1	0	Page (0–3)		Sets display RAM page in page address register.
(4)	Set Column (Segment) Address	0	1	0	0	Column Address (0–79)							Sets display RAM column address in column address register.
(5)	Read Status	0	0	1	Busy	ADC	ON/OFF	RESET	0	0	0	0	Reads the following status: BUSY 1: Internal operation 0: Ready ADC 1: CW output (forward) 0: CCW output (reverse) ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
(6)	Write Display Data	1	1	0	Write Data								Writes data from data bus into display RAM. Display RAM location whose address has been preset is accessed. After access, the column address is incremented by 1.
(7)	Read Display Data	1	0	1	Read Data								Reads data from display RAM onto data bus.
(8)	Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	Used to invert relationship of assignment between display RAM column addresses and segment driver outputs. 0: CW output (forward) 1: CCW output (reverse)
(9)	Static Drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects normal display or static driving operation. 1: Static drive (power-saving mode) 0: Normal driving
(10)	Select Duty	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD cell driving duty 1: 1/32 0: 1/16
(11)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments column address counter by 1 when display data is written. (This is not done when data is read.)
(12)	End	0	1	0	1	1	1	0	1	1	1	0	Clears read modify write mode.
(13)	Reset	0	1	0	1	1	1	0	0	0	1	0	Sets display start line register on the first line. Also sets column address counter and page address counter to 0.

* With display off (command (1)), static drive going on (9) invokes power-saving mode.

A detailed description of all the commands follows.

4.1 Display ON/OFF

This command forces all display to turn on or off.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	0	1	1	1	D

Note:
D = 0 Display OFF
D = 1 Display ON

4.2 Display Start Line

This command specifies a line address (shown in Figure 3.3) thus marking the display line that corresponds to COM0. Display begins with the specified line address and covers as many lines as match the display duty in address ascending order. Dynamic line address change with the Display Start Line command enables column-wise scrolling or page change.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	0	A4	A3	A2	A1	A0

← High order bits

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		↓			↓
1	1	1	1	1	31

4.3 Set Page Address

This command is used to specify a page address equivalent to a row address for MPU access to the display data RAM. A required bit of the display data RAM can be accessed by specifying its page address and column address. Changing the page address causes no change in display.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	1	1	0	A1	A0

A1	A0	Page
0	0	0
0	1	1

A1	A0	Page
1	0	2
1	1	3

4.4 Column Address

This command specifies a display data RAM column address. The column address is incremented by 1 each time the MPU accesses from the set address to the display data RAM. Thus it is possible for the MPU to gain continuous access to only the data. This incrementing stops with address 80; the page address is not continuously changed.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			↓				↓
1	0	0	1	1	1	1	79

4.5 Read Status

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	1	BUSY	ADC	ON / OFF	RESET	0	0	0	0

Note:

BUSY BUSY being "1" means that system is performing an internal operation or is reset. No command is accepted before BUSY = "0". As long as the cycle time requirement is met, no BUSY check is needed.

ADC Indicates assignment of column addresses to segment drivers.

0 : Inverted (column address 79 – n ↔ segment driver n)

1 : Forward (column address n ↔ segment driver n)

ON/OFF Indicates display on or off.

0 : Display on

1 : Display off

This bit has polarity reverse to the Display ON/OFF command.

RESET Indicates that system is being initialized by the $\overline{RES}$ signal or the Reset command.

0 : Display mode

1 : Being reset

4.6 Write Display Data

This command allows the MPU to write 8 bits of data into the display data RAM. Once the data is written, the column address is automatically incremented by 1; this enables the MPU to write multi-word data continuously.

R/$\overline{W}$

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	WRITE DATA							

4.7 Read Display Data

This command allows the MPU to read 8 bits of data from the display data RAM location specified by a column address and a page address. Once the data is read, the column address is automatically incremented by 1; this enables the MPU to read multi-word data continuously.

A dummy read is needed immediately after the column address is set. For details, see 3. (1) – (c).

R/$\overline{W}$

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	READ DATA							

4.8 Select ADC

This command inverts the relation of assignment between display data RAM column addresses and segment driver outputs. In other words, the Select ADC command can software-invert the order of segment driver output pins, reducing the restrictions on the configuration of ICs at LCD module assembly. For details, see Figure 3.3.

Incrementing the column address by 1, which takes place after the MPU writing or reading display data, follows the sequence of column addresses specified in Figure 3.3.

R/$\overline{W}$

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	0

Note:
D = 0 Clockwise output (forward)
D = 1 Counterclockwise output (reverse)

4.9 Static Drive ON/OFF

This command forces all display to be on and, at the same time, all common output to be selected.

R/$\overline{W}$

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

Note:
D = 0 Static drive off
D = 1 Static drive on

4.10 Select Duty

This command is used to select the duty (degree of multiplexity) of LCD driving. It is valid for the SED1520F (actively operating LSI) only, not valid for the SED1521F (passively operating LSI). The SED1521F operates with any duty determined by the FR signal.

R/$\overline{W}$

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

Note:
D = 0 Duty 1/16
D = 1 Duty 1/32

If the system contains both SED1520F0A (internal oscillation) and the SED1521F0A LSIs, they must have the same duty.

4.11 Read Modify Write

This command is used with the End command in a pair. Once it has been entered, the column address will be incremented, not by the Read Display Data command, but by the Write Display Data command only. This mode will stay until the End command is entered.

Entry of the End command causes the column address to return to the address which was valid when the Read Modify Write command was entered. This function lessens the load of the MPU when the data in a specific display area are repeatedly updated (as blinking cursor).

R/$\overline{W}$

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in the Read Modify Write mode, any command other than Read/Write Data and Set Column Address may be used.

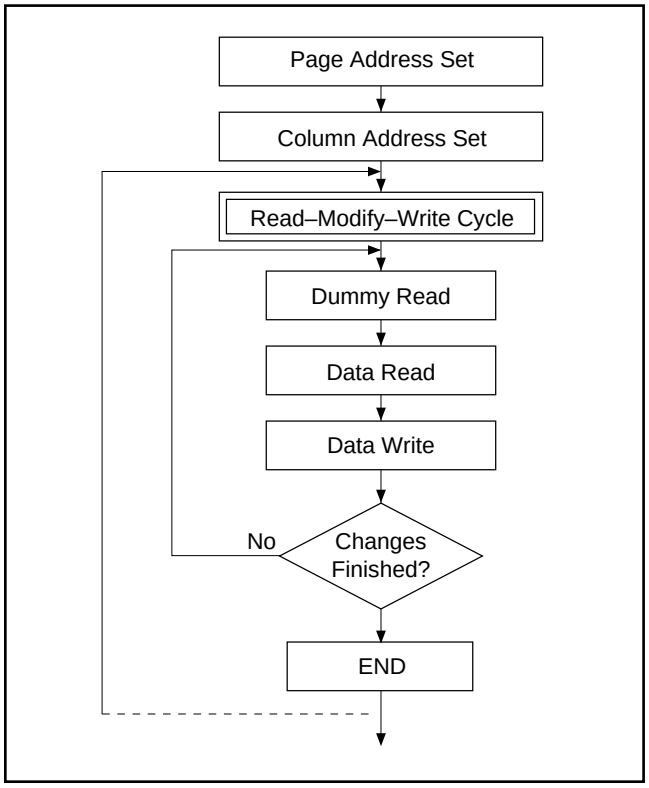

Figure 4.1. Cursor blinking sequence

4.12 End

This command cancels the Read Modify Write command, returning the column address to the initial mode address. See Figure 4.2.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	1	0	1	1	1	0

4.13 Reset

This command initializes the display start line register, column address counter, and page address counter without any effect on the display data RAM. For details, see 6-(12).

The reset operation follows entry of the Reset command.

		R/$\overline{W}$								
A0	**$\overline{RD}$**	**$\overline{WR}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	1	1	0	0	0	1	0

Initialization at power-on is performed, not by the Reset command, but by a reset signal applied to the $\overline{RES}$ pin.

4.14 Save Power (Combined Command)

Static drive going on with display off invokes power-saving mode, reducing current consumption to nearly static current level. During this mode, the SED1520 holds the following conditions:

- It stops driving the LCD; the segment and common driver outputs are at V_{DD} level.
- Oscillation and external clock input are disabled; OSC2 is in floating condition.
- The display data and operational mode are held.

The power-saving mode is cancelled by display on or static drive off.

If an external resistor division circuit is used to give LCD driving voltage level, the current flowing into the resistors must be cut off by the power-save signal.

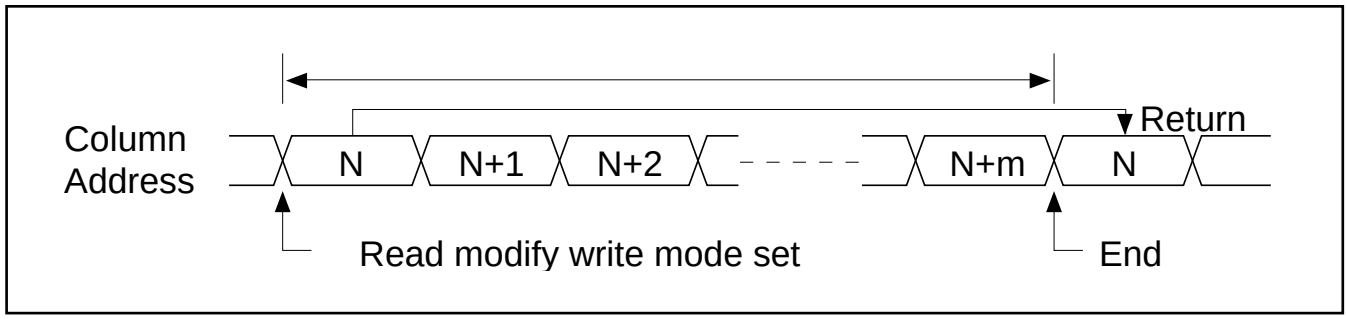

Figure 4.2

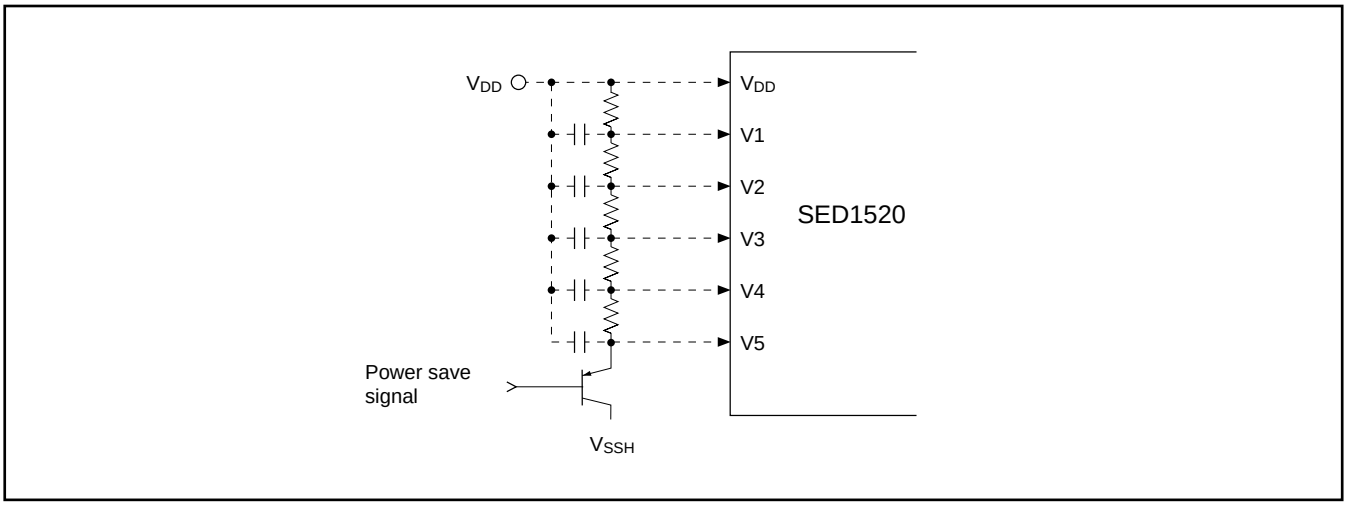

Figure 4.3

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5.0
Electrical Characteristics

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5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Supply voltage (1)	V_{SS}	–8.0 ~ +0.3	V
Supply voltage (2)	V5	–16.5 ~ +0.3	V
Supply voltage (3)	V1, V4, V2, V3	V5 ~ +0.3	V
Input voltage	V_{IN}	V_{SS} – 0.3 ~ +0.3	V
Output voltage	V0	V_{SS} – 0.3 ~ +0.3	V
Allowable loss	P_D	250	mW
Operating temperature	T_{opr}	–30 ~ +85	°C
Storage temperature	T_{stg}	–65 ~ +150	°C
Soldering temperature/time	T_{solder}	260 / 10 (at lead)	°C / Sec

Notes:

1. All voltages are based on V_{DD} = 0V.
2. The following condition must always hold true with voltages V1, V2, V3, V4 and V5:

   $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$
3. The LSI may be permanently damaged if used with any value in excess of the absolute maximum ratings. During normal operation, the LSI should preferably be used within the specified electrical characteristics. Failure to meet them can cause the LSI to malfunction or lose its reliability.
4. Generally, flat package LSIs may have moisture resistance lowered when solder dipped. In mounting LSIs on a board, it is recommended to use a method which is least unlikely to give thermal stress on the package resin.

5.2 DC Characteristics

V_{DD} = 0V, T_a = –20 to 75°C

Parameter		Symbol	Condition		Min	Typ	Max	Unit	Applicable Pin
Operating voltage (1)	Recommended	V_{SS}	*1		–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V5			–13.0	—	–3.5	V	V5
	Allowable				–13.0	—	—		*10
	Allowable	V1, V2			0.6 × V5	—	V_{DD}	V	V1, V2
	Allowable	V3, V4			V5	—	0.4 × V5	V	V3, V4
High-level input voltage		V_{IHT}			V_{SS} + 2.0	—	V_{DD}	V	*2
		V_{IHC}			0.2 × V_{SS}	—	V_{DD}		*3
Low-level input voltage		V_{ILT}			V_{SS}	—	V_{SS} + 0.8	V	*2
		V_{ILC}			V_{SS}	—	0.8 × V_{SS}		*3
High-level output voltage		V_{OHT}	I_{OH} = –3.0 mA		V_{SS} + 2.4	—	—	V	*4
		V_{OHC1}	I_{OH} = –2.0 mA		V_{SS} + 2.4	—	—		*5
		V_{OHC2}	I_{OH} = –120 µA		0.2 × V_{SS}	—	—		OSC2
Low-level output voltage		V_{OLT}	I_{OL} = 3.0 mA		—	—	V_{SS} + 0.4	V	*4
		V_{OLC1}	I_{OL} = 2.0 mA		—	—	V_{SS} + 0.4		*5
		V_{OLC2}	I_{OL} = 120 µA		—	—	0.8 × V_{SS}		OSC2
Input leakage current		I_{LI}			–1.0	—	1.0	µA	*6
Output leakage current		I_{LO}			–3.0	—	3.0	µA	*7
LCD driver ON resistor		R_{ON}	T_a = 25°C	V5 = –5.0V	—	5.0	7.5	kΩ	SEG0~79 COM0~15 *11
				V5 = –3.5V	—	10.0	50.0		
Static current dissipation		I_{DDQ}	$\overline{CS}$ = CL = V_{DD}		—	0.05	1.0	µA	V_{DD}
Dynamic current dissipation		I_{DD} (1)	During display V5 = –5.0V	f_{CL} = 2 kHz	—	2.0	5.0	µA	V_{DD} *12
				R_f = 1 MΩ	—	9.5	15.0		*13
				f_{CL} = 18 kHz	—	5.0	10.0		*14
		I_{DD} (2)	During access t_{cyc} = 200 kHz		—	300	500	µA	*8
Input pin capacitance		C_{IN}	T_a = 25°C f = 1 MHz		—	5.0	8.0	pF	All input pins
Oscillation frequency		f_{OSC}	R_f = 1.0 MΩ ± 2%	V_{SS} = –5.0V	15	18	21	kHz	*9
			R_f = 1.0 MΩ ± 2%	V_{SS} = –3.0V	11	16	21		
Reset time		t_R			1.0	—	1000	µs	$\overline{RES}$

Notes:

*1. Operation over a wide range of voltages is guaranteed, except where a sudden voltage change occurs during access.

*2. Pins A0, D0 – D7, E ($\overline{RD}$), R/$\overline{W}$ ($\overline{WR}$) and $\overline{CS}$

*3. Pins CL, FR, M/S and $\overline{RES}$

*4. Pins D0 – D7

*5. Pin FR

*6. Pins A0, E ($\overline{RD}$), R/$\overline{W}$ ($\overline{WR}$), $\overline{CS}$, CL and $\overline{RES}$

*7. Applicable when pins D0 – D7 and FR are at high impedance.

*8. This value is current consumption when a vertical stripe pattern is written at t_{CYC}. Current consumption during access is nearly proportionate to access frequency (t_{CYC}). Only T_{DD} (1) is consumed while no access is made.

*9. Relationship between the oscillation frequency, frame and R_f (see Figures 5.1 – 5.3).

*10. Operating voltage ranges of V_{SS} and V5 (see Figure 5.4).

*11. Resistance with a voltage of 0.1V applied between the output pin (SEG, COM) and each power pin (V1, V2, V3, V4). It is specified within the operating voltage range.

*12, 13, 14. Current consumed by each discrete IC, not including LCD panel and wiring capacitances.

*12. Applicable to SED1520F$_{AA}$ and SED1521F$_{AA}$

*13. Applicable to SED1520F$_{0A}$

*14. Applicable to SED1521F$_{0A}$

*9 Relation between oscillation frequency, frame and R_f [SED1520F$_{0A}$]

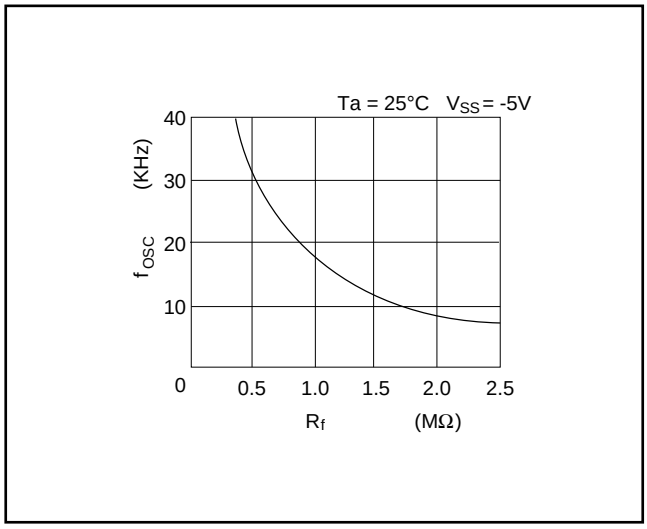

Figure 5.1

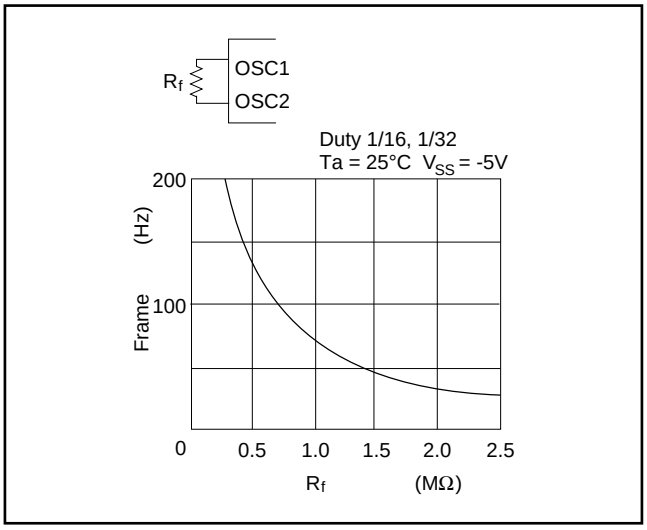

Figure 5.2

Relationship between external clock (f_{CL}) and frame [SED1520F$_{AA}$]

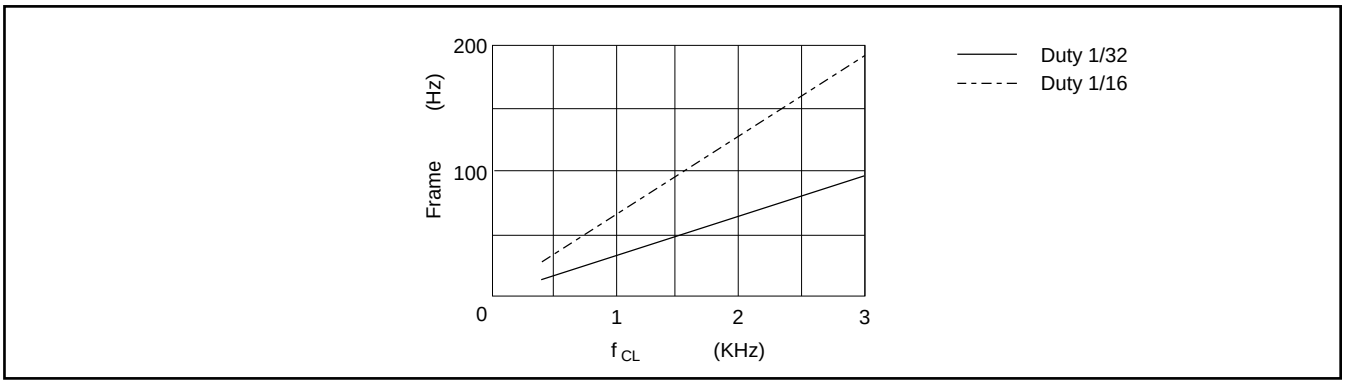

Figure 5.3

*10 Operating voltage range of V_{SS} and V5

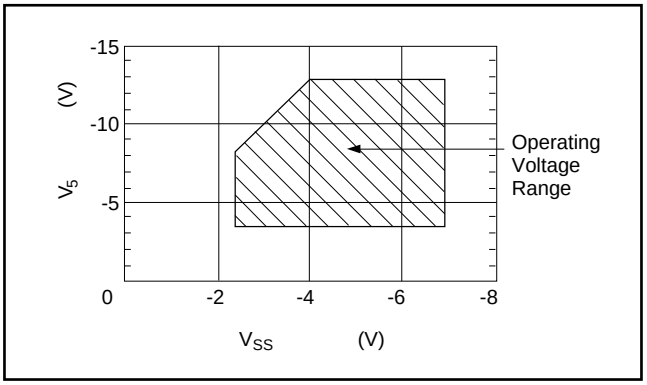

Figure 5.4

5.3 Timing Characteristics

5.3.1 System Bus Read/Write I (80-family MPU)

T_a = –20 to 75°C, V_{SS} = –5.0V ±10%

Parameter	Symbol	Signal	Condition	Min	Typ	Max	Unit
Address hold time	t_{AH8}	A0, $\overline{CS}$		10	—	—	ns
Address setup time	t_{AW8}			20	—	—	ns
System cycle time	t_{CYC8}	$\overline{WR}$, $\overline{RD}$		1000	—	—	ns
Control pulse width	t_{CC}			200	—	—	ns
Data setup time	t_{DS8}	D0 – D7		80	—	—	ns
Data hold time	t_{DH8}			10	—	—	ns
$\overline{RD}$ access time	t_{ACC8}		C_L = 100 pF	—	—	90	ns
Output disable time	t_{OH8}			10	—	60	ns

*1 Each of the values where V_{SS} = –3.0V is about 200% of that where V_{SS} = –5.0V (i.e., the listed value).

*2 The rise or fall time of input signals should be less than 15 ns.

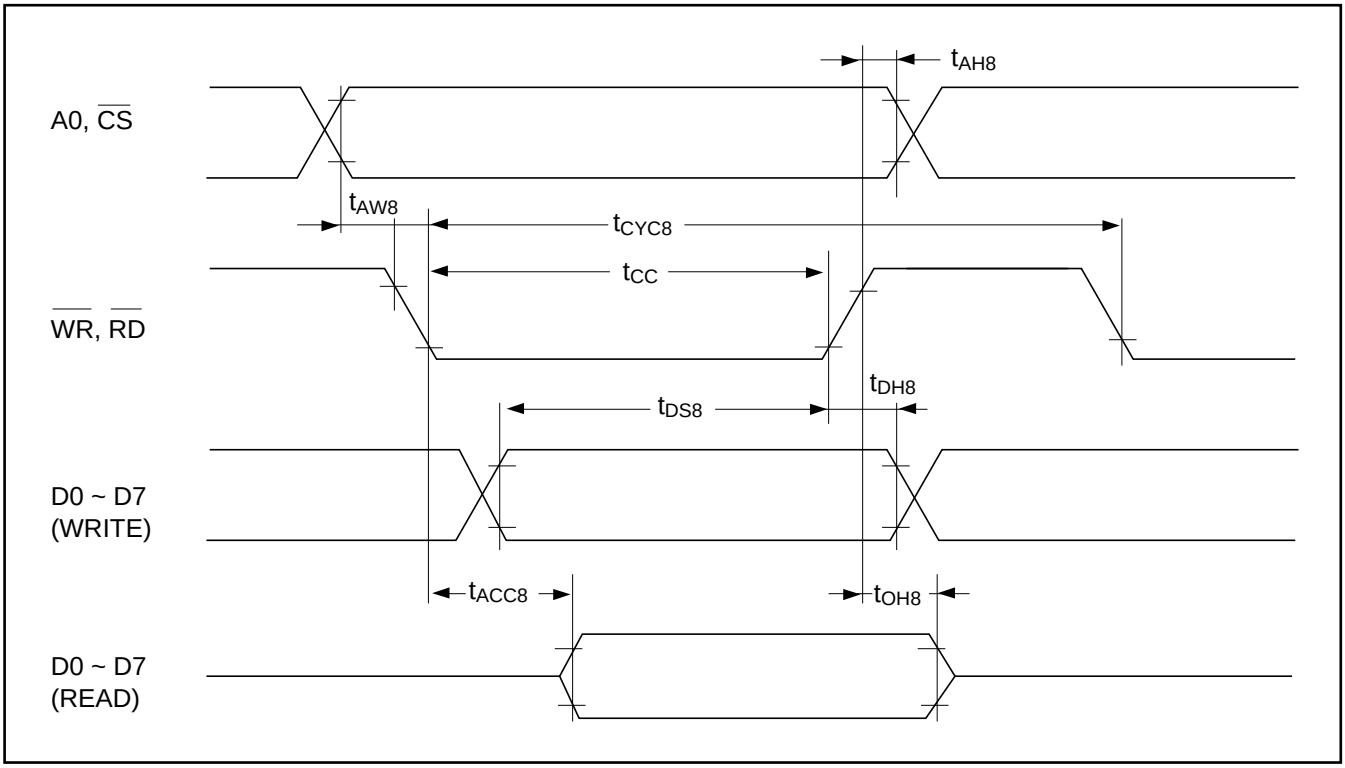

Figure 5.5. System bus read/write I (80-family MPU)

5.3.2 System Bus Read/Write II (68-family MPU)

T_a = –210 to 75°C, V_{SS} = –5.0V ±10%

Parameter	Symbol	Signal	Condition	Min	Typ	Max	Unit
System cycle time	t_{CYC6} *1	A0, $\overline{CS}$		1000	—	—	ns
Address setup time	t_{AW6}	R/$\overline{W}$		20	—	—	ns
Address hold time	t_{AH6}			10	—	—	ns
Data setup time	t_{DS6}	D0 – D7		80	—	—	ns
Data hold time	t_{DH6}			10	—	—	ns
Output disable time	t_{OH6}		CL = 100 pF	10	—	60	ns
Access time	t_{ACC6}			—	—	90	ns
Enable pulse width: Read	t_{EW}	E		100	—	—	ns
Enable pulse width: Write				80	—	—	ns

*1 t_{CYC6} indicates the cycle time during which $\overline{CS}$•E = “H”. It does not mean the cycle time of signal E.

*2 Each of the values where V_{SS} = –3.0V is about 200% of that where V_{SS} = –5.0V (i.e., the listed value).

*3 The rise or fall time of input signals should be less than 15 ns.

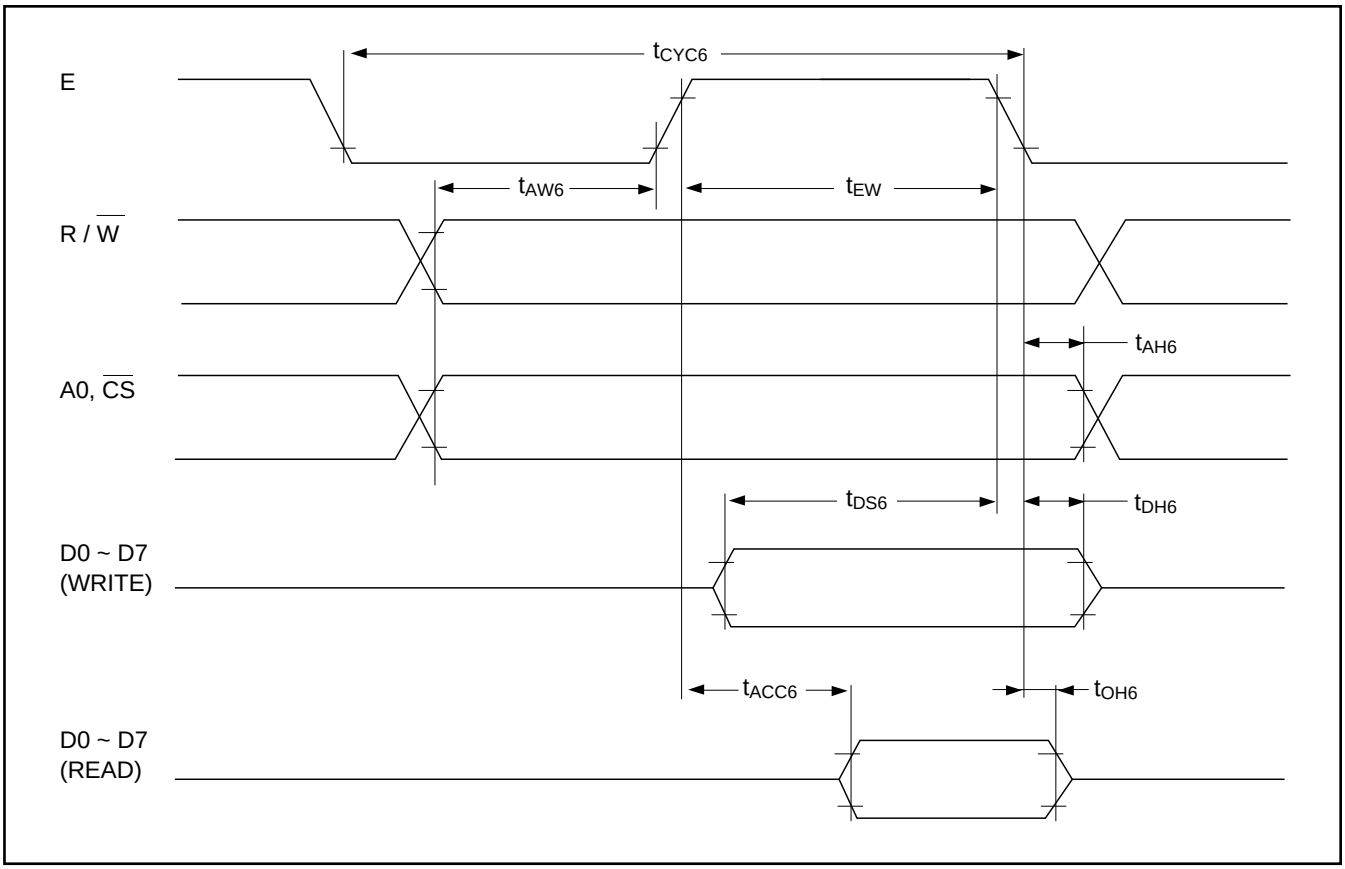

Figure 5.6. System bus read/write II (68-family MPU)

5.3.3 Display Control Timing

Input Timing

T_a = –20 to 75°C, V_{SS} = –5.0V ±10%

Parameter	Symbol	Signal	Condition	Min	Typ	Max	Unit
Low level pulse width	t_{WLCL}	CL		35	—	—	µs
High level pulse width	t_{WHCL}			35	—	—	µs
Rise time	t_r			—	30	150	ns
Fall time	t_f			—	30	150	ns
FR delay time	t_{DFR}	FR		–2.0	0.2	2.0	µs

Output Timing

T_a = –20 to 75°C, V_{SS} = –5.0V ±10%

Parameter	Symbol	Signal	Condition	Min	Typ	Max	Unit
FR delay time	t_{DFR}	FR	CL = 100 pF	—	0.2	0.4	µs

*1. The listed FR input delay time applies to the SED1521 and 1520 (slave).
The listed FR output delay time applies to the SED1520 (master).

*2. Each of the values where V_{SS} = –3.0V is about 200% of that where V_{SS} = –5.0V (i.e., the listed value).

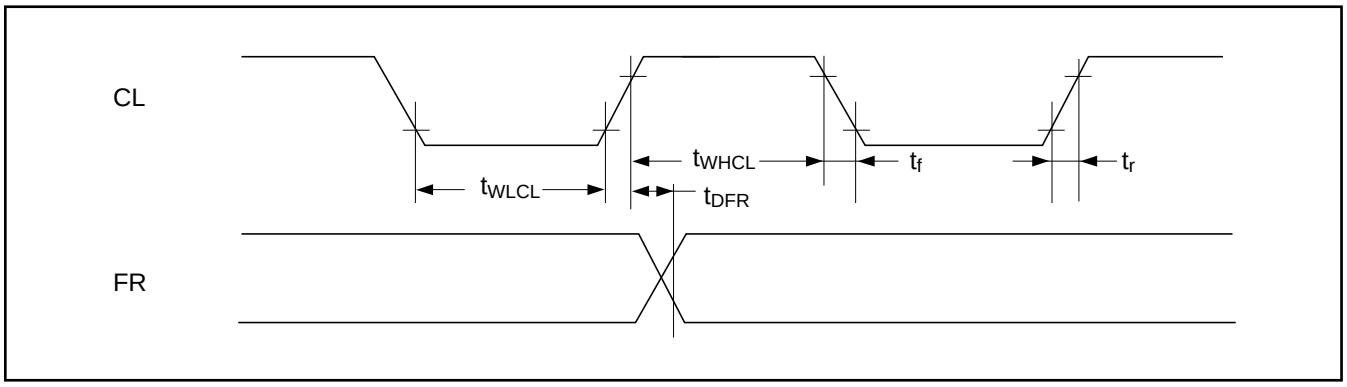

Figure 5.7. Display control timing

6.0
MPU Interface
(Reference)

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6.0 MPU Interface (Reference)

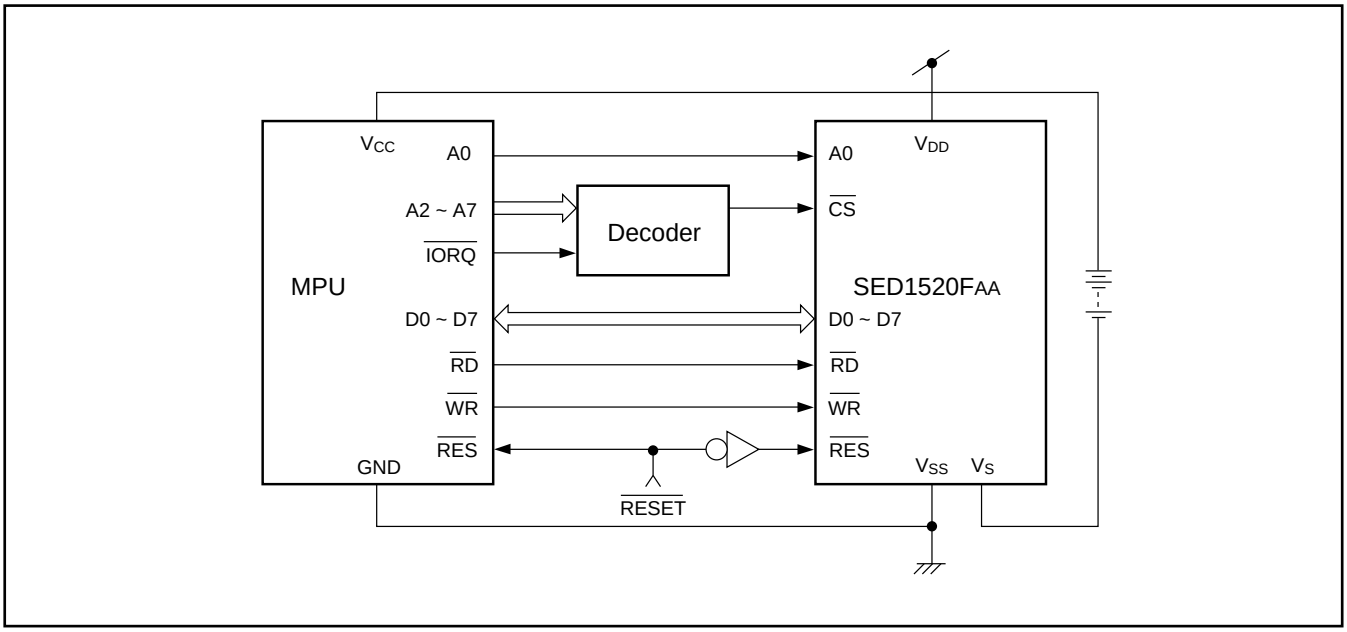

Figure 6.1. 80-family MPU

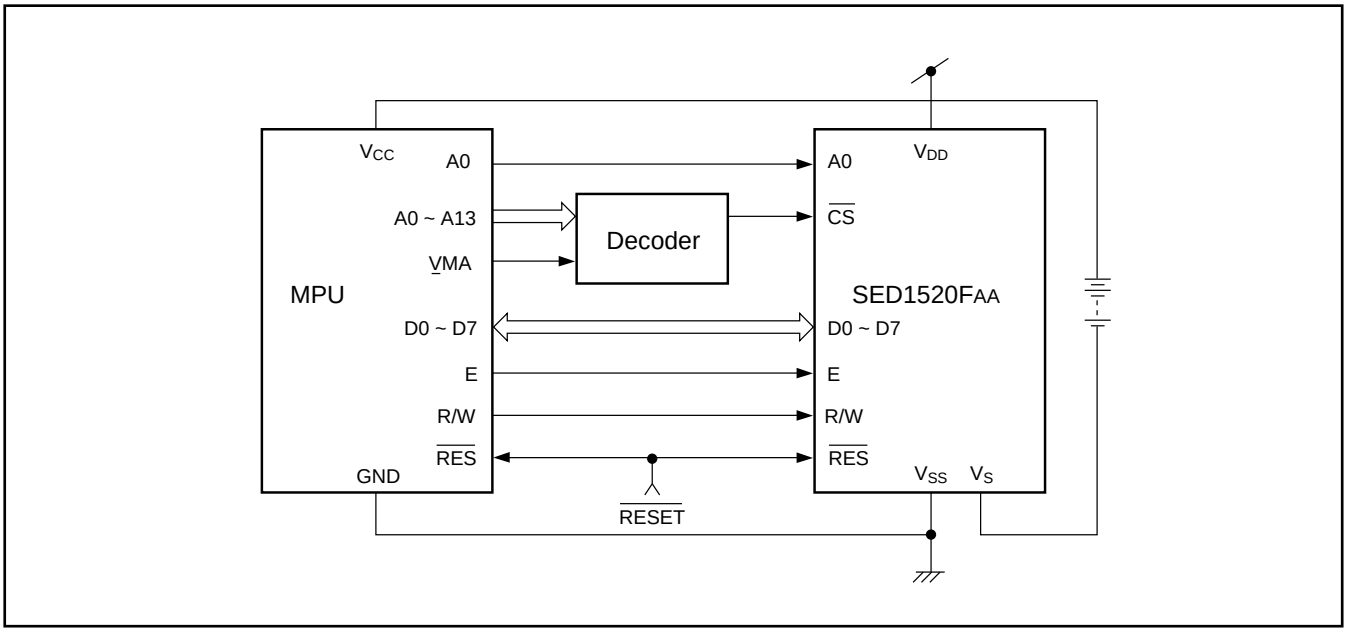

Figure 6.2. 68-family MPU

* These examples also apply to the SED1521F0A/ SED1521FAA.
* The SED1520F0A (containing an oscillator) does not have pin $\overline{CS}$. The output ORed with $\overline{CS}$ must be applied to pins A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/W).

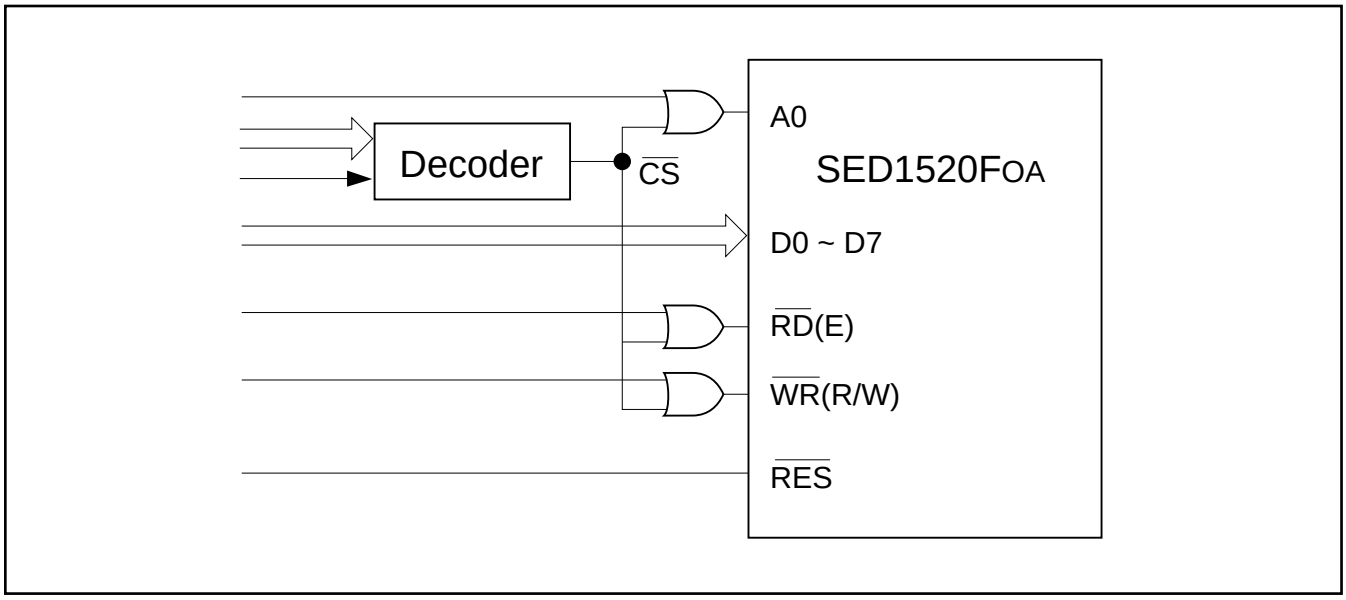

Figure 6.3

7.0
LCD Driver Interconnections

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7.0 LCD Driver Interconnections

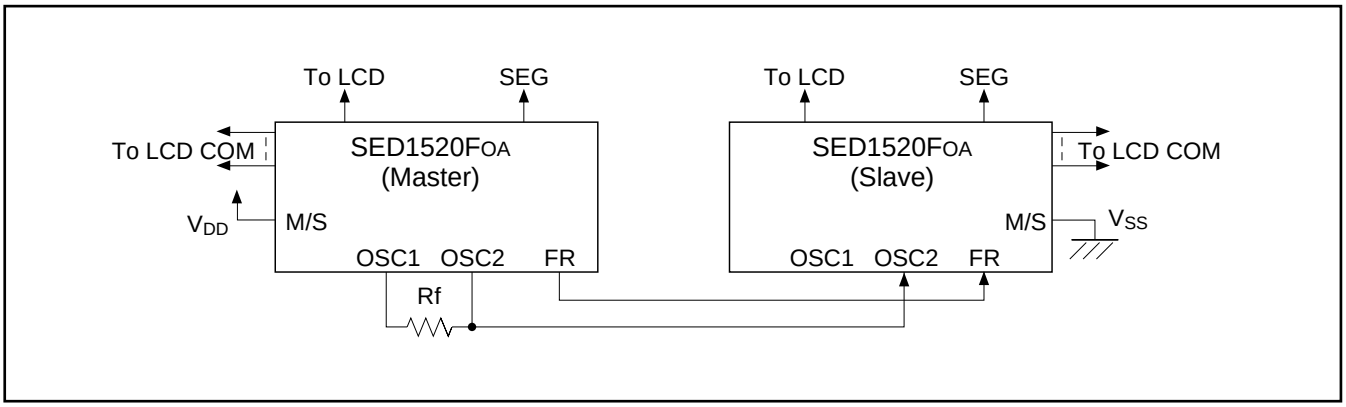

Figure 7.1. SED1520FOA – SED1520FOA

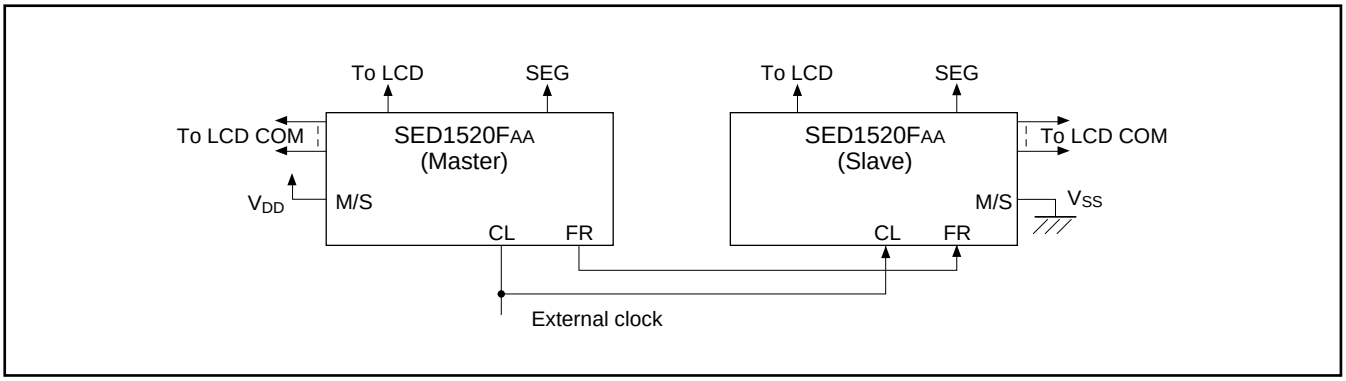

Figure 7.2. SED1520FAA – SED1520FAA

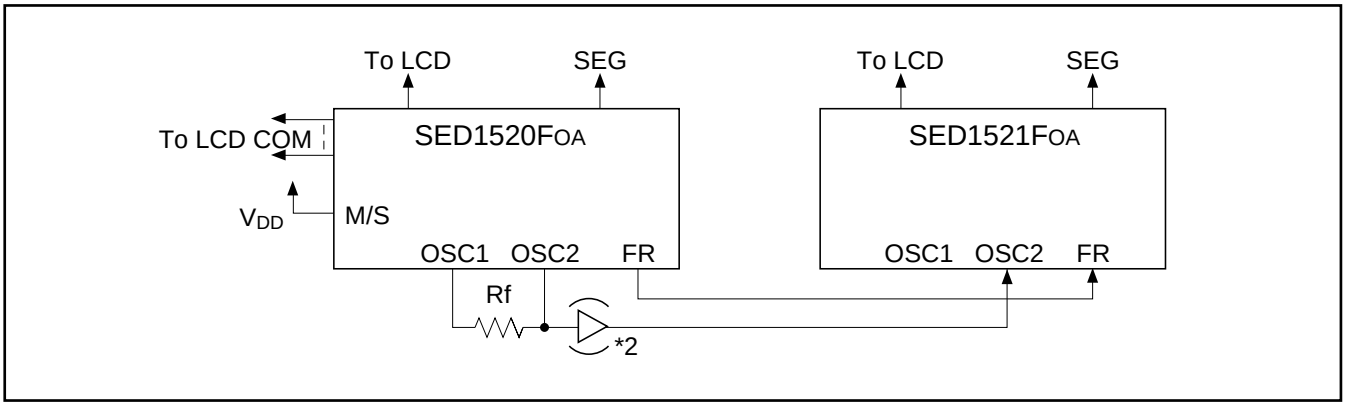

Figure 7.3 SED1520FOA – SED1521FOA *1

*1. In this connection, the duty of the SED1521FOA must be the same as that of the SED1520FOA.

*2. A CMOS buffer is neede for a system having two or more slave LSIs.

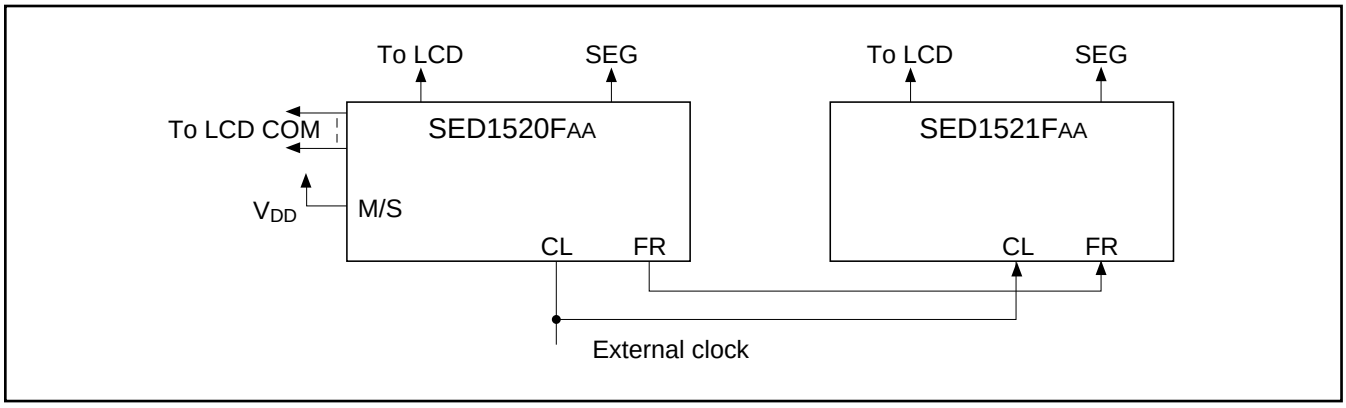

Figure 7.4. SED1520FAA – SED1521FAA

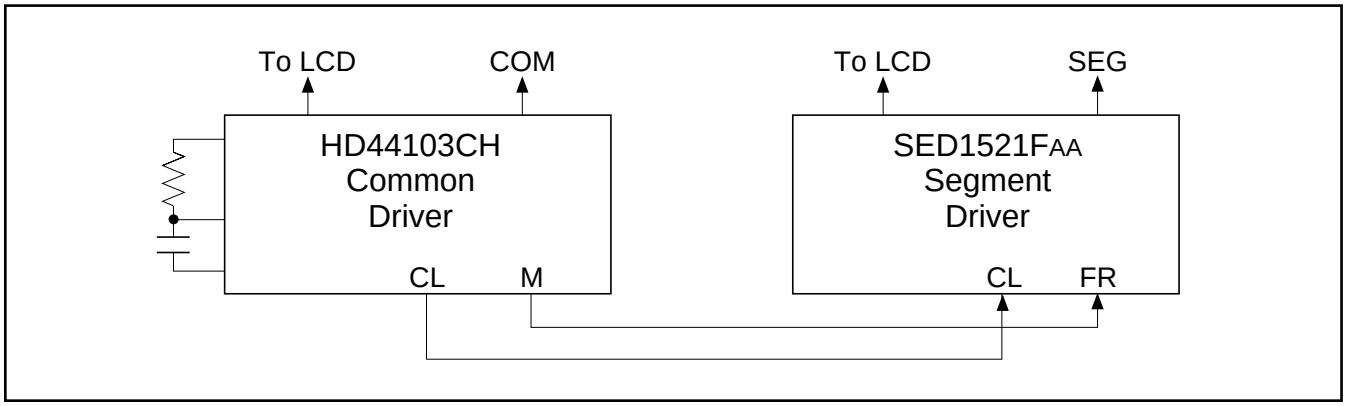

Figure 7.5. HD44103CH – SED1521FAA

*1. In this connection, the duty of the SED1521FOA must be the same as that of the SED1520FOA.

*2. A CMOS buffer is neede for a system having two or more slave LSIs.

8.0
Typical Connections with LCD Panel

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8.0 Typical Connections with LCD Panel

[Full dot LCD panel: 1 character = 6 × 8 dots]

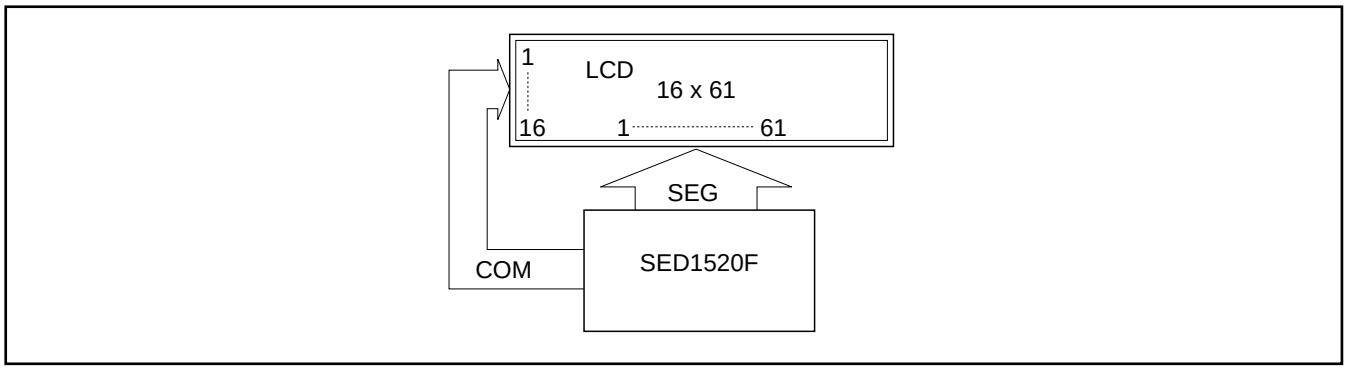

Figure 8.1. Duty 1/16, 10 characters × 2 lines

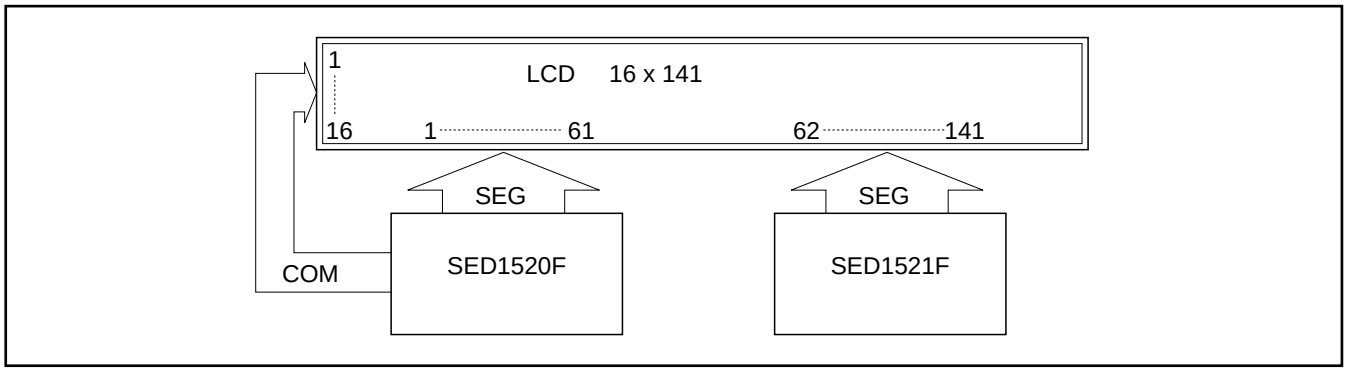

Figure 8.2. Duty 1/16, 23 characters × 2 lines

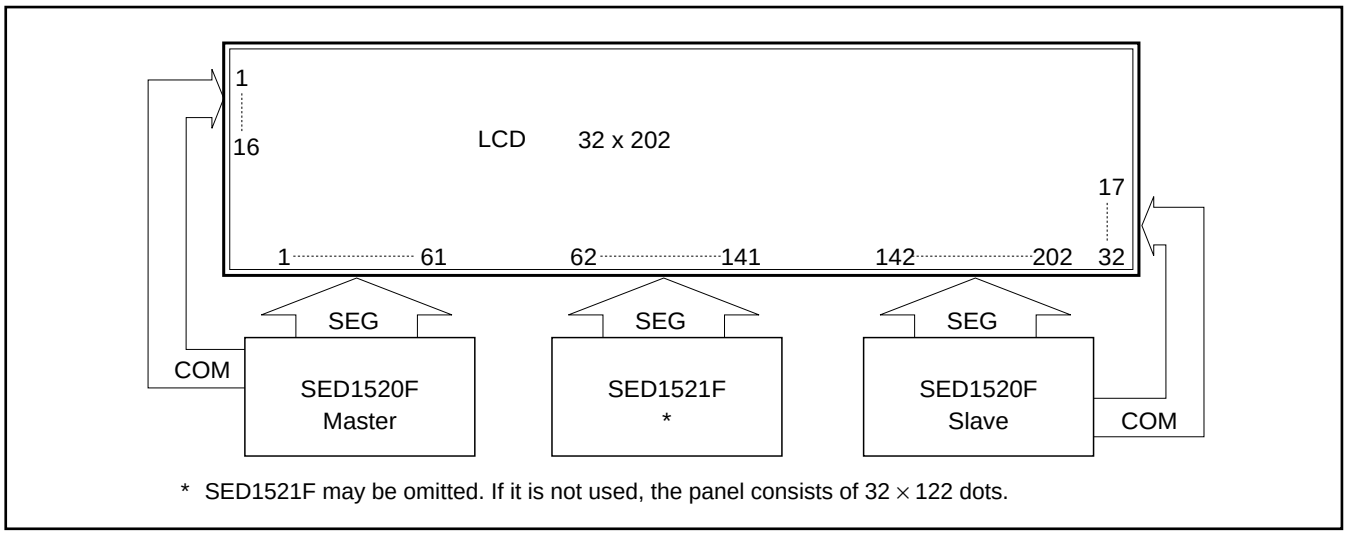

Figure 8.3. Duty 1/32, 33 characters × 4 lines

Note: Type AA (using external clock) and type 0A (containing an oscillator) cannot coexist for the same panel.

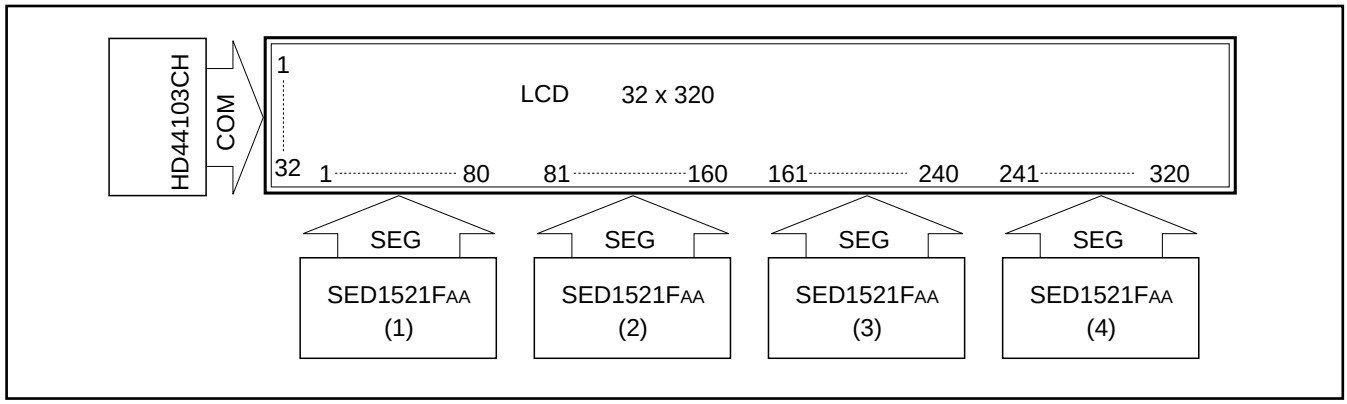

Figure 8.4. Duty 1/32, 20 kanji characters × 2 lines (kanji character 16 × 16 dots)

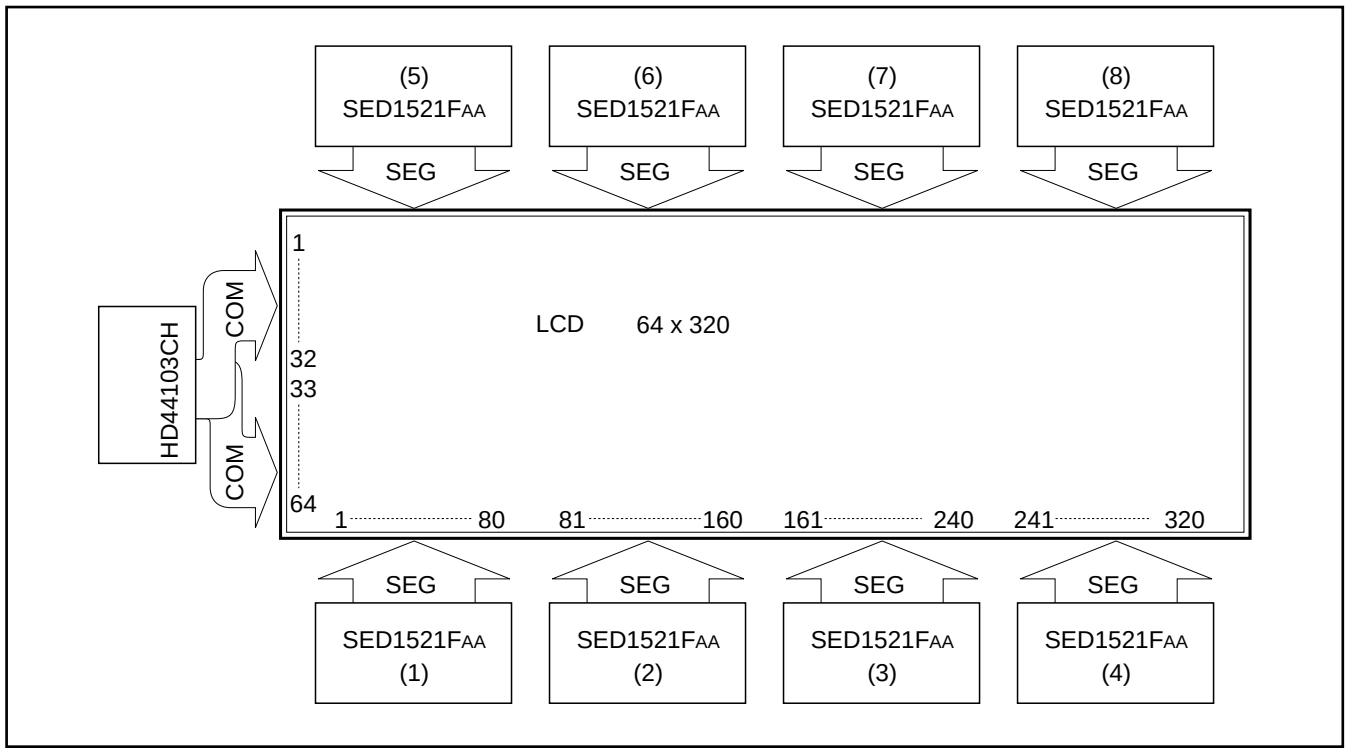

Figure 8.5. Duty 1/32, 2-screen display, 20 kanji characters × 4 lines

9.0
Package Dimensions (Reference)

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9.0 Package Dimensions (Reference)

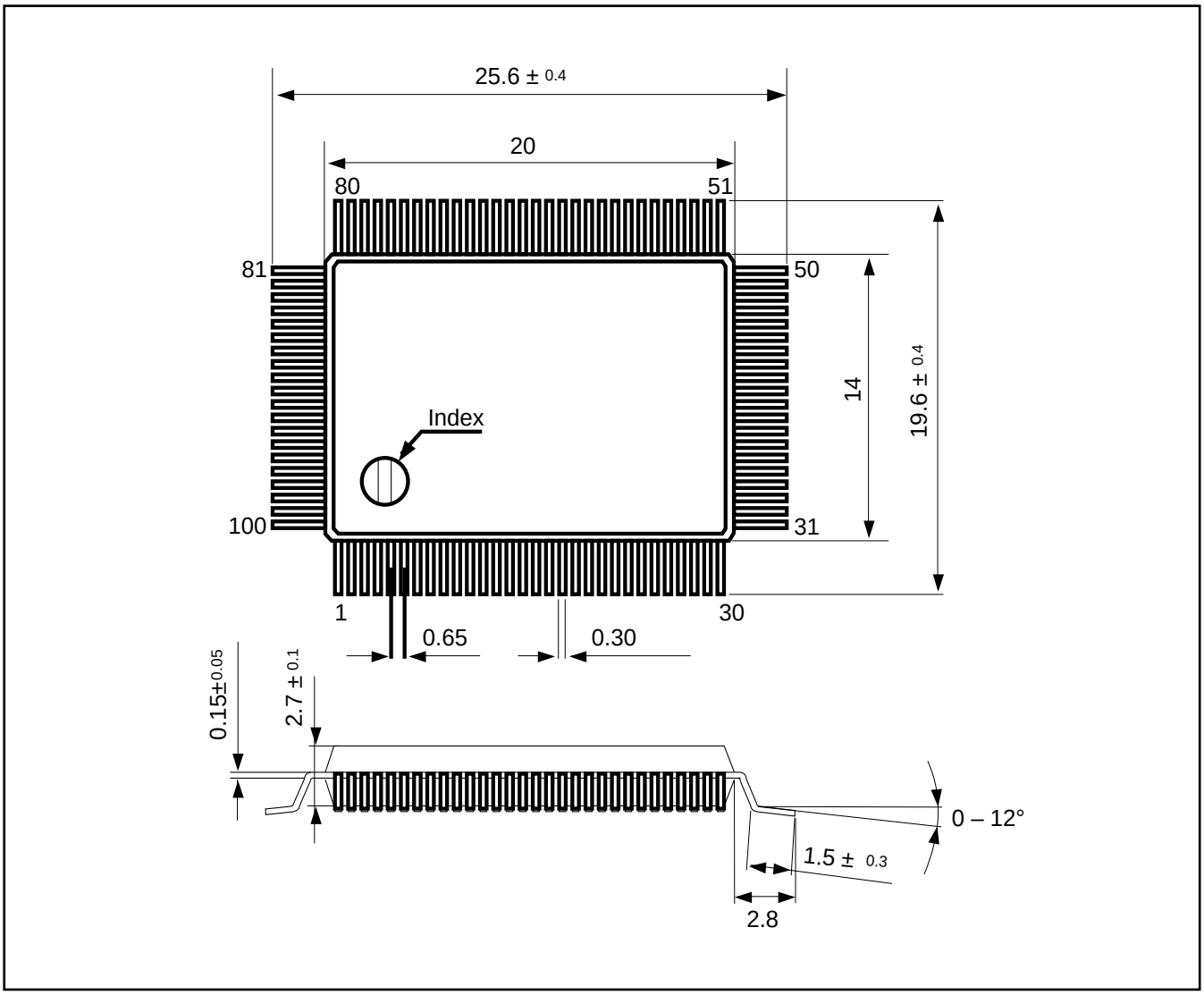

Figure 9.1. Package Dimensions

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