4. SED1526 Series

Contents

OVERVIEW

The SED1526 series is a single-chip LCD driver for dot-matrix liquid crystal displays (LCD's). It accepts serial or 8-bit parallel display data directly from a microprocessor and stores data in an on-chip display RAM. It can generate an LCD drive signal independent from microprocessor clock.

As the SED1526 series features the very low power dissipation and wide operating voltage range, it can easily realize a powerful but compact display unit having a small battery.

A single chip of SED1526 series can drive a 17×80-pixel or 33×64-pixel LCD panel.

(Note: The SED1526 series are not designed to have EMI resistance.)

FEATURES

- Direct data display using the display RAM. When RAM data bit is 0, it is not displayed; when 1, it is displayed.
- Large 80×33-bit RAM capacity
- On-chip LCD driver circuit (97 segment and common drivers)
- High-speed, 8-bit microprocessor interface allowing direct connection to both the 8080 and 6800
- Supported serial interface
- Rich command functions (upward compatible to SED 1520 Series); they are Read/Write Display Data, Display On/Off Switching, Set Page Address, Set Initial Display Line, Set Column Address, Read Status, Static Drive On/Off Switching, Select Duty, Duty+1, Read-Modify-Write, Select Segment Driver Direction, Power Save, Reset, Set Power Control, Set Electronic Controls, Clock Stop.
- On-chip CR oscillator circuit
- On-chip LCD power circuit (The on-chip and external LCD power supplies are software selectable.)
- Very low power consumption
- Flexible power voltages; 2.4 to 6.0 V (V_{DD}-V_{SS}) and -13.0 to -4.0 V (V_{DD}-V5)
- -40 to +85°C wide operating temperature range
- CMOS process
- 128-pin QFP5 package with aluminum pad or gold bump

Series Specifications (for 128-pin flat package)

Model	Operating clock (Internal OSC)	f_{CL} (TYP.)	Duty	Segment driver	Common driver	V_{REG} type	COM pin positions	QFP
SED1526F0A		2.9					Type A	
SED1526FBA		5.8				Type 1		
SED1526FAA		2.9	1/8, 1/9, 1/16, 1/17	80	17		Type B	5
SED1526FEA	20 kHz	2.9						
SED1526FEY		2.9				Type 2	Type A	26
SED1528F0A		2.9	1/32, 1/33	64	33	Type 1		5
SED1528DBB		5.8						—

V_{REG} type   Type 1 V_{REG} (Built-in power supply regulating voltage)
                            Temperature gradient: -0.17% /°C
                 Type 2 V_{REG} (Built-in power supply regulating voltage)
                            Temperature gradient: 0.00% /°C
COMS pin positions   Refer to No. P3 (Package pin layout), No. P4 (PAD layout) and No. P5 (PAD coordinates).

An SED1526 series package has one of following subcodes according to its package type (an example of SED1526):
     SED1526F∗∗:   128-pin QFP5 flat package
     SED1526F∗Y: 128-pin QFP26 flat package
     SED1526D∗∗:   Bear chip
                     SED1526D∗A having aluminum pad
                     SED1526D∗B having gold bump
     SED1526T∗∗:   TCP

BLOCK DIAGRAM (SED1526✽0✽)

EPSON
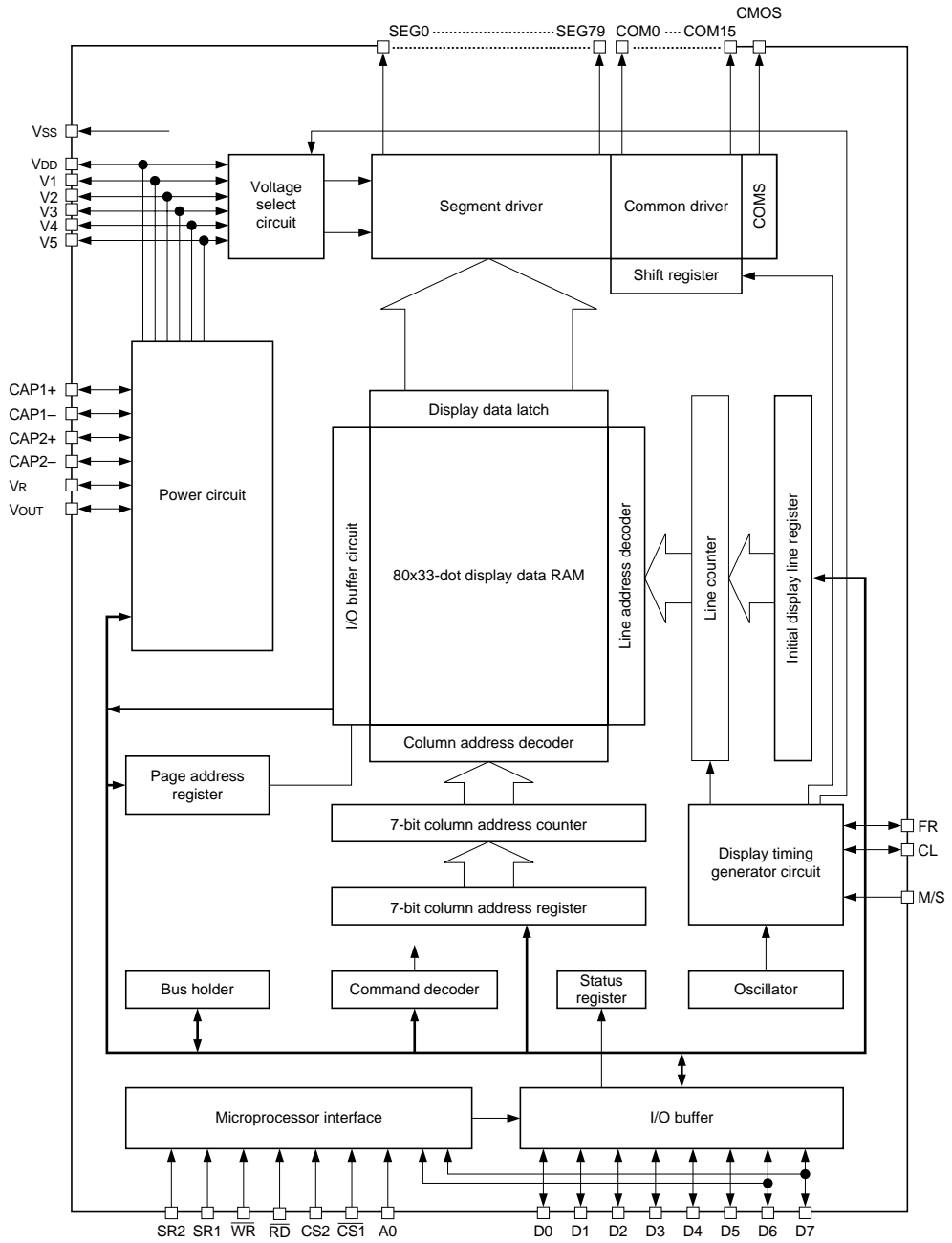
PIN ASSIGNMENT
Package Pin Assignment

Pad Layout

Top row (left to right): SEG53 SEG52 SEG51 SEG50 SEG49 SEG48 SEG47 SEG46 SEG45 SEG44 SEG43 SEG42 SEG41 SEG40 SEG39 SEG38 SEG37 SEG36 SEG35 SEG34 SEG33 SEG32 SEG31 SEG30 SEG29 SEG28 SEG27 SEG26 SEG25 SEG24 SEG23 SEG22 SEG21 SEG20 SEG19 SEG18 SEG17 SEG16

102   90   80   70   65

Left column:
- SEG54 — 103
- SEG55
- SEG56
- SEG57
- SEG58
- SEG59
- SEG60
- SEG61 — 110
- SEG62
- SEG63
- SEG64 (COM15)
- SEG65 (COM14)
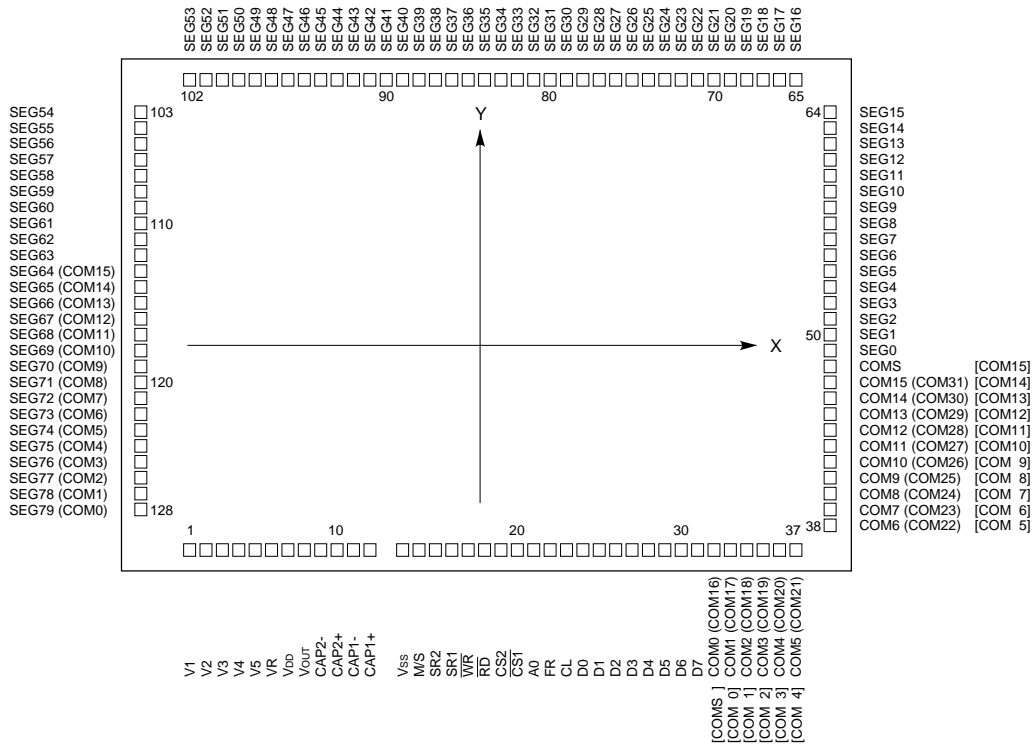- SEG66 (COM13)
- SEG67 (COM12)
- SEG68 (COM11)
- SEG69 (COM10)
- SEG70 (COM9)
- SEG71 (COM8) — 120
- SEG72 (COM7)
- SEG73 (COM6)
- SEG74 (COM5)
- SEG75 (COM4)
- SEG76 (COM3)
- SEG77 (COM2)
- SEG78 (COM1)
- SEG79 (COM0) — 128

Right column:
- 64 — SEG15
- SEG14
- SEG13
- SEG12
- SEG11
- SEG10
- SEG9
- SEG8
- SEG7
- SEG6
- SEG5
- SEG4
- SEG3
- SEG2
- SEG1
- 50 — SEG0
- COMS   [COM15]
- COM15 (COM31) [COM14]
- COM14 (COM30) [COM13]
- COM13 (COM29) [COM12]
- COM12 (COM28) [COM11]
- COM11 (COM27) [COM10]
- COM10 (COM26) [COM 9]
- COM9 (COM25)   [COM 8]
- COM8 (COM24)   [COM 7]
- COM7 (COM23)   [COM 6]
- COM6 (COM22)   [COM 5]
- 38

Y axis, X axis labels shown. 1   10   20   30   37

Bottom labels (left to right):
V1 V2 V3 V4 V5 VR V$_{DD}$ V$_{OUT}$ CAP2- CAP2+ CAP1- CAP1+ V$_{SS}$ M/S SR2 SR1 $\overline{WR}$ $\overline{RD}$ $\overline{CS2}$ $\overline{CS1}$ A0 FR CL D0 D1 D2 D3 D4 D5 D6 D7 COM0 (COM16) COM1 (COM17) COM2 (COM18) COM3 (COM19) COM4 (COM20) COM5 (COM21)

[COMS] [COM 0] [COM 1] [COM 2] [COM 3] [COM 4]

* Pin names in (   ) apply to SED1528.
* Pin names in [   ] apply to SED1526D$_A$* (CMOS pin = Type B).

Aluminum pad chip
- Chip size   5.92 mm × 4.68 mm
- Chip thickness   0.4 mm
- Pad opening   90.2 μm × 90.2 μm
- Pad pitch   130 μm (Min)

Gold bump chip (reference)
- Chip size   5.92 mm × 4.68 mm
- Chip thickness   0.4 mm
- Bump size   81.7 μm × 81.7 μm
- Bump height   22.5 μm

EPSON

Pad Coordinates

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	V$_1$	−2767	−2106	65	SEG16	2516	2185
2	V$_2$	−2637	−2106	66	SEG17	2367	2185
3	V$_3$	−2507	−2106	67	SEG18	2218	2185
4	V$_4$	−2377	−2106	68	SEG19	2088	2185
5	V$_5$	−2246	−2106	69	SEG20	1957	2185
6	V$_R$	−2116	−2149	70	SEG21	1827	2185
7	V$_{DD}$	−1985	−2176	71	SEG22	1697	2185
8	V$_{OUT}$	−1857	−2176	72	SEG23	1567	2185
9	CAP2−	−1727	−2176	73	SEG24	1437	2185
10	CAP2+	−1522	−2176	74	SEG25	1307	2185
11	CAP1−	−1318	−2176	75	SEG26	1177	2185
12	CAP1+	−1113	−2176	76	SEG27	1046	2185
13	V$_{SS}$	−553	−2166	77	SEG28	916	2185
14	M/S	−356	−2185	78	SEG29	786	2185
15	SR2	−226	−2185	79	SEG30	656	2185
16	SR1	−95	−2185	80	SEG31	526	2185
17	WR	35	−2185	81	SEG32	396	2185
18	RD	165	−2185	82	SEG33	266	2185
19	CS2	295	−2185	83	SEG34	135	2185
20	CS1	425	−2185	84	SEG35	5	2185
21	A0	555	−2185	85	SEG36	−125	2185
22	FR	719	−2185	86	SEG37	−255	2185
23	CL	849	−2185	87	SEG38	−385	2185
24	D0	979	−2185	88	SEG39	−515	2185
25	D1	1109	−2185	89	SEG40	−646	2185
26	D2	1239	−2185	90	SEG41	−776	2185
27	D3	1369	−2185	91	SEG42	−906	2185
28	D4	1500	−2185	92	SEG43	−1036	2185
29	D5	1630	−2185	93	SEG44	−1166	2185
30	D6	1760	−2185	94	SEG45	−1296	2185
31	D7	1890	−2185	95	SEG46	−1426	2185
32	COM0 (COM16) [CMOS]	2069	−2185	96	SEG47	−1557	2185
33	COM1 (COM17) [COM0]	2199	−2185	97	SEG48	−1687	2185
34	COM2 (COM18) [COM1]	2329	−2185	98	SEG49	−1817	2185
35	COM3 (COM19) [COM2]	2459	−2185	99	SEG50	−1947	2185
36	COM4 (COM20) [COM3]	2589	−2185	100	SEG51	−2077	2185
37	COM5 (COM21) [COM4]	2719	−2185	101	SEG52	−2226	2185
38	COM6 (COM22) [COM5]	2802	−1654	102	SEG53	−2375	2185
39	COM7 (COM23) [COM6]	2802	−1524	103	SEG54	−2802	1932
40	COM8 (COM24) [COM7]	2802	−1393	104	SEG55	−2802	1802
41	COM9 (COM25) [COM8]	2802	−1263	105	SEG56	−2802	1672
42	COM10 (COM26) [COM9]	2802	−1133	106	SEG57	−2802	1541
43	COM11 (COM27) [COM10]	2802	−1003	107	SEG58	−2802	1411
44	COM12 (COM28) [COM11]	2802	−873	108	SEG59	−2802	1281
45	COM13 (COM29) [COM12]	2802	−743	109	SEG60	−2802	1151
46	COM14 (COM30) [COM13]	2802	−612	110	SEG61	−2802	1021
47	COM15 (COM31) [COM14]	2802	−482	111	SEG62	−2802	891
48	COMS [COM15]	2802	−352	112	SEG63	−2802	760
49	SEG0	2802	−193	113	SEG64 (COM15)	−2802	599
50	SEG1	2802	−63	114	SEG65 (COM14)	−2802	469
51	SEG2	2802	67	115	SEG66 (COM13)	−2802	339
52	SEG3	2802	197	116	SEG67 (COM12)	−2802	209
53	SEG4	2802	327	117	SEG68 (COM11)	−2802	78
54	SEG5	2802	457	118	SEG69 (COM10)	−2802	−52
55	SEG6	2802	588	119	SEG70 (COM9)	−2802	−182
56	SEG7	2802	718	120	SEG71 (COM8)	−2802	−312
57	SEG8	2802	848	121	SEG72 (COM7)	−2802	−442
58	SEG9	2802	978	122	SEG73 (COM6)	−2802	−572
59	SEG10	2802	1108	123	SEG74 (COM5)	−2802	−703
60	SEG11	2802	1238	124	SEG75 (COM4)	−2802	−833
61	SEG12	2802	1368	125	SEG76 (COM3)	−2802	−963
62	SEG13	2802	1499	126	SEG77 (COM2)	−2802	−1093
63	SEG14	2802	1629	127	SEG78 (COM1)	−2802	−1223
64	SEG15	2802	1759	128	SEG79 (COM0)	−2802	−1353

* Pin names in (   ) apply to SED1528.
* Pin names in [   ] apply to SED1526D$_A$* (CMOS pin = Type B).

PIN DESCRIPTION

Power Supply

Name	I/O	Description	Number of pins
V_{DD}	Supply	+5VDC power supply. Common to microprocessor power supply pin V_{CC}.	1
V_{SS}	Supply	Ground	1
V_1, V_2 V_3, V_4 V_5	Supply	LCD driver supply voltages. The Set Power Control command can switch the on-chip and external power supply modes of these pins. When external mode selects, the voltage determined by LCD cell is impedance-converted by a resistive divider or an operational amplifier for application. Voltages should be the following relationship: $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ When master mode selects, these voltages are generated on the chip: 		SED1526	SED1528	 	---	---	---	 	V1	1/5 V_5	1/7 V_5	 	V2	2/5 V_5	2/7 V_5	 	V3	3/5 V_5	5/7 V_5	 	V4	4/5 V_5	6/7 V_5		5

LCD Driver Supplies

Name	I/O	Description	Number of pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connection	1
CAP1−	O	DC/DC voltage converter capacitor 1 negative connection	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connection	1
CAP2−	O	DC/DC voltage converter capacitor 2 negative connection	1
V_{OUT}	O	DC/DC voltage converter output	1
V_R	I	Voltage adjustment pin. Applies voltage between V_{DD} and V_5 using a resistive divider.	1

Microprocessor Interface

Name	I/O	Description	Number of pins
D0 to D7 (SI) (SCL)	I/O	Data input/outputs. The 8-bit bidirectional data buses to be connected to the standard 8-bit microprocessor data buses. When the serial interface selects, D7 is serial data input (SI) and D6 is serial clock input (SCL).	8
A0	I	Control/display data flag input. It is connected to the LSB of micro-processor address bus. When low, the data on D0 to D7 is control data. When high, the data on D0 to D7 is display data.	1
$\overline{CS1}$ CS2	I	Chip select input. Data input/output is enabled when -CS1 is low and CS2 is high.	2
$\overline{RD}$ (E)	I	• Read enable input. When interfacing to an 8080-series microprocessor and when its $\overline{RD}$ is low, the SED1526 series data bus output is enabled. • When interfacing to an 6800-series microprocessor and when its R/$\overline{W}$ Enable (E) is high, the SED1526 series R/$\overline{W}$ input is enabled.	1
$\overline{WR}$ (R/$\overline{W}$)		• Write enable input. When interfacing to an 8080-series microprocessor, $\overline{WR}$ is active low. • When interfacing to an 6800-series microprocessor, it will be read mode when R/$\overline{W}$ is high and it will be write mode when R/$\overline{W}$ is low. R/$\overline{W}$ = "1" : Read R/$\overline{W}$ = "0" : Write	1

Name	I/O	Description	Number of pins
SR1, SR2	I	Microprocessor interface select, and parallel/serial data input select. <table><tr><td>SR1</td><td>SR2</td><td>Type</td></tr><tr><td>0</td><td>1</td><td>8080 microprocessor bus (parallel input)</td></tr><tr><td>1</td><td>1</td><td>6800 microprocessor bus (parallel input)</td></tr><tr><td>1</td><td>0</td><td>Serial input</td></tr><tr><td>0</td><td>0</td><td>Reset</td></tr></table> * In serial mode, no data can be read from RAM and D0 to D5 are HZ. $\overline{RD}$ and $\overline{WR}$ must be high or low. When set for the 68 family MPU, the SR1 and SR2 timing must match or SR1 must rise first.	2

LCD Driver Outputs

| Name	I/O	Description	Number of pins
M/S	I	Normally "1".	1
CL	I/O	Normally "1".	1
FR	I/O	Normally "1".	1
SEGn	O	LCD segment driver output. V_{DD}, V_2, V_3, or V_5 can select according to the display RAM and FR signal. <table><tr><td>RAM data</td><td>FR signal</td><td>Output voltage of SEGn</td></tr><tr><td rowspan="2">1</td><td>1</td><td>V_{DD}</td></tr><tr><td>0</td><td>V_5</td></tr><tr><td rowspan="2">0</td><td>1</td><td>V_2</td></tr><tr><td>0</td><td>V_3</td></tr><tr><td>Power save</td><td>–</td><td>V_{DD}</td></tr></table>	80 (SED1526) or 64 (SED1528)
COMn	O	LCD common driver output. V_{DD}, V_1, V_4, or V_5 can select according to IC internal scan signal and FR signal. The common scan sequence is reversed in slave mode. <table><tr><td>Internal scan signal</td><td>FR signal</td><td>Output voltage of COMn</td></tr><tr><td rowspan="2">1</td><td>1</td><td>V_5</td></tr><tr><td>0</td><td>V_{DD}</td></tr><tr><td rowspan="2">0</td><td>1</td><td>V_1</td></tr><tr><td>0</td><td>V_4</td></tr><tr><td>Power save</td><td>–</td><td>V_{DD}</td></tr></table>	16 (SED1526) or 32 (SED1528)
COMS	O	Indicator COM output. COMS pin is equivalent to following COM output pin when Duty+1 command is running: <table><tr><td></td><td colspan="2">SED1526</td><td>SED1528</td></tr><tr><td></td><td>1/9 duty</td><td>1/17 duty</td><td>1/33 duty</td></tr><tr><td>Indicator COMS output</td><td>COM8</td><td>COM16</td><td>COM32</td></tr></table>	1

FUNCTIONAL DESCRIPTION

Microprocessor Interface

Parallel/Serial Interface

The SED1526 series can transfer data via 8-bit bidirectional data buses D0 to D7 or via serial data input D7 (SI). The 8-bit parallel data input or serial data input, 8080/6800-series microprocessor, and reset status can select according to SR1 and SR2.
No data can be read from RAM and no status can be read during serial data input. Also, $\overline{RD}$ and $\overline{WR}$ are high or low, and D0 to D5 are open.

Table 1

SR1	SR2	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	Data (D0 to D7)
0	1	8080 microprocessor bus (parallel)	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
1	1	6800 microprocessor bus (parallel)	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
1	0	Serial input	$\overline{CS1}$	CS2	A0	0/1	0/1	D6 (SCL) and D7 (SI)
0	0	Reset	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	— — — — — — —

* When set for the 68 family interface, the SR1 and SR2 timing must match or SR1 must rise first.
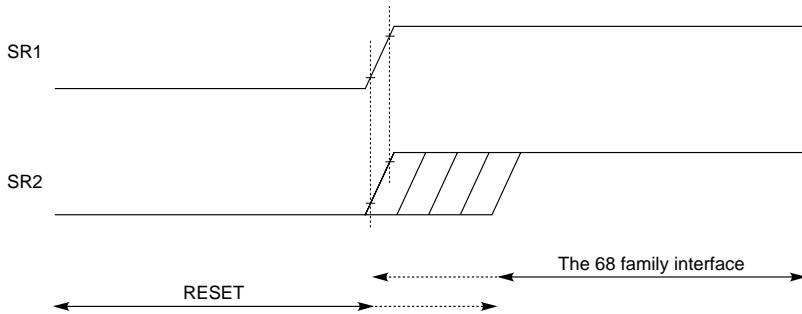
Data Bus Signals

The SED1526 series identifies the data bus signal according to A0, $\overline{RD}$, and $\overline{WR}$ (E, R/$\overline{W}$) signals.

Table 2

Common	6800 processor	8080 processor		Function
A0	$\overline{WR}$ (R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (commands)

Serial Interface (SR1 is high and SR2 is low)

The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data input and serial clock input are enabled when $\overline{CS1}$ is low and CS2 is high (in chip select status). When chip is not selected, the shift register and counter are reset.
When serial data input is enabled by SR1 and SR2, D7 (SI) receives serial data and D6 (SCL) receives serial clock. Serial data of D7, D6, ..., D0 is read at D7 in this sequence when serial clock goes high. They are converted into 8-bit parallel data and processed on rising

edge of every eighth serial clock signal.
The serial data input is determined to be the display data when A0 is high, and it is control data when A0 is low. A0 is read on rising edge of every eighth clock signal.
Figure 1 shows a timing chart of serial interface signals. The serial clock signal must be terminated correctly against termination reflection and ambient noise. Operation checkout on the actual machine is recommended.
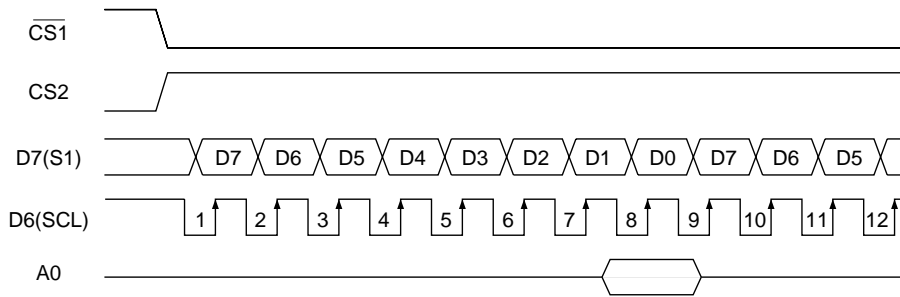
Figure 1

Chip Select Inputs

The SED1526 series can interface to microprocessor when $\overline{CS1}$ is low and CS2 is high.

When these pins are set to any other combination, D0 to D7 are high impedance. A0, $\overline{RD}$, and $\overline{WR}$ input are disabled. However, the reset signal is entered regardless of $\overline{CS1}$ and CS2 setup. The internal IC status including LCD driver circuit is held until a reset signal is entered.

Access to Display Data RAM and Internal Registers

The SED1526 series can perform a series of pipeline processing between LSI's using bus holder of internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in bus holder, and outputs it onto system bus in the next data read cycle. Also, the microprocessor temporarily stores display data in bus holder, and stores it in display RAM until the next data write cycle starts.

When viewed from the microprocessor, the SED1526 series access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC} and t_{DS}). It shows the data transfer speed to/from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure 2).
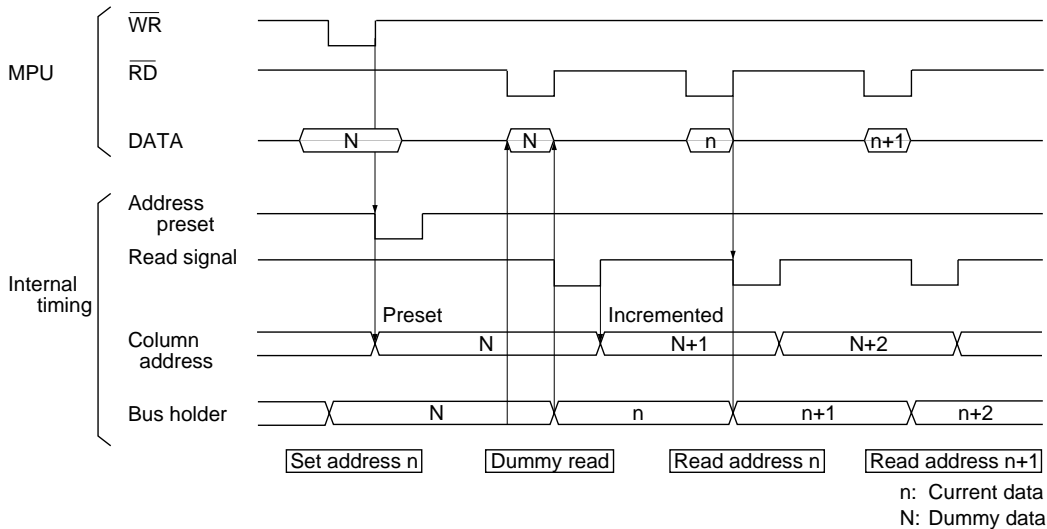
•**Write**

•**Read**

n: Current data
N: Dummy data
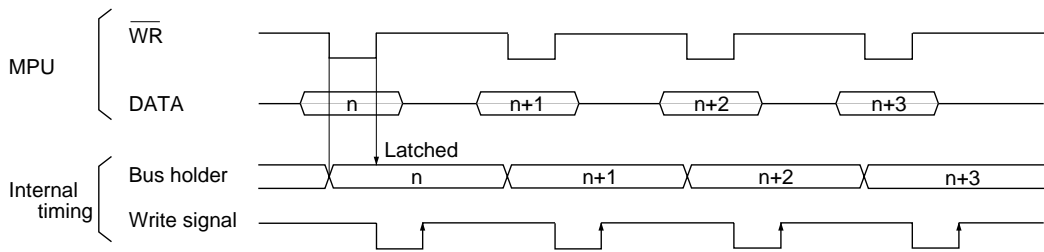
Figure 2

Busy Flag

The Busy flag is set when the SED1526 series starts to operate. During operating, it accepts Read Status instruction only. The busy flag signal is output at pin D7 when Read Status is issued. If the cycle time (t_{cyc}) is correct, the microprocessor needs not to check the flag before issuing a command. This can greatly improve the microprocessor performance.

Initial Display Line Register

When the display RAM data is read, the display line according to COM0 (usually, the top line of screen) is determined using register data. The register is also used for screen scrolling and page switching.

The Set Display Start Line command sets the 5-bit display start address in this register. The register data is preset on the line counter each time FR signal status changes. The line counter is incremented by oscillator circuit output (in master mode) or CL input (in slave mode), and it generates a line address to allow 80-bit sequential data output from display RAM to LCD driver circuit.

Column Address Counter

This is a 7-bit presettable counter that provides column address to the display RAM (refer to Figure 4). It is incremented by 1 when a Read/Write command is entered. However, the counter is not incremented but locked if a non-existing address above 50H is specified. It is

unlocked when a column address is set again. The Column Address counter is independent of Page Address register.

When ADC Select command is issued to display inverse display, the column address decoder inverts the relationship between RAM column address and display segment output.

Page Address Register

This is a 4-bit page address register that provides page address to the display RAM (refer to Figure 4). The microprocessor issues Set Page Address command to change the page and access to another page. Page address 4 (D2 is high, but D0 and D1 are low) is RAM area dedicate to the indicator, and display data D0 is only valid.

Display Data RAM

The display data RAM stores pixel data for LCD. It is a 33-column by 80-row (4-page by 8+1 bit) addressable array. Each pixel can be selected when page and column addresses are specified.

The time required to transfer data is very short because the microprocessor enters D0 to D7 corresponding to LCD common lines as shown in Figure 3. Therefore, multiple SED1526's can easily configure a large display having the high flexibility with very few data transmission restriction.

The microprocessor writes and reads data to/from the RAM through I/O buffer. As LCD controller operates independently, data can be written into RAM at the same time as data is being displayed, without causing the LCD to flicker.
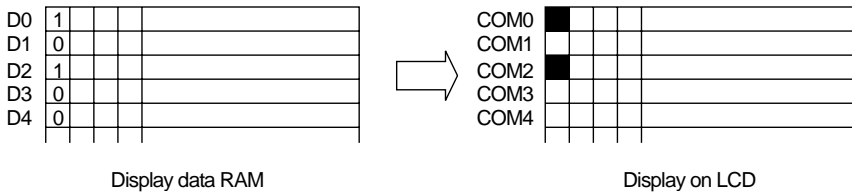

Display data RAM   Display on LCD

Figure 3

Relationship between display data RAM and addresses (if initial display line is 08):

Page address	Data	Display (Page)	Line address		COM output
D2,D1,D0 =0,0,0	D0	Page 0	00		COM 0
	D1		01		COM 1
	D2		02		COM 2
	D3		03		COM 3
	D4		04		COM 4
	D5		05		COM 5
	D6		06		COM 6
	D7		07		COM 7
0,0,1	D0	Page 1	08	Start	COM 8
	D1		09		COM 9
	D2		0A		COM10
	D3		0B	1/8	COM11
	D4		0C		COM12
	D5		0D		COM13
	D6		0E		COM14
	D7		0F		COM15
0,1,0	D0	Page 2	10		COM16
	D1		11		COM17
	D2		12		COM18
	D3		13	1/16	COM19
	D4		14		COM20
	D5		15		COM21
	D6		16		COM22
	D7		17		COM23
0,1,1	D0	Page 3	18		COM24
	D1		19		COM25
	D2		1A		COM26
	D3		1B		COM27
	D4		1C		COM28
	D5		1D		COM29
	D6		1E		COM30
	D7		1F		COM31
1,0,0	D0	Page 4			COM S

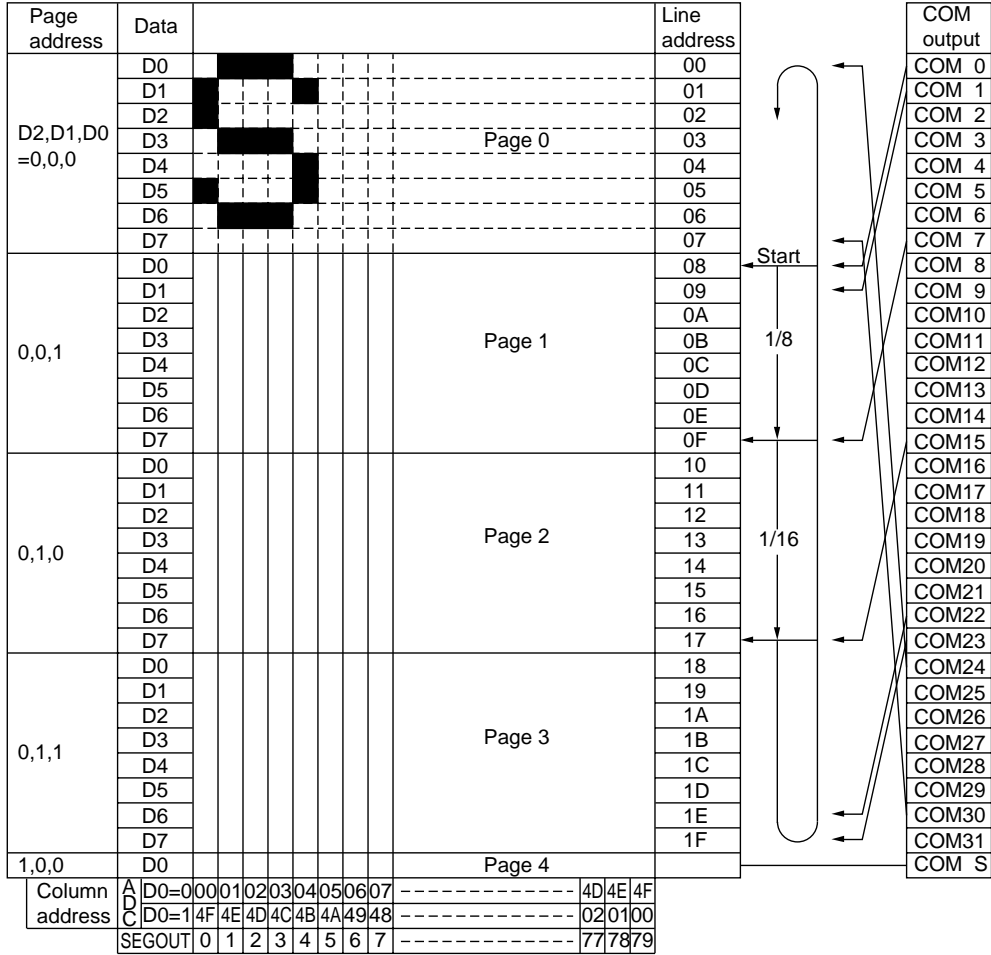| Column address														
ADC	D0=0	00	01	02	03	04	05	06	07	-------------	4D	4E	4F	
	D0=1	4F	4E	4D	4C	4B	4A	49	48	-------------	02	01	00	
	SEGOUT	0	1	2	3	4	5	6	7	-------------	77	78	79	

Figure 4

Display Timing Generator Circuit

This section explains how the display timing generator circuit operates.

### Signal generation to line counter and display data latch circuit

The line address counter, RAM, and latch circuit of the SED1526 series operate synchronous to the display clock (the oscillator circuit outp).mm The LCD drive signal is sent to LCD panel driver output pin SEGn.

The timing of LCD panel driver outputs is independent of the timing of RAM data input from microprocessor.

LCD AC Signal (FR)

The LCD AC signal, FR, is generated from the display clock. The FR controller generates dual-frame AC driver waveforms for LCD panel driver circuit.

• **Dual-frame AC driver waveforms**
(If SED1526 is used in 1/16 duty)
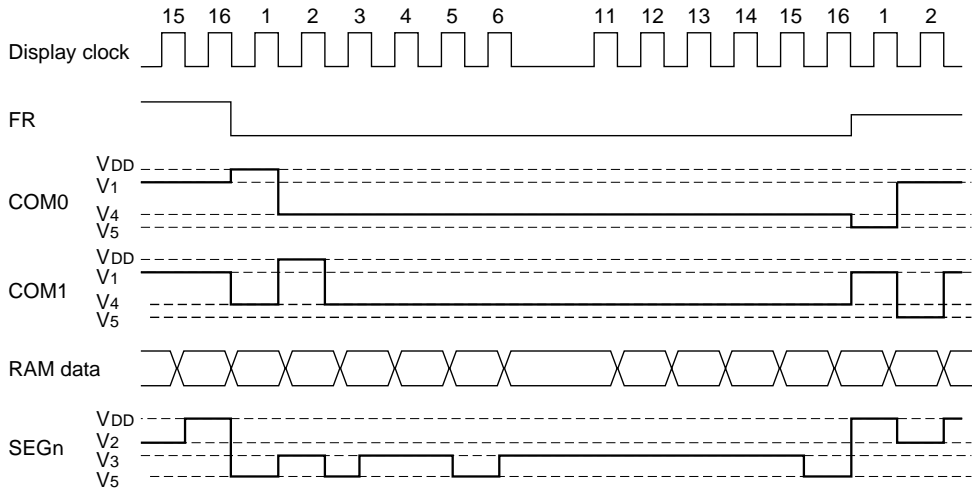
Common timing Signals

The common timing generator circuit uses the display clock to generate common timing signal and FR frame signal. The Duty Select command can select 1/8 or 1/16 duty (SED1526). A combination of Select Duty and Duty+1 commands can select 1/9 or 1/17 duty (SED1526).

Display Data Latch Circuit

This circuit temporarily stores (or latches) display data (during a single common signal period) when it is output from display RAM to LCD panel driver circuit. This latch is controlled by Display ON/OFF and Static Drive ON/OFF commands. These commands do not alter the data.

LCD Driver

This is a multiplexer circuit consisting of 96 segment outputs to generate four-level LCD panel drive signals. The circuit also has a pair of COM outputs for indicator display.

The COMn output has a shift register to sequentially output COM scan signals. The LCD panel drive voltage is generated by a specific combination of display data, COM scan signal, and FR signal. Figure 6 gives an example of SEG and COM output waveforms.

Oscillation Circuit

This is a low power consumption CR oscillator having an oscillator resistor, and its output is used as the display timing signal source or as the clock for voltage boost circuit of LCD power supply.

The display clock output can be stopped by Clock Stop command to minimize the current consumption of LCD panel.

Power Supply Circuit

The power supply circuit produces voltage to drive LCD panel at low power consumption. The power circuit consists of three subcircuits: voltage tripler, voltage regulator, and voltage follower. The voltage tripler outputs V_{DD} -($V_{SS} \times 2$) or -($V_{SS} \times 3$) voltage at V_{OUT}. The regulator circuit generates V_5 voltage using external resistor. The voltage follower circuit changes the impedance of V_1 to V_4 that are generated from V_5 through division with internal resistors. (Details are explained later.)

SED1526 series can drive LCD panel using on-chip power circuit. However, the on-chip power circuit is intended to use for a small LCD panel and it is inappropriate to a large panel requiring multiple driver chips. As the large LCD panel has the dropped display quality due to large load capacity, it must use an external power source.

The power circuit is controlled by Set Power Control command. This command sets a three-bit data in Power Control register to select one of eight power circuit functions. The external power supply and part of on-chip power circuit functions can be used simultaneously. The following explains how the Set Power Control command works.

[Control by Set Power Control command]

D2 turns on when triple booster control bit goes high, and D2 turns off when this bit goes low.

D1 turns on when voltage regulator control bit goes high, and D1 turns off when this bit goes low.

D0 turns on when voltage follower control bit goes high, and D0 turns off when this bit goes low.

[Practical combination examples]

D2 D1 D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Voltage booster terminal	Voltage regulator terminal
1 1 1	ON	ON	ON	—	Used	Used
1 0 0	ON	OFF	OFF	—	Used	OPEN
0 1 1	OFF	ON	ON	To V_{OUT}	OPEN	Used
0 0 0	OFF	OFF	OFF	To V_1 to V_5	OPEN	OPEN

To use the on-chip (internal) power supply only, set $(D2,D1,D0)=(1,1,1)$.

To use the voltage booster circuit only, set $(D2,D1,D0)=(1,0,0)$.

To use the voltage regulator and voltage follower, set $(D2,D1,D0)=(0,1,1)$.

To use an external power supply only, set $(D2,D1,D0)=(0,0,0)$.

Notes: 1. The voltage booster terminals are CAP1+, CAP1-, CAP2+, and CAP2-.
2. The above listed examples are the most practical use to control each circuit using control bits. Any other setup is unpractical and omitted in this manual.
3. The V/F circuit alone cannot be used. When this circuit is used, the V adjustment circuit must be set simultaneously.
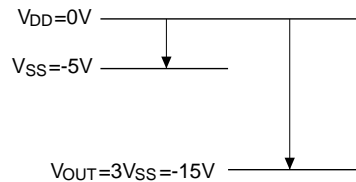
Voltage tripler

If capacitors C1 are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2–, and between V_{SS} and V_{OUT}, the potential between V_{DD} and V_{SS} is boosted to triple toward negative side and it is output at V_{OUT}. For double boosting, remove only capacitor C1 between CAP2+ and CAP2-, open CAP2+, and jumper between CAP2- and V_{OUT}. The double boosted voltage appears at V_{OUT} (CAP2-).

The booster receives signals from oscillator circuit and, therefore, the oscillator must be active. The following shows the boosted potential.

$(V_{CC}=+5V)\ V_{DD}=0V$

$(GND)\ V_{SS}=-5V$

$V_{OUT}=2V_{SS}=-10V$
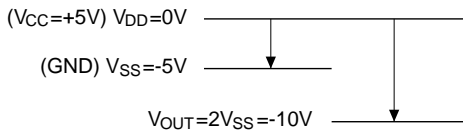
Potential during double boosting

$V_{DD}=0V$

$V_{SS}=-5V$

$V_{OUT}=3V_{SS}=-15V$

Potential during triple boosting

Voltage regulator

The boosting voltage occurring at V_{OUT} is sent to the voltage regulator and the V_5 liquid crystal display (LCD) drive voltage is output. This V_5 voltage can be determined by the following equation when resistors Ra and Rb (R1, R2 and R3) are adjusted within the range of $|V5|<|V_{OUT}|$.

$$V_5 = (1 + \frac{Rb}{Ra}) \cdot V_{REG} + I_{REF} \cdot Rb$$

$$= (1 + \frac{R3 + R2 - \Delta R2}{R1 + \Delta R2}) \cdot V_{REG}$$

$$+ I_{REF} \cdot (R3 + R2 - \Delta R2)$$
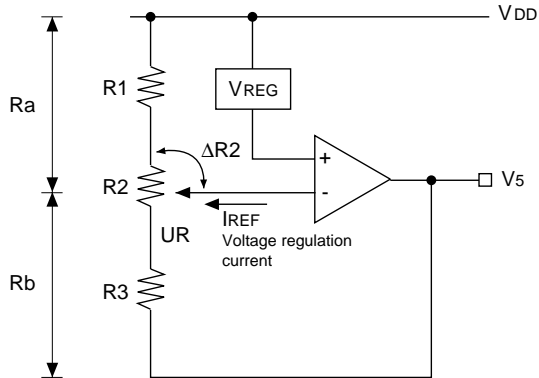
where, V_{REG} is the constant voltage source of the IC, and it is constant ($V_{REG} \doteqdot -3.1$ V). (V_{REG}=Type1) V_{REG}=V_{SS}(V_{DD} basis) (V_{REG}=Type2)
I_{REF} is the voltage regulation current of the Electronic Volume Control Function, and $I_{REF} \doteqdot 2.4$ μA if the electronic volume control register (32-state) has (D4,D3,D2,D1,D0)=(1,1,1,1,1).
To adjust the V_5 output voltage, insert a variable resistor between V_R, V_{DD} and V_5 as shown. A combination of R1 and R3 constant resistors and R2 variable resistor is recommended for fine-adjustment of V_5 voltage.

Setup example of resistors R1, R2 and R3:
When the Electronic Volume Control Function is OFF (electronic volume control register values are (D4,D3,D2,D1,D0) =(0,0,0,0,0)):

$$V_5 = (1 + \frac{R3 + R2 - \Delta R2}{R1 + \Delta R2}) \cdot V_{REG} \quad \text{.............} \quad ①$$

(As I_{REF} = 0A)
• R1 + R2 + R3 = 6.0 MΩ .... ②
(Determined by the current passing between V_{DD} and V5)
• Variable voltage range by R2: –6.2 to –9.3 V
(Determined by the LCD characteristics)
$\Delta R2$ = 0Ω, V_{REG} = –3.1 V
To obtain V_5 = –9.3 V, from equation (1):
R2 + R3 = 2 · R1 .... ③
$\Delta R2$ = R2, V_{REG} = –3.1 V
To obtain V_5 = –6.2 V, from equation (1):
R1 + R2 = 1 · R1 .... ④

From equations ②, ③ and ④: R1 = 2.0 MΩ
R2 = 1.0 MΩ
R3 = 3.0 MΩ

The voltage regulator circuit has a temperature gradient of approximately –0.17%/°C as the V_{REG} voltage. To obtain another temperature gradient, use the Electronic Volume Control Function for software processing using the MPU.
As the VR pin has a high input impedance, the shielded and short lines must be protected from a noise interference.
When the V_{REG} = Type 2, similarly preset R1, R2 and R3 on the basis of V_{REG} = V_{SS}.

Voltage regulator circuit using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of liquid crystal display (LCD) screen by command control of V_5 LCD driver voltage.
This function sets five-bit data in the electronic volume control register, and the V_5 LCD driver voltage can be one of 32-state voltages.

To use the Electronic Volume Control Function, issue the Set Power Control command to simultaneously operate both the voltage regulator circuit and voltage follower circuit.
Also, when the voltage tripler off, the voltage must be supplied from V_{OUT} terminal.

When the Electronic Volume Control Function is used, the V_5 voltage can be expressed as follows:

$$V_5 = (1 + \frac{Rb}{Ra}) \cdot V_{REG} + I_{REF} \cdot Rb \quad \text{.................} \quad ⑤$$

(Variable voltage range)

The increased V_5 voltage is controlled by use of I_{REF} current source of the IC. (For 32 voltage levels, ΔI_{REF}=I_{REF}/31)

The minimum setup voltage of the V_5 absolute value is determined by the ratio of external Ra and Rb, and the increased voltage by the Electronic Volume Control Function is determined by resistor Rb. Therefore, the resistors must be set as follows:
(1) Determine Rb resistor depending on the V_5 variable voltage range by use of the Electronic Volume Control.

$$Rb = \frac{V_5 \text{ variable voltage range}}{I_{REF}}$$

(2) To obtain the minimum voltage of the V_5 absolute value, determine Ra using the Rb of Step (1) above.

$$Ra = \frac{Rb}{\frac{V_5}{V_{REG}} - 1} \qquad [V_5 = (1 + Rb/Ra) \cdot V_{REG}]$$

The SED1526 series have the built-in V_{REG} reference voltage and I_{REF} current source which are constant during voltage variation. However, they may change due to the variation occurring in IC manufacturing and due to the temperature change as shown below. Consider such variation and temperature change, and set the Ra and Rb appropriate to the LCD used.
V_{REG} =–3.1V±0.4V (Type1) V_{REG} =–0.17%/°C
V_{REG} =V_{SS} (V_{DD} basis) (Type2) V_{REG} =–0.00%/°C
I_{REF} = –1.2 μA ± 40% (For 16 levels) I_{REF} = 0.011 μA/°C
I_{REF} = –2.4 μA ± 40% (For 32 levels) I_{REF} = 0.022 μA/°C
Ra is a variable resistor that is used to correct the V_5 voltage change due to V_{REG} and I_{REF} variation. Also, the contrast adjustment is recommended for each IC chip.
Before adjusting the LCD screen contrast, set the electronic volume control register values to (D4,D3,D2,D1,D0)=(1,0,0,0,0) or (0,1,1,1,1) first.
When not using the Electronic Volume Control Function, set the register values to (D4,D3,D2,D1,D0)=(0,0,0,0,0) by sending the $\overline{RES}$ signal or by issuing the Set Electronic Volume Control Register command.

Setup example of constants when Electronic Volume Control Function is used:

V_5 maximum voltage: $V_5 = -6.2$ V (Electronic volume control register values $(D4,D3,D2,D1,D0)=(0,0,0,0,0)$)

V_5 minimum voltages: $V_5 = -8.6$ V (Electronic volume control register values $(D4,D3,D2,D1,D0)=(1,1,1,1,1)$)

V_5 variable voltage range: 2.4 V

Variable voltage levels: 32 levels

(1) Determining the Rb:

$$Rb = \frac{V_5 \text{ variable voltage range}}{|I_{REF}|} = \frac{2.4 \text{ V}}{2.4 \text{ } \mu A} \qquad \underline{Rb = 1.0 \text{ M}\Omega}$$

(2) Determining the Ra:

$$Ra = \frac{Rb}{\frac{V_5 \text{ max}}{V_{REG}} - 1} = \frac{1.0 \text{ M}\Omega}{\frac{-6.2 \text{ V}}{-3.1 \text{ V}} - 1} \qquad \underline{Ra = 1.0 \text{ M}\Omega}$$

According to the V_5 voltage and temperature change, equation ⑤ can be as follows (if $V_{DD} = 0$ V reference):

If Ta = 25°C:

$$\begin{aligned} V_5 \text{ max} &= (1 + Rb/Ra) \cdot V_{REG} \\ &= (1 + 1 \text{ M}\Omega/1 \text{ M}\Omega) \times (-3.1 \text{ V}) \\ &= -6.2 \text{ V} \end{aligned}$$

$$\begin{aligned} V_5 \text{ min} &= V_5 \text{ max} + Rb \cdot I_{REF} \\ &= -6.2 \text{ V} + 1 \text{ M}\Omega \times (-2.4 \text{ } \mu A) \\ &= -8.6 \text{ V} \end{aligned}$$

If Ta = -10°C:

$$\begin{aligned} V_5 \text{ max} &= (1 + Rb/Ra) \cdot V_{REG} \\ &= (1 + 1 \text{ M}\Omega/1\text{M}\Omega) \times (-3.1 \text{ V}) \times \{1 + (-0.17\%/°C) \\ &\quad \times (-10°C - 25°C)\} \\ &= -6.57 \text{ V} \end{aligned}$$

$$\begin{aligned} V_5 \text{ min} &= V_5 \text{ max} + Rb \cdot I_{REF} \\ &= -6.57 \text{ V} + 1\text{M}\Omega \times \{-2.4 \text{ } \mu A + (0.022 \text{ } \mu A/°C) \times \\ &\quad (-10°C - 25°C)\} \\ &= -8.20 \text{ V} \end{aligned}$$

If Ta = 50°C:

$$\begin{aligned} V_5 \text{ max} &= (1 + Rb/Ra) \cdot V_{REG} \\ &= (1 + 1 \text{ M}\Omega/1 \text{ M}\Omega) \times (-3.1 \text{ V}) \times \{1 + (-0.17\%/°C) \\ &\quad \times (50°C - 25°C)\} \\ &= -5.94 \text{ V} \end{aligned}$$

$$\begin{aligned} V_5 \text{ min} &= V_5 \text{ max} + Rb \cdot I_{REF} \\ &= -5.94 \text{ V} + 1\text{M}\Omega \times \{-2.4 \text{ } \mu A + (0.022 \text{ } \mu A/°C) \times \\ &\quad (-50°C - 25°C)\} \\ &= -8.89 \text{ V} \end{aligned}$$

The margin must also be determined in the same procedure given above by considering the V_{REG} and I_{REF} variation. This margin calculation results show that the V_5 center value is affected by the V_{REG} and I_{REF} variation. The voltage setup width of the Electronic Volume Control depends on the I_{REF} variation. When the typical value of 0.2 V/step is set, for example, the maximum variation range of 0.12 to 0.28 V must be considered.

When the V_{REG} = Type 2, it so becomes that $V_{REG} = V_{SS}$ and there is no temperature gradient. However, I_{REF} carries the same temperature characteristics as with V_{REG} = Type 1.

Voltage generator for LCD (Voltage fullower)

The V_5 potential is divided using resistance within IC and V_1, V_2, V_3 and V_4 potentials are generated for LCD panel drive. These potentials are then converted in impedance by voltage follower, and sent to LCD driver circuit.

Because the LCD drive voltage has been fixed to each model, the display quality may drop in specific duty selected by Select Duty command. If it occurs, use an external power supply.

Model	LCD drive voltage
SED1526	1/5 of bias voltage
SED1528	1/7 of bias voltage

Subsection gives wiring examples and reference parts list when on-chip power supply is used and when not used.

Command sequence for built-in power circuit startup

The built-in power circuit must follow the command sequence given below.

• To start the built-in power circuit when logic units are being powered:

```
┌──────────────────┐
│  Hardware reset  │
│  (SR1=SR2='0')   │
└──────────────────┘
         │
         ▼
┌──────────────────┐
│  Setup of power  │
│     control      │
└──────────────────┘
         │  *After approx. 200 msec
         ▼
┌──────────────────┐
│ Display turns ON.│
└──────────────────┘
```
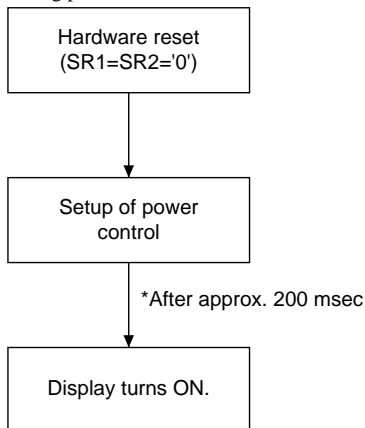
• To start the built-in power circuit after release of Power Save mode:

```
┌──────────────────────┐
│ Release the Power Save│
│ mode. (Static drive is│
│ OFF or display is ON.)│
└──────────────────────┘
         │
         ▼
┌──────────────────┐
│  Setup of power  │
│     control      │
└──────────────────┘
         │  *After approx. 200 msec
         ▼
┌──────────────────┐
│ Display turns ON.│
└──────────────────┘
```
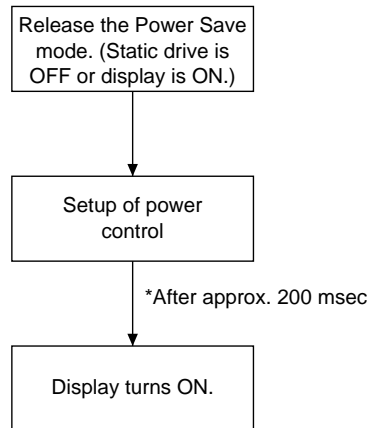
* When the Set Power Control command is issued, the V_{DD} level signal is output at both COM and SEG terminals for approximately 200 msec. Any other command can be entered during this period.

When turning off the built-in power circuit, observe the following command sequence to mainyain power save status.

When turning off the built-in
power supply:

Display "OFF"	Command AEh

↓

Static drive "ON"	Command A5h

Power save
command

↓

Built-in power supply "OFF"
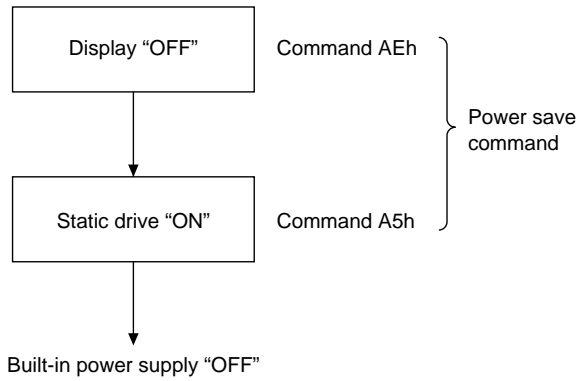
Reset Circuit

The SED1526 series chip parameters are initialized when both SR1 and SR2 are set to low.

○ **Initial parameter setup**

1. Display : Off
2. Duty cycle : 1/16 (SED1526)
3. ADC select : Normal (D0 ADC command is high and ADC status flag is set)
4. Read-modify-write : Off
5. Power Control register : 0
6. Initial Display Line register : Line 1
7. Column Address counter : Address 0
8. Page Address register : Page 0
9. Register data of serial interface : Cleared
10. Electronic control register : 0
11. Static drive : Off
12. Clock : Output

As explained in Section 4-32, the microprocessor should also be reset when SR1 and SR2 are reset. The SR1 and SR2 go low only when logical low pulses are entered at least 10 microseconds (refer to Section for AC characteristics). The normal reset signal appears 1 microsecond after the rising edge of this signal.

If the on-board LCD power circuit of the SED1526 series is not used, both SR1 and SR2 must be low when an external LCD power is supplied. If not low, the IC chip may be destroyed by surge current. When reset, each register is cleared but the present setup of oscillator circuit and output terminals (FR, CL, D0 to D7) is not cleared.

As the SED1526 series does not have a Power-On Clear circuit, both SR1 and SR2 must go low when logic power applies. If not, any recovery may fail.

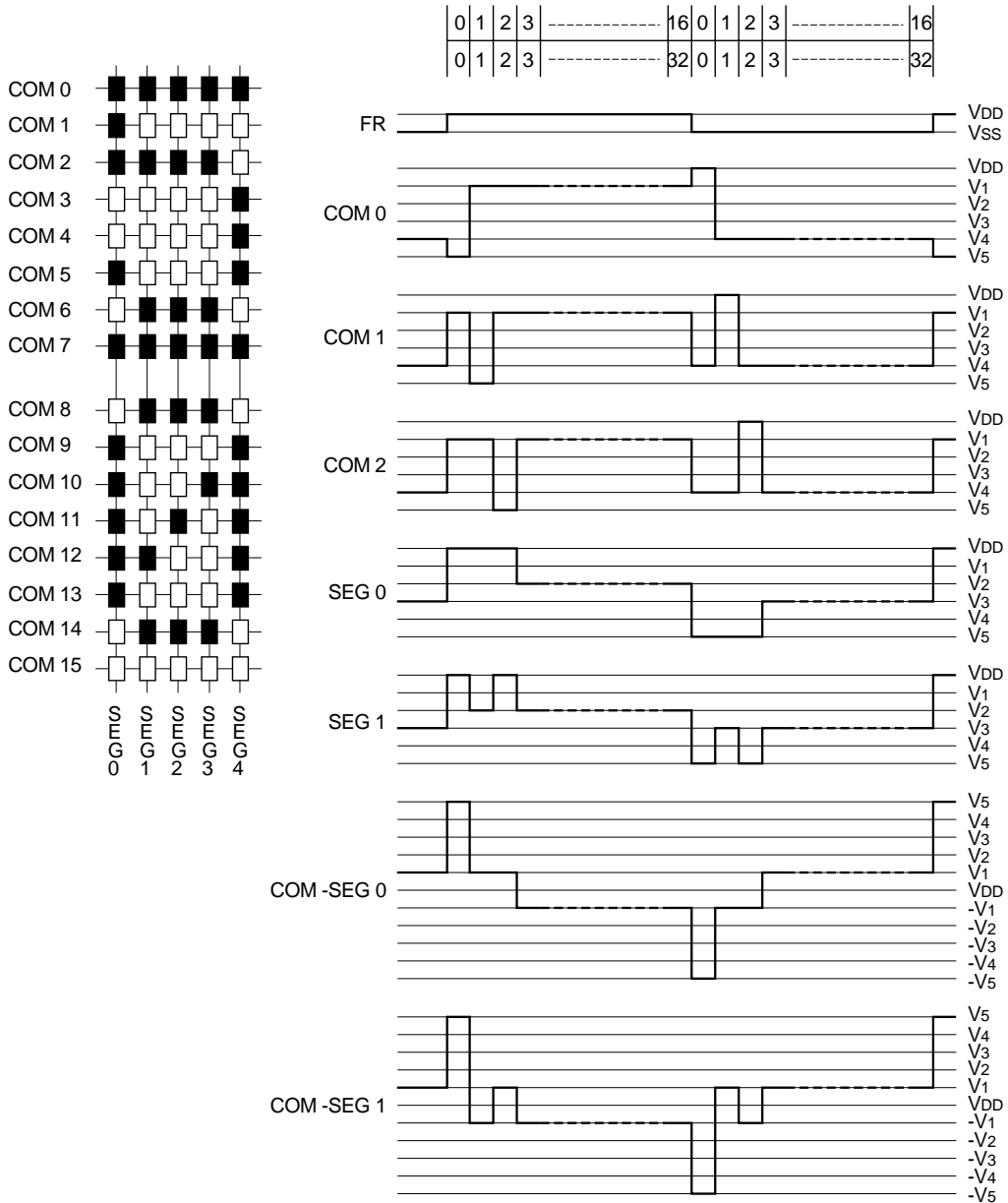The Reset command can reset parameters 6 to 10 listed above.

Figure 6

COMMANDS

Page 4–21 lists available commands. The SED1526 series uses a combination of A0, $\overline{RD}$ and $\overline{WR}$ (or R/$\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only (any external clock is required), its processing speed is very high and its busy check is usually not required.

• Command set

(1) Display ON/OFF

Alternatively turns the display on and off.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

The display turns off when D goes low, and it turns on when D goes high.

(2) Initial Display Line

Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	0	A4	A3	A2	A1	A0

$\leftarrow$ High-order bit

A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
:				:	:
1	1	1	1	0	3 0
1	1	1	1	1	3 1

(3) Set Page Address

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 4 is the display RAM area dedicate to the indicator, and only D0 is valid for data change.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	1	1	A2	A1	A0

A2	A1	A0	Page Address
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

(4) Set Column Address

Specifies column address of display RAM. When the microprocessor repeats to access to the display RAM, the column address counter is incremented by 1 during each access until address 80 is accessed. The page address is not changed during this time.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	0	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
1	0	0	1	1	1	1	7 9

(5) Read Status

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	PS	0	0	0

BUSY: When high, the SED1526 series is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is normal and column address "79-n" corresponds to segment driver n. When high, the display is reversed and column address n corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When goes low, the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by SR1 and SR2 to go low or by Reset command. When low, the display is on. When high, the chip is being reset.

PS: When low, LCD panel is in Power Save mode.

(6) Write Display Data

Writes 8-bit data in display RAM. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
1	1	0				Write data				

(7) Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
1	0	1				Read data				

(8) ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pins can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	$\overline{\text{RD}}$	R/$\overline{\text{W}}$ $\overline{\text{WR}}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction). When D is high, the left rotation (reverse direction).

(9) Static Drive ON/OFF

Forcibly turns the entire display ON and makes all common outputs selectable regardless of RAM data contents. The RAM data is held.

A0	$\overline{\text{RD}}$	R/$\overline{\text{W}}$ $\overline{\text{WR}}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D goes low, the static drive turns off. When D goes high, the static drive turns on.

The LCD panel enters Power Save mode if Static Drive ON command is issued when the display is off. Refer to the Power Save section for details.

(10) Select Duty

Selects the LCD driver duty. However, the bias of LCD driver voltage is fixed when on-chip power circuit is used (refer to Subsection).

A0	$\overline{\text{RD}}$	R/$\overline{\text{W}}$ $\overline{\text{WR}}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

Model	D	Duty
SED1526	0 1	1/8 1/16
SED1528	0 1	1/32 1/32

(11) Duty+1

Increments the duty by 1. If 1/8 duty is set for the SED1526, for example, it is incremented to 1/9 duty. If 1/16 duty is set, it is incremented to 1/17 duty. The COMS terminal functions as COM8 or COM16. The display line of RAM area corresponding to page address 4, or D0, is always accessed.

A0	$\overline{\text{RD}}$	R/$\overline{\text{W}}$ $\overline{\text{WR}}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	D

| Model	D	Duty
SED1526	0 1	1/8 or 1/16 1/9 or 1/17
SED1528	0 1	1/32 1/33

(12) Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremented by Read Display Data command but incremented by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	$\overline{\text{RD}}$	R/$\overline{\text{W}}$ $\overline{\text{WR}}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.
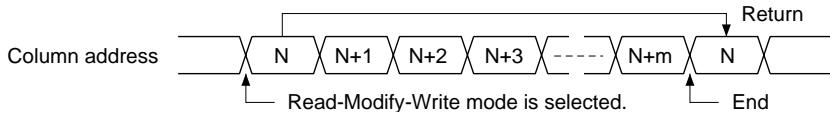
• Cursor display sequence
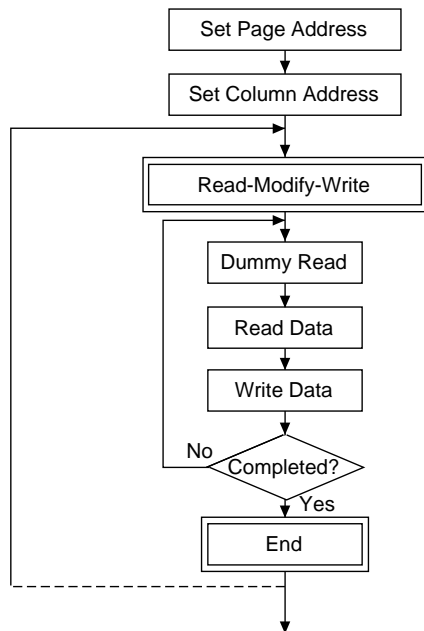
(13) End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write was issued).

A0	$\overline{RD}$	R/$\overline{W}$ WR	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Column address — N N+1 N+2 N+3 ---- N+m N — Return

Read-Modify-Write mode is selected.   End

(14) Reset

Resets the Initial Display Line register, Column Address counter, Page Address register, register data of serial interface, and Electronic Control register to their initial status. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of FUNCTIONAL DESCRIPTION.

A0	$\overline{RD}$	R/$\overline{W}$ WR	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply. Only RES (that sets SR1 and SR2 to low) can initialize the supplies.

(15) Set Power Control

Selects one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power supply functions can be used simultaneously. Refer to Power Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	$\overline{RD}$	R/$\overline{W}$ WR	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	1	0	D2	D1	D0

When D0 goes low, voltage follower turns off. When D0 goes high, it turns on.
When D1 goes low, voltage regulator turns off. When D1 goes high, it turns on.
When D2 goes low, voltage booster turns off. When D2 goes high, it turns on.

(16) Set Electronic Control

Adjusts the contrast of LCD panel display by changing V_5 LCD drive voltage that is output by voltage regulator of on-chip power supply.
This command selects one of 32 V_5 LCD drive voltages by storing data in 5-bit register. The V_5 voltage adjusting range should be determined depending on the external resistance. Refer to the Voltage Regulator Circuit section of FUNCTIONAL DESCRIPTION for details.
This command is valid only when voltage regulator circuit is turned on by Set Power Control command.

A0	$\overline{RD}$	R/$\overline{W}$ WR	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	0	D4	D3	D2	D1	D0

D4	D3	D2	D1	D0	$|V_5|$
0	0	0	0	0	Low
0	0	0	0	1	
0	0	0	1	0	
		↓			↓
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	High

Set register to (D4,D3,D2,D1,D0)=(0,0,0,0,0) to suppress electronic control function.

(17) Clock Stop

Stops clock output at CL to reduce current consumption.

A0	$\overline{RD}$	R/$\overline{W}$ WR	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	1	D

Clock outputs when D is low, but clock stops when D is high.

(18) Power Save (a combination with Static Drive command)

Sets LCD panel in power save mode if Static Drive ON is issued when the display is off. Power consumption drops power consumption level.
When LCD panel enters Power Save mode:
(a) Both oscillator and power supply stop.
(b) LCD driver stops, and segment and common driver have V_{DD} level output.
(c) External clock input is disabled, and clock output is set to low (at CL).
(d) Both display data and operation mode before issue of Power Save are held.
(As the power control register is cleared, the Set Power Control command must be issued again after the Power Save mode has been released.)
(e) All LCD driver voltages are fixed to V_{DD}.
The Power Save is released when the display is turned on or when Static Drive OFF is issued. If external voltage driver resistors are used to supply voltage to LCD panel, current passing through resistors must be cut off. An external power supply must be turned off if used; its voltage must be fixed to floating or V_{DD} level.
* When the SED1526 family is operating, the internal status data set by commands is held. However, the internal status may change due to an excessive ambient noise. The package and system noise generation must be suppressed or a noise protection design must be considered.
We recommend to periodically refresh the internal status data to prevent a spike noise and other interference.
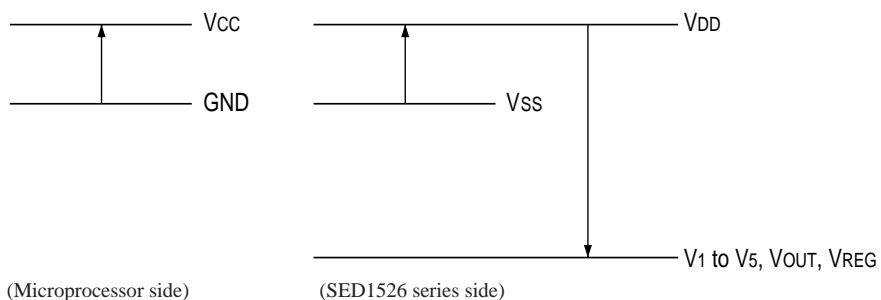
SED1526 Series Command Table

Command	Code										Function
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns on LCD panel when goes high, and turns off when goes low.
(2) Initial Display Line	0	1	0	1	1	0	Initial display address					Specifies RAM display line for COM0.
(3) Set Page Address	0	1	0	1	0	1	1	1	Page address			Sets the display RAM page in Page Address register.
(4) Set Column Address	0	1	0	0	Column address							Sets RAM column address in Column register.
(5) Read Status	0	0	1	Status				0	0	0		Reads the status information.
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM.
(7) Read Display Data	1	0	1	Read data								Reads data from display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Sets normal relationship between RAM column address and segment driver when low, but reverses the relationship when high.
(9) Static Drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Normal indication when low, but full indication when high.
(10) Duty Select	0	1	0	1	0	1	0	1	0	0	0 1	Selects LCD driver duty of 1/8 (1/16) when low and 1/16 (1/32) when high.
(11) Duty+1	0	1	0	1	0	1	0	1	0	1	0 1	Selects normal LCD driver duty when low, and selects the duty added by 1 when high.
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low.
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Power Control	0	1	0	1	0	1	1	0	Power control			Selects various power circuit functions.
(16) Set Electronic Control	0	1	0	1	0	0	Electronic control value					Sets V_5 output voltage to Electronic Control register.
(17) Clock Stop	0	1	0	1	1	1	0	0	1	1	0 1	Stops clock output at CL when low, and stops clock when high.
(18) Power Save	–	–	–	–	–	–	–	–	–	–	–	A combination of Display OFF and Static Drive ON commands.

Note: Do not use any other command, or the system malfunction may result.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply voltage range		V_{DD}	−0.3 to +7.0	V
	Triple voltage conversion	V_{DD}	−0.3 to +6.0	
Driver supply voltage range (1)		V5	−18.0 to +0.3	V
Driver supply voltage range (2)		V1, V2, V3, V4	V5 to +0.3	V
Input voltage range		V_{IN}	−0.3 to V_{DD}+0.3	V
Output voltage range		VO	−0.3 to V_{DD}+0.3	V
Allowable loss		P_D	250	mW
Operating temperature range		T_{OPR}	−40 to +85	°C
Storage temperature range	QFP • TCP	T_{STG}	−65 to +150	°C
	Bear chip		−55 to +125	
Soldering temperature and time		T_{SOLDER}	260-10 (at leads)	°C•sec

```
         ┌───────▲──── Vcc      ┌───────▲─────────── VDD
         │       │              │       │       │
         └───────┴──── GND      └───────┴── Vss   │
                                                  │
                                                  │
                                                  │
                                                  ▼
                                        ┌───────────── V1 to V5, VOUT, VREG
     (Microprocessor side)       (SED1526 series side)
```

Notes: 1. V_1 to V_5, V_{OUT}, and V_{REG} voltages are based on V_{DD}=0 V.
       2. Voltages $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{SS} \geq V_{OUT}$ must always be satisfied.
       3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.
       4. The moisture resistance of the flat package may drop during soldering. Take care not to excessively heat the package resin during chip mounting.

ELECTRICAL CHARACTERISTICS
DC Characteristics

V_{DD} = 5 V ±10%, V_{SS} = 0 V, Ta = −40 to +85°C unless otherwise noted.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)	Operational	V_{DD}		2.4		6.0	V	V_{DD} *1
Operating voltage	Operational	V_5		−13.0		−4.0	V	V_5 *2
(2)	Operational	V_1, V_2		$0.6 \times V_5$		V_{DD}	V	V_1, V_2
	Operational	V_3, V_4		V_5		$0.4 \times V_5$	V	V_3, V_4
CMOS	High-level input voltage	V_{IHC}		$0.7 \times V_{DD}$		V_{DD}	V	*3
			V_{DD} = 2.7 V	$0.8 \times V_{DD}$		V_{DD}		
	Low-level input voltage	V_{ILC}		V_{SS}		$0.3 \times V_{DD}$	V	*3
			V_{DD} = 2.7 V	V_{SS}		$0.2 \times V_{DD}$		
	High-level output voltage	V_{OHC}	I_{OH} = −1 mA	$0.8 \times V_{DD}$		V_{DD}	V	*4
			V_{DD} = 2.7 V, I_{OH} = −0.5 mA	$0.8 \times V_{DD}$		V_{DD}		
	Low-level output voltage	V_{OLC}	I_{OH} = 1 mA	V_{SS}		$0.2 \times V_{DD}$	V	*4
			V_{DD} = 2.7 V, I_{OL} = 0.5 mA	V_{SS}		$0.2 \times V_{DD}$		
Schmitt	High-level input voltage	V_{IHS}		$0.4 \times V_{DD}$		$0.8 \times V_{DD}$	V	*5
			V_{DD} = 2.7 V	$0.4 \times V_{DD}$		$0.8 \times V_{DD}$		
	Low-level input voltage	V_{ILS}		$0.2 \times V_{DD}$		$0.6 \times V_{DD}$	V	*5
			V_{DD} = 2.7 V	$0.2 \times V_{DD}$		$0.6 \times V_{DD}$		
Input leakage current		I_{LI}		−1.0		1.0	μA	*6
Output leakage current		I_{LO}		−3.0		3.0	μA	*7
LCD driver ON resistance		R_{ON}	Ta = 25°C V_5 = −0.5 V		15.0	30.0	KΩ	SEG0 to 79 COS0 to 15 COMS *9
Static current consumption		I_{DDQ}	$\overline{CS}$ = C_L = V_{DD}		0.05	3.0	μA	V_{DD}
Input pin capacity		C_{IN}	Ta = 25°C, f = 1 MHz		5.0	8.0	pF	Input pins
CL output frequency		f_{CL}	Ta = 25°C, V_{DD} = 2.7 to 5 V	2.4	2.9	3.7	kHz	*8
				4.8	5.8	7.4		Applies to the SED1526*B*, SED1528*B*

Dynamic current consumption (1) when the built-in power supply is OFF
1.7 times of normal products apply to f_{CL} = 5.8 kHz products of SED1526FB* and SED1528FB*.   Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SED1526	I_{DD} (1)	V_{DD} = 5.0V, V_5–V_{DD} = −6.0V	–	9.1	18	μA	*12
		V_{DD} = 3.0V, V_5–V_{DD} = −6.0V	–	12.0	24		
SED1528		V_{DD} = 5.0V, V_5–V_{DD} = −8.0V	–	7.5	15		
		V_{DD} = 3.0V, V_5–V_{DD} = −8.0V	–	9.5	19		

Dynamic current consumption (2) when the built-in power supply is ON (Display all white)

1.7 times of normal products apply to f_{CL} = 5.8 kHz products of SED1526FB* and SED1528FB*.   Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SED1526	I_{DD} (2)	V_{DD} = 5.0V, V_5–V_{DD} = −6.0V, dual boosting	–	31	62	μA	*13
		V_{DD} = 3.0V, V_5–V_{DD} = −6.0V, triple boosting	–	44	88		
SED1528		V_{DD} = 5.0V, V_5–V_{DD} = −8.0V, dual boosting	–	37	74		
		V_{DD} = 3.0V, V_5–V_{DD} = −8.0V, triple boosting	–	55	110		

Dynamic current consumption (2) when the built-in power supply is ON (Display checker pattern)

1.7 times of normal products apply to f_{CL} = 5.8 kHz products of SED1526FB* and SED1528FB*.   Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SED1526	I_{DD} (2)	V_{DD} = 5.0V, V_5–V_{DD} = −6.0V, dual boosting	–	34	68	μA	*13
		V_{DD} = 3.0V, V_5–V_{DD} = −6.0V, triple boosting	–	46	92		
SED1528		V_{DD} = 5.0V, V_5–V_{DD} = −8.0V, dual boosting	–	42	84		
		V_{DD} = 3.0V, V_5–V_{DD} = −8.0V, triple boosting	–	60	120		

Current consumption during Power Save mode V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V   Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power save mode	I_{DDS1}	SED1526, SED1528	—	3	6	μA	—

Typical current consumption characteristics (reference data)

• Dynamic current consumption (1) when LCD external power mode lamp is ON
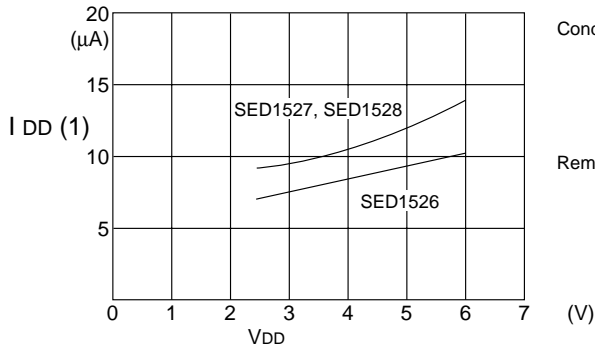
Conditions: The built-in power supply is OFF and an external power supply is used.
SED1526 V_5-V_{DD}=−6.0V
SED1528 V_5-V_{DD}=−8.0V
Ta=25°C

Remarks: *12
1.7 times of normal products apply to f_{CL} = 5.8 kHz products of SED1526FB* and SED1528FB*.

• Dynamic current consumption (2) when the LCD built-in power supply lamp is ON
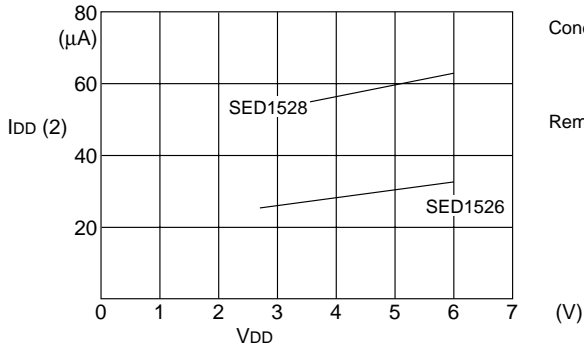
Conditions: The built-in power supply is ON.
SED1526 V_5-V_{DD}=−6.0V dual boosting
SED1528 V_5-V_{DD}=−8.0V triple boosting
Ta=25°C

Remarks: *13
1.7 times of normal products apply to f_{CL} = 5.8 kHz products of SED1526FB* and SED1528FB*.

- Current consumption I $_{DD}$ during access (2) during MPU access cycle

10
(mA)

SED1526

1

I$_{DD}$(2)

0.1

SED1528

0.01

0   0.01   0.1   1   10

f $_{CYC}$ (MHz)
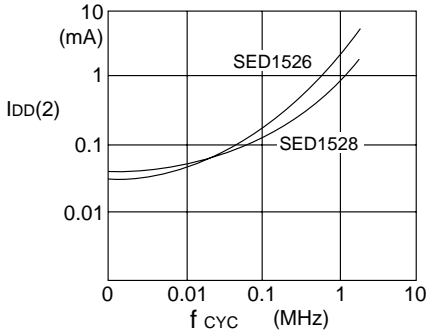
It shows the current consumption when a checker pattern is always written in f$_{SYNC}$ timing. When not accessed, only the current consumption of I$_{DD}$ (2) occurs.

Conditions: SED1526 V$_5$ – V$_{DD}$ = –6.0 V, dual boosting
SED1528 V$_5$ – V$_{DD}$ = –8.0 V, triple boosting
Ta = 25°C

	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Pins used
Built-in power circuit	Input voltage	V$_{DD}$	—	2.4	—	6.0	V	*10
	Booster output voltage	V$_{OUT}$	V$_{DD}$ reference (during triple boosting)	–16.5	—	—	V	V$_{OUT}$
	Voltage regulator circuit operating voltage	V$_{OUT}$	V$_{DD}$ reference	–16.5	—	–4.0	V	V$_{OUT}$
	Voltage follower operating voltage	V$_5$	V$_{DD}$ reference	–13.0	—	–4.0	V	*11
	Reference voltage	V$_{REG}$	V$_{DD}$ reference Ta = 25°C	–3.5	–3.1	–2.7	V	V$_R$

* See notes below.

*1   Although the wide range of operating voltage is guaranteed, a spike voltage change during access to the MPU is not guaranteed.
*2   The operating voltage range of the V$_{DD}$ and V$_5$ systems (See Figure 9.)
The operating voltage range is applied if an external power supply is used.
*3   Pins D0 to D5, A0, CS1, CS2, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), M/S, CL, and FR
*4   Pins D0 to D7, FR, and CL
*5   Pins SI (D7), SCL (D6), SR1, and SR2
*6   Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), CS1, CS2, M/S, SR1, and SR2
*7   Applied if pins D0 to D7, FR, and CL are high impedance.
*8   For the relationship between CL output frequency and frames, see Figure 7.
For the relationship between CL output frequency and power voltage, see Figure 8.
For the relationship between CL output frequency and temperature, see Figure 11.
*9   The resistance when the 0.1-volt voltage is applied between the SEG and COM output terminals and each power terminal (V$_1$, V$_2$, V$_3$ or V$_4$). It must be within operating voltage (2).
RON = 0.1 V/ΔI
where, ΔI is the current that flows between power supply and SEG or COM terminal when the 0.1-volt voltage is applied.
*10 If the triple voltage by the built-in power circuit are used the V$_{DD}$ primary power must be used within the input voltage range.
*11 The V$_5$ voltage can be adjusted within the voltage follower operating range by use of voltage regulator.
*12 Applied if the built-in oscillation circuit is used and if not accessed by the MPU.
*13 Applied if the built-in oscillation circuit and the built-in power circuit are used, and if not accessed by the MPU.
The current flowing through the voltage regulator resistors (R1, R2 and R3) is not included.
When the built-in voltage booster is used, the current consumption for the V$_{DD}$ power supply is shown.

- Relationship between CL output frequency and frames (SED 1526 series)

The relationship between CL output frequency (f$_{CL}$) and frame frequency (f$_F$) can be determined as follows:

	Duty	f$_F$
SED1526	1/9 1/17	8 • F$_{OSC}$/288 8•f$_{OSC}$/272
SED1528	1/33	8•f$_{OSC}$/264

Figure 7

("f$_F$" indicates the LCD current alternating cycle, but not the cycle of f$_F$ signals.)

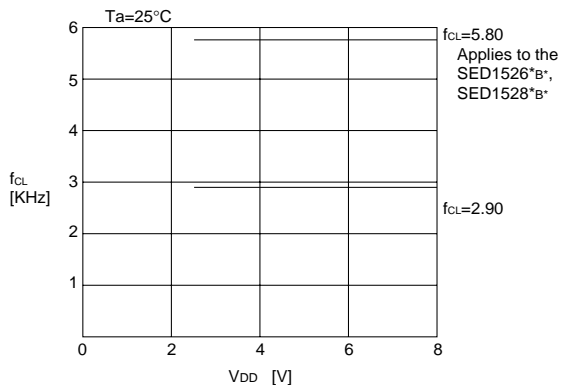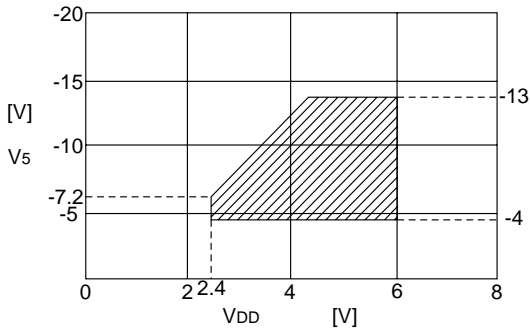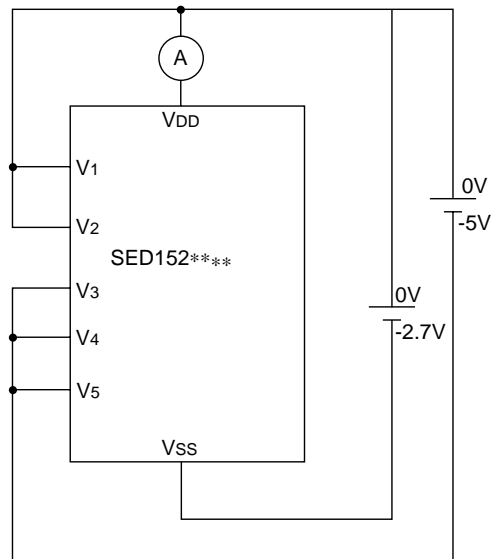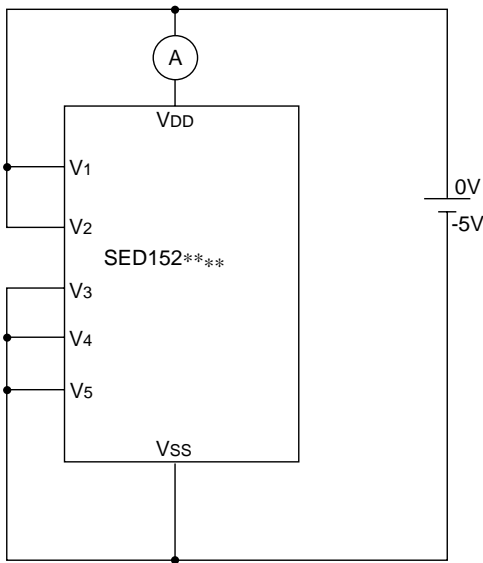- Relationship between CL output frequency and power voltage

Ta=25°C

6

5

4

f$_{CL}$
[KHz]   3

2

1

0   2   4   6   8

V$_{DD}$ [V]

f$_{CL}$=5.80
Applies to the SED1526*B*, SED1528*B*

f$_{CL}$=2.90

Figure 8
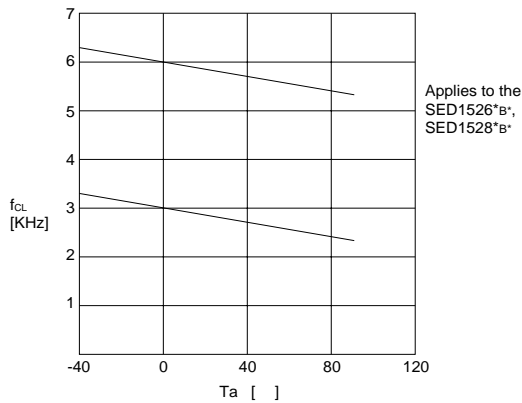
• Operating voltage range on V_{DD} and V_5

• I_{DD} measuring circuits
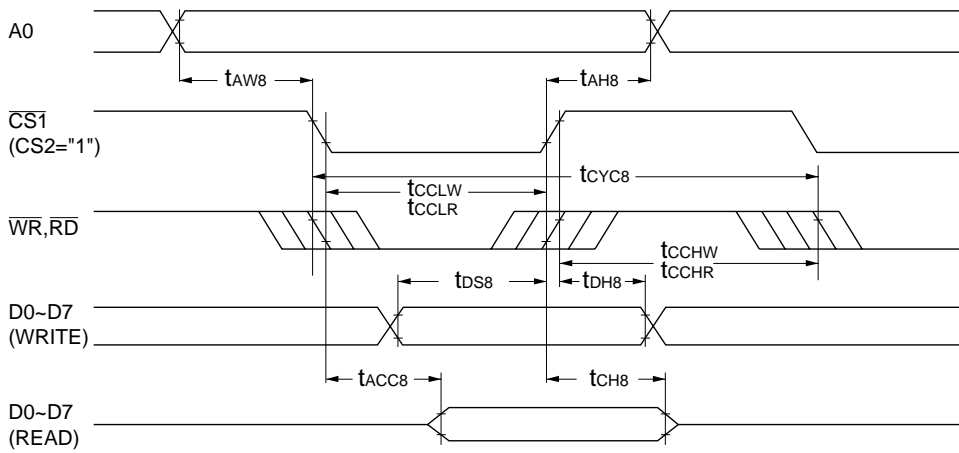

• Relationship between CL output frequency and temperature

AC Characteristics

(1) System buses
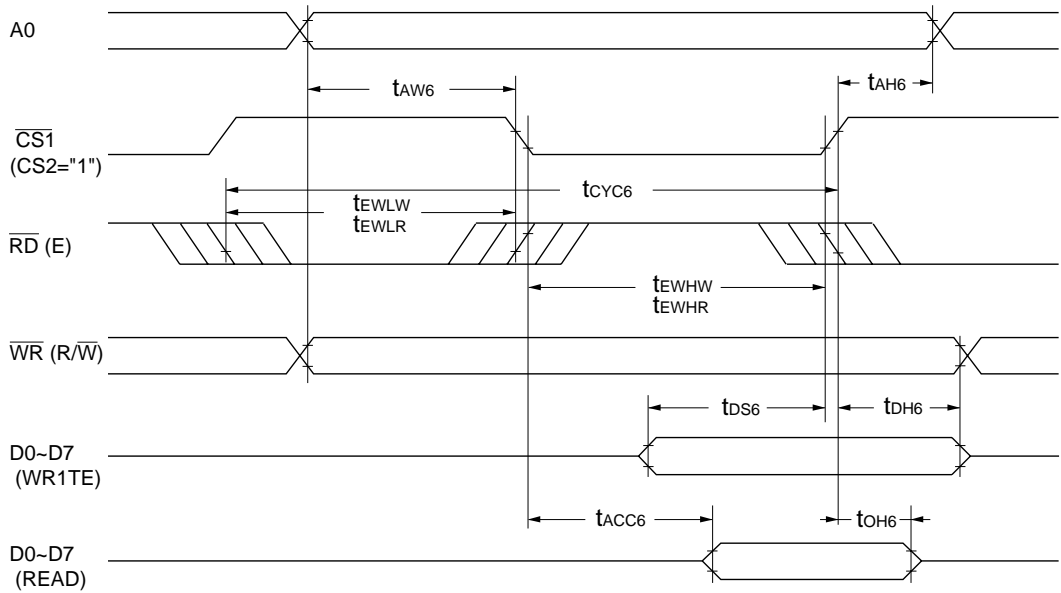
Read/write characteristics I (8080-series microprocessor)

$V_{SS} = 0$ V, $V_{DD} = 5.0$ V $\pm10\%$, Ta = -40 to $+85°$C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address setup time	A0	t_{AH8} t_{AW8}		5 5		ns ns
System cycle time		t_{CYC8}		400		ns
Control L pulse width (WR) Control L pulse width (RD) Control H pulse width (WR) Control H pulse width (RD)	$\overline{WR}$ $\overline{RD}$ $\overline{WR}$ $\overline{RD}$	t_{CCLW} t_{CCLR} t_{CCHW} t_{CCHR}		100 75 145 145		
Data setup time Data hold time		t_{DS8} t_{DH8}		80 10		ns ns
$\overline{RD}$ access time Output disable time	D0 to D7	t_{ACC8} t_{CH8}	CL=100pF	 10	80 60	ns ns

$V_{SS} = 0$ V, $V_{DD} = 2.7$ V to 4.5 V, Ta = -40 to $+85°$C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address setup time	A0	t_{AH8} t_{AW8}		10 10		ns ns
System cycle time		t_{CYC8}		800		ns
Control L pulse width (WR) Control L pulse width (RD) Control H pulse width (WR) Control H pulse width (RD)	$\overline{WR}$ $\overline{RD}$ $\overline{WR}$ $\overline{RD}$	t_{CCLW} t_{CCLR} t_{CCHW} t_{CCHR}		185 185 285 285		 ns ns
Data setup time Data hold time		t_{DS8} t_{DH8}		160 20		ns ns
$\overline{RD}$ access time Output disable time	D0 to D7	t_{ACC8} t_{CH8}	CL=100pF	 20	180 120	ns ns

Notes: 1. t_{CCLW} and t_{CCLR} are limited depending on the overlap time of $\overline{CS1}$ low (CS2 high) and $\overline{WR}$ or $\overline{RD}$ low.
2. The input signal rise and fall times must be within 15 nanoseconds.
3. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(2) System buses

Read/write characteristics II (6800-series microprocessor)

V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, Ta = −40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		400		ns
Address setup time Address hold time		$\overline{WR}$ (R/$\overline{W}$) A0	t_{AW6} t_{AH6}		20 10		ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		80 10		ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL=100pF	10	60 90	ns ns
Enable	READ	$\overline{RD}$ (E)	t_{EWLR}		85		ns
low pulse width	WRITE		t_{EWLW}		75		ns
Enable	READ	$\overline{RD}$ (E)	t_{EWHR}		135		ns
high pulse width	WRITE		t_{EWHW}		145		ns

V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = −40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		800		ns
Address setup time Address hold time		$\overline{WR}$ (R/$\overline{W}$) A0	t_{AW6} t_{AH6}		40 20		ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		160 20		ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL=100pF	20	120 180	ns ns
Enable	READ	$\overline{RD}$ (E)	t_{EWLR}		185		ns
low pulse width	WRITE		t_{EWLW}		145		ns
Enable	READ	$\overline{RD}$ (E)	t_{EWHR}		285		ns
high pulse width	WRITE		t_{EWHW}		325		ns

Notes: 1. t_{EWHR} and t_{EWHW} are limited depending on the overlap time of $\overline{CS1}$ low (CS2 high) and $\overline{RD}$ (E) high.
2. The input signal rise and fall times must be within 15 nanoseconds.
3. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(3) Serial interface

V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, Ta = −40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle Serial clock H pulse width Serial clock L pulse width	Serial clock	t_{SCYC} t_{SHW} t_{SLW}		500 150 150		ns ns ns
Address setup time Address hold time	A0	t_{SAS} t_{SAH}		120 200		ns ns
Data setup time Data hold time	Serial data	t_{SDS} t_{SDH}		120 120		ns ns
$\overline{CS}$ serial clock time	$\overline{CS1}$ (CS2="1")	t_{CSS} t_{CSH}		80 400		ns ns

V_{SS} = 0 V, V_{DD} = 2.7 to 4.5V, Ta = −40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle Serial clock H pulse width Serial clock L pulse width	Serial clock	t_{SCYC} t_{SHW} t_{SLW}		1000 300 300		ns ns ns
Address setup time Address hold time	A0	t_{SAS} t_{SAH}		250 400		ns ns
Data setup time Data hold time	Serial data	t_{SDS} t_{SDH}		250 250		ns ns
$\overline{CS}$ serial clock time	$\overline{CS1}$ (CS2="1")	t_{CSS} t_{CSH}		160 800		ns ns

Notes: 1. The input signal rise and fall times must be within 15 nanoseconds.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(4) Display control timing
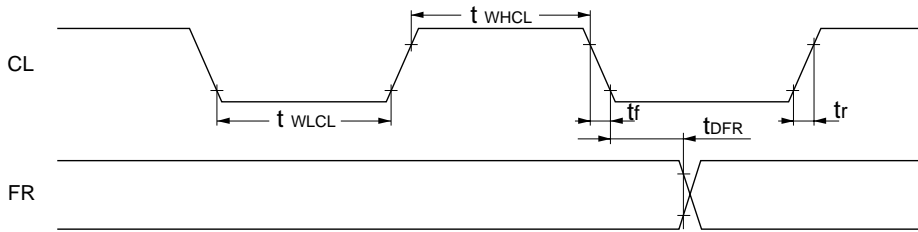
<div align="right">$V_{SS} = 0$ V, $V_{DD} = 5.0$ V $\pm 10\%$, Ta = -40 to $+85°$C</div>

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level pulse width	CL	t_{WLCL}		35			μs
High level pulse width		t_{WHCL}		35			μs
Rise time		tr			30	120	ns
Fall time		tf			30	120	ns
FR delay time	FR	t_{DFR}		−1.0	0.2	1.0	μs

<div align="right">$V_{SS} = 0$ V, $V_{DD} = 2.7$ V to 4.5 V, Ta = -40 to $+85°$C</div>

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level pulse width	CL	t_{WLCL}		70			μs
High level pulse width		t_{WHCL}		70			μs
Rise time		tr			60	240	ns
Fall time		tf			60	240	ns
FR delay time	FR	t_{DFR}		−2.0	0.4	2.0	μs

Output timing
<div align="right">$V_{SS} = 0$ V, $V_{DD} = 5.0$ V $\pm 10\%$, Ta = -40 to $+85°$C</div>

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	CL=100pF		0.2	0.4	μs

<div align="right">$V_{SS} = 0$ V, $V_{DD} = 2.7$ V to 4.5 V, Ta = -40 to $+85°$C</div>

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	CL=100pF		0.4	0.8	μs

Notes: 1. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(5) Reset timing
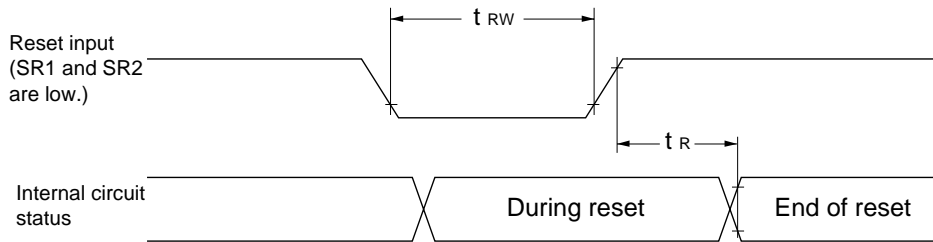
V_{DD} = 5.0 V ±10%, Ta = −40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		1.0			μs
Reset low pulse width	Reset input	t_{RW}		10			μs

V_{DD} = 2.7 V ±10%, Ta = −40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		3.0			μs
Reset low pulse width	Reset input	t_{RW}		30			μs

Notes: 1. t_R (reset time) represents the period from rising edge of reset input to end of internal circuit reset. The SED1526 series can operate normally after t_R.
2. t_{RW} specifies the minimum pulse width of reset input. The low pulse exceeding t_{RW} is required for reset.
3. The input signal rise and fall times must be within 15 nanoseconds.
4. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

EXTERNAL WIRINGS
Power Supply and LCD Power Circuit
If a single SED1526 series chip is used and if on-board power supply is used and not used

If on-chip power supply is used
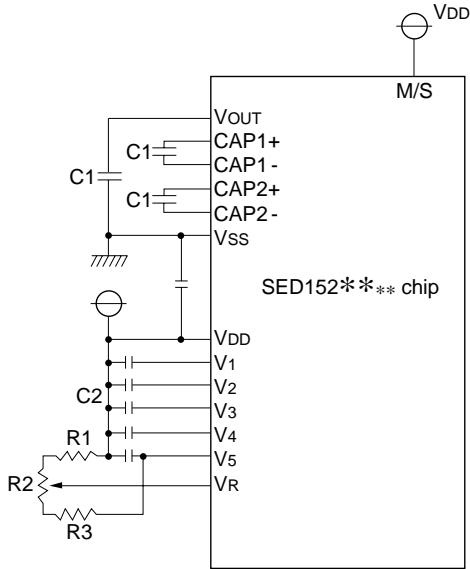
If on-chip power supply is NOT used
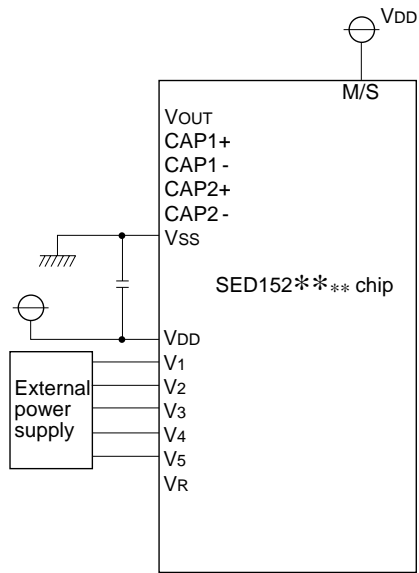
Parts list (Reference)

Variable $V_5 \fallingdotseq$ –9.3 to –6.2 V

C 1	0.1 to 1 µF
C 2	0.1 to 1 µF
R 1	2.0 MΩ
R 1	1.0 MΩ
R 1	3.0 MΩ

Note: Use jumper and shielded wires as the input impedance of VR terminal is high.

Setting value for your reference: 100 kΩ to 1 MΩ.

In order to select an optimum value for resistor R4, you should reference the LCD and the drive waveform.

Notes: 1. Because of high input impedance on V_R terminal, wiring should made as short as possible and shielded wire should be used for the wiring.
2. C1 and C2 depend on size of the liquid crystal panel to be driven. The value to be selected for C1 and C2 must be able to stabilize the liquid crystal drive voltage.
[A setting example]
Turn on the voltage regulator circuit and the voltage follower circuit to apply voltage to V_{OUT} externally. Display the LCD heavy load patterns (horizontal stripe-shaped), then select the C2 value that can stabilize the liquid crystal drive voltages (V_1 to V_5). All C2 capacity values selected, however, must be the same. Then, turn on every built-in power supplies and select an appropriate C1 value.
3. In order to regulate the voltage, a capacitor must be connected between V_{DD} and V_{SS} (near to the IC).

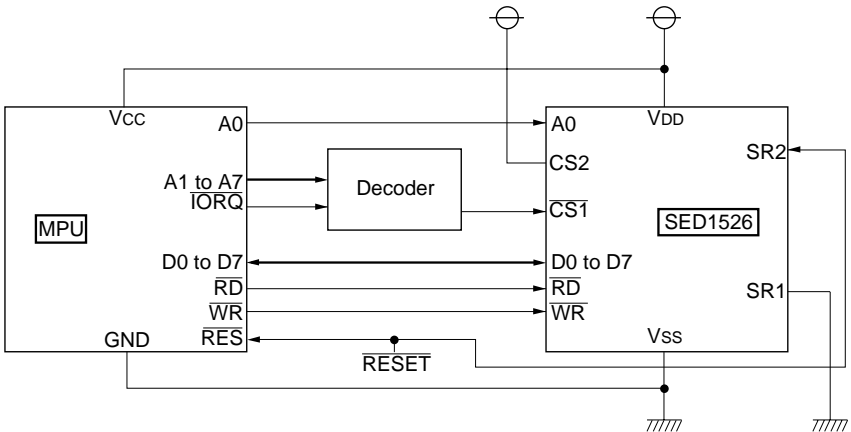**EPSON**
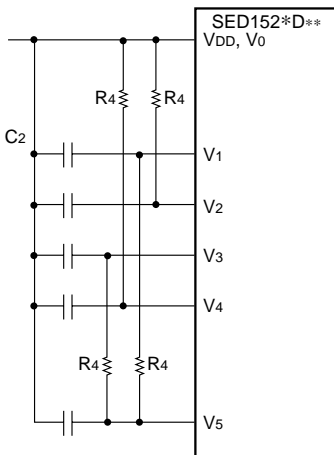
Microprocessor Interface

The SED1526 series chips can directly connect to 8080 and 6800-series microprocessors. Also, serial interfacing requires less signal lines between them.

8080-series microprocessors
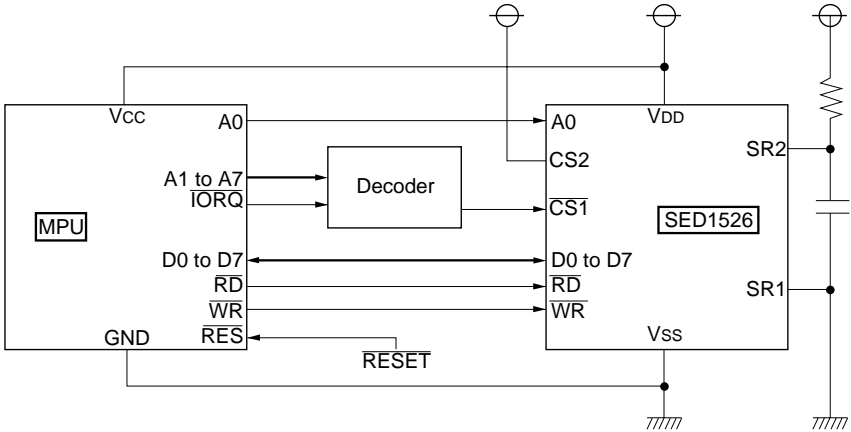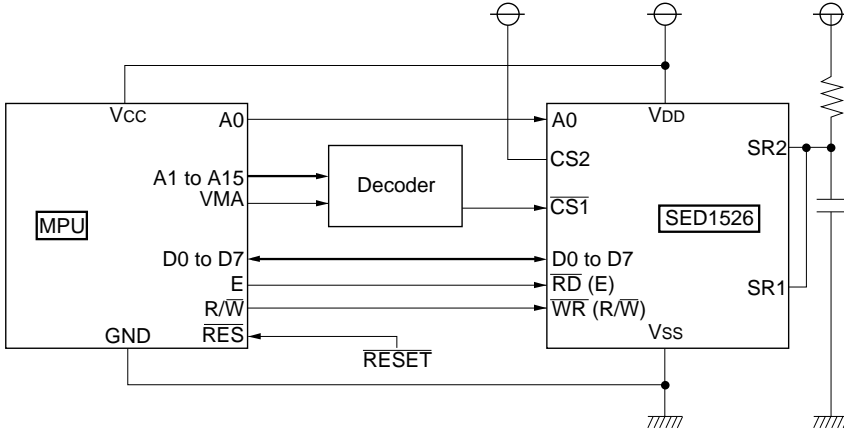
Wiring example 1:
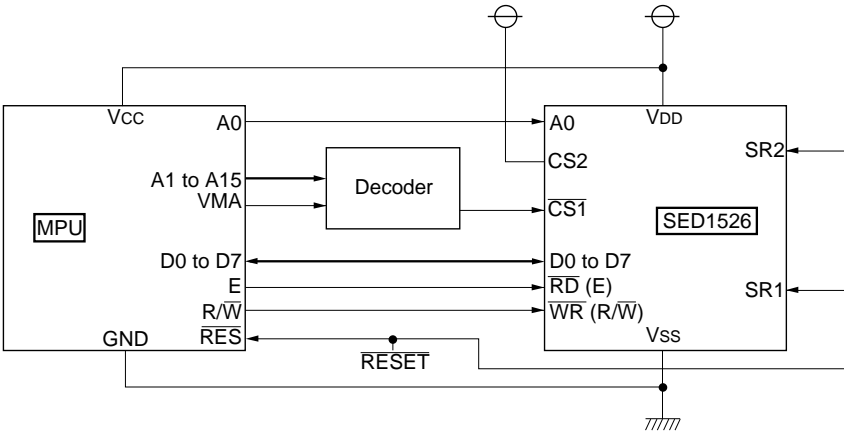

Wiring example 2:
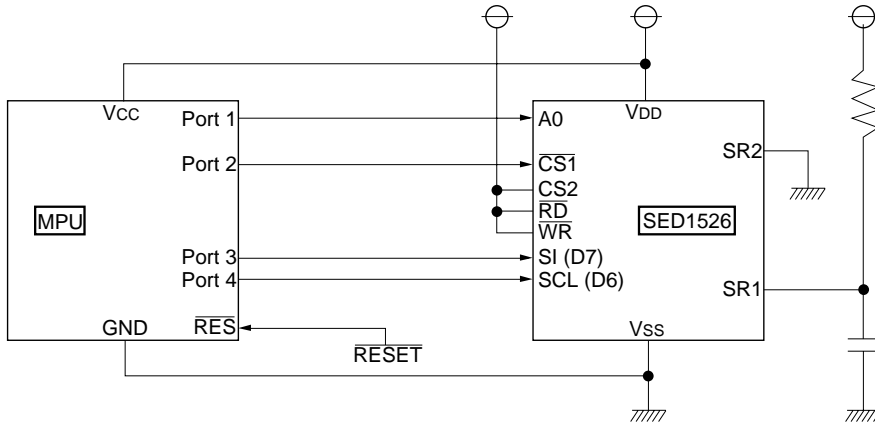
6800-series microprocessors

Wiring example 1:

Wiring example 2:

Serial interface

Wiring example 1:
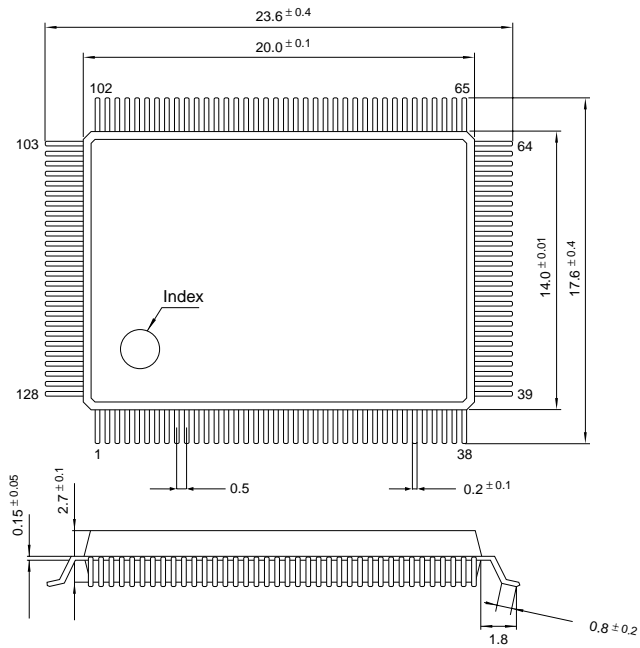

Wiring example 2:
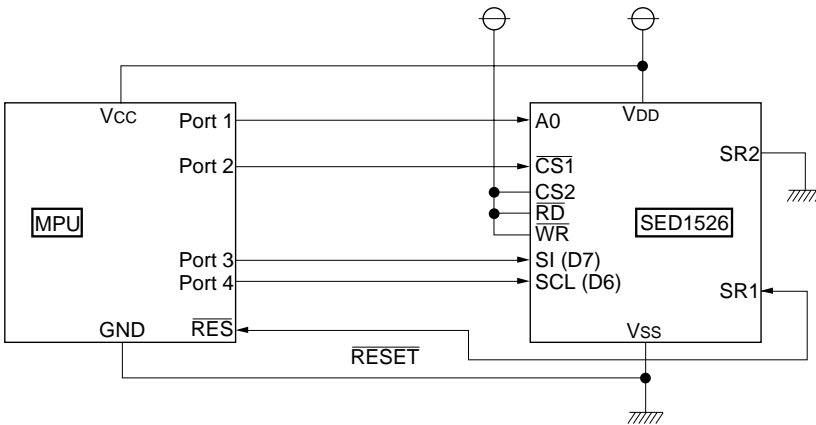
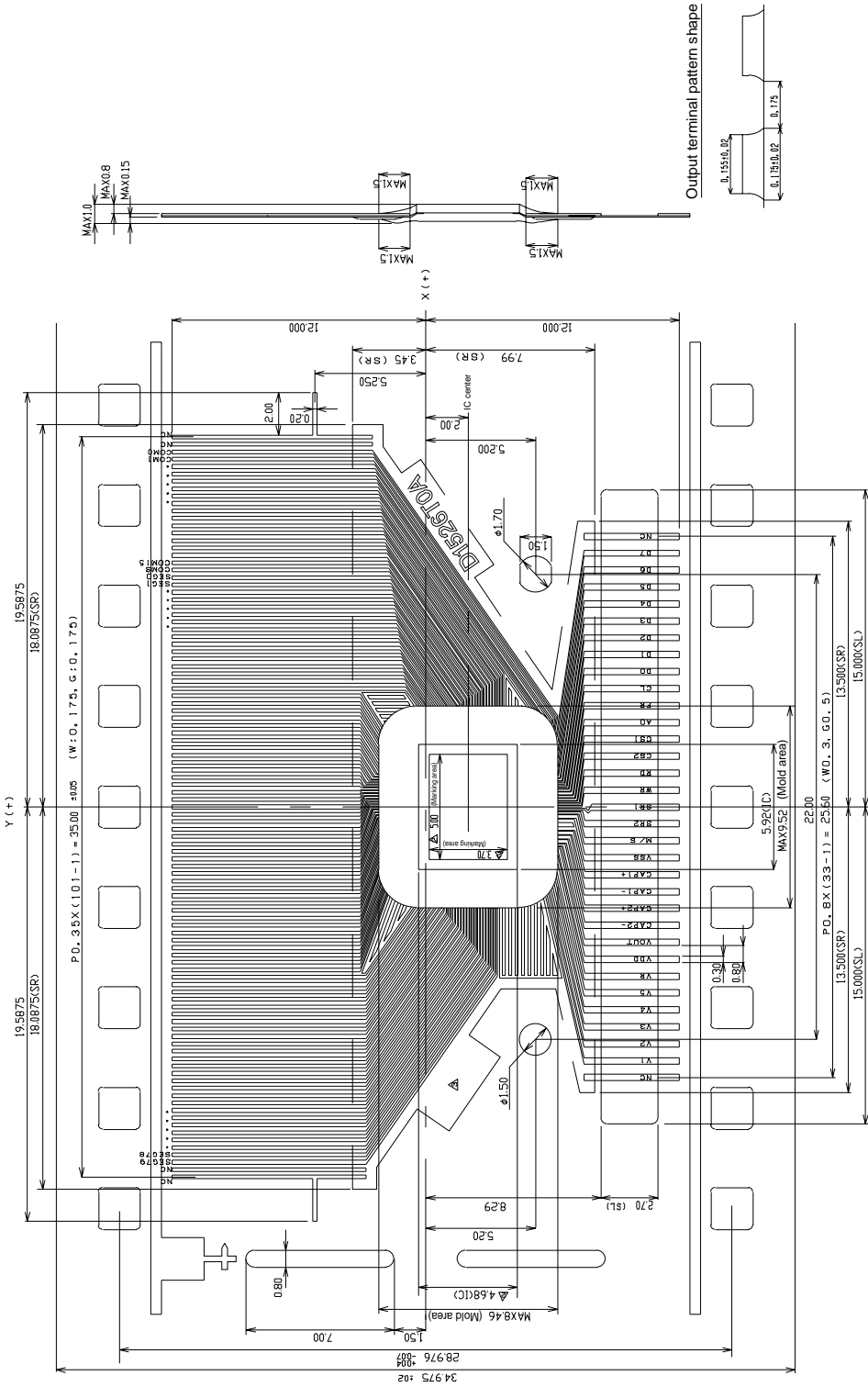## LCD Panel and Wiring Examples

Single-chip configuration

EPSON
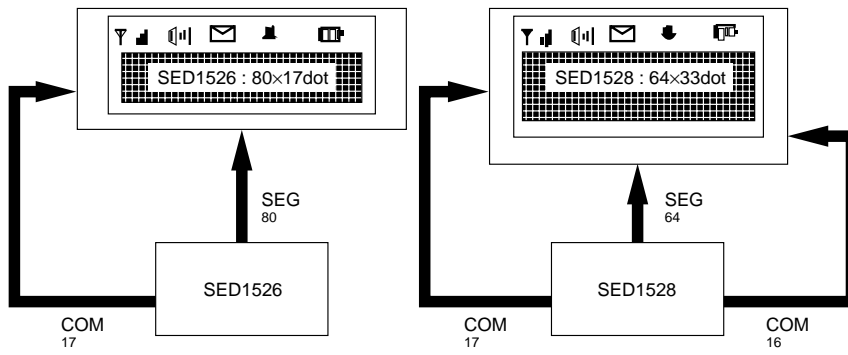
DIMENSIONS
Plastic 128-Pin QFP5 Package

The package dimensions are subject to change without notice.

TPC shape SED1526T0A (Reference drawing)

This dimensional outline drawing is subject to change for improvements without prior notice