CMOS DOT MATRIX HIGH DUTY LCD DRIVER

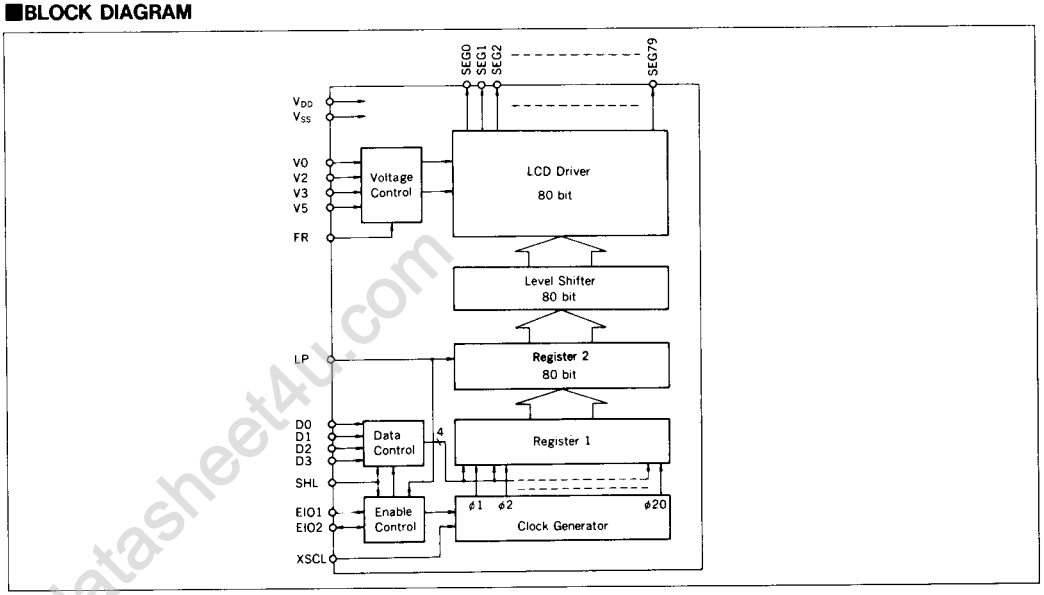
■DESCRIPTION

The SED1600F is an 80 output segment (column) driver, used to driver large-capacity dot matrix LCD panels with a duty ratio of 1/300 (from 1/100). It is used in conjunction with the SED1610F or SED1630F common (row) drivers. The SED1600F has a wide range of drive voltages. The maximum voltage V0 is isolated from V_{DD} to enable the application of any external LCD driving bias voltage from outside to the SED1600F. These unique features enable the SED1600F to operate with a wide variety of LCD panels. The SED1600F requires no enable signal to implement an enable chain technology which provides low power dissipation. This offers simpler interface with the LCD controller SED1330F/SED1341F or a microprocessor.

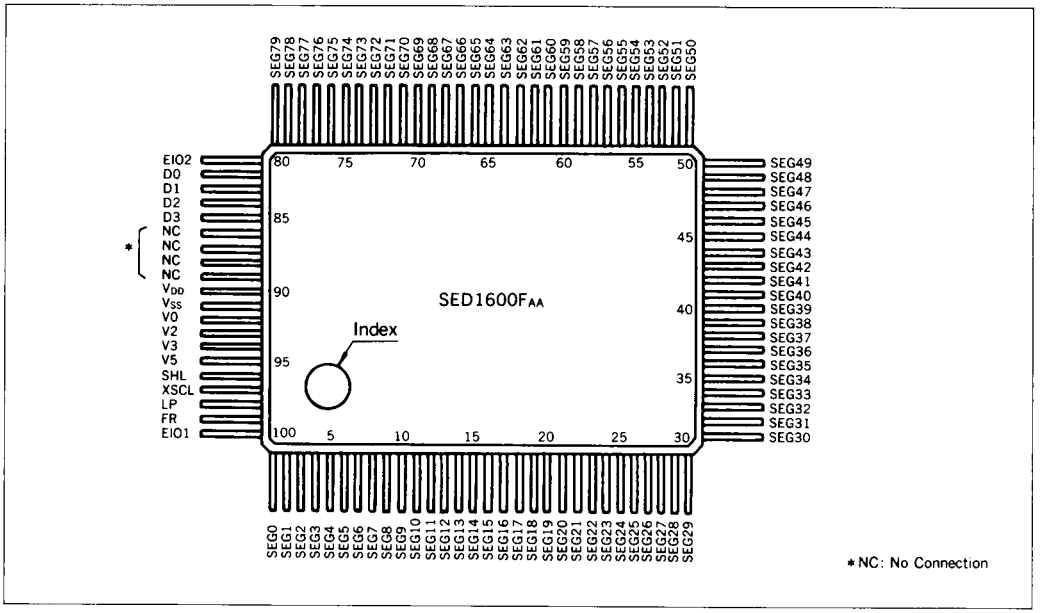
■FEATURES

- ●80 LCD driving outputs
- ●Display capacity ·····640×200×3 dots when combined with SED1610F (SED1630F)
- ●Wide range of LCD driving voltages ·····12 to 28V
  (Absolute maximum voltage·····30V)
- ●High-speed, low-power data transfer by 4-bit bus enable chain technology
  Shift clock·····6MHz Max
- ●Enable auto-transfer function to allow cascade connection and low power dissipation (requiring no enable signal to be furnished by a controller)
- ●Output shift direction pin selectable
- ●Ability to adjust offset bias of LCD source from V_{DD}
- ●Power supply for the logic ····· −5V±10%
- ●Si gate CMOS process
- ●Package·····100-pin QFP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin name	I/O	Functions
SEG0 to SEG79	O	LCD driving segment (column) outputs. Each output changes at the falling edge of LP.
D0 to D3	I	Display data inputs.
XSCL	I	Shift clock of display data (falling edge trigger).
LP	I	Latch pulse of display data (falling edge trigger).
EIO1, EIO2	I/O	Enable I/O, which is controlled by SHL input. Output is reset by LP, and automatically falls when 80 bits of data are taken in.
SHL	I	Shift direction selection and EIO pin I/O control. When data (a, b, c, d) (e, f, g, h)·····(w, x, y, z) are input to pins (D3, D2, D1, D0) respectively, the following relation is established between the data and segment outputs:
FR	I	AC signal of LCD driving outputs.
V_{DD}, V_{SS}	Power supplies	Logic circuit power. V_{DD}: 0V (GND) V_{SS}: −5.0V
V0, V2, V3, V5	Power supplies	LCD driving power. V5: −12 to −28V $V_{DD} \geq V0 \geq V2 > V3 \geq V5$

SHL	SEG													EIO	
	79	78	77	76	75	74	73	72	·····	3	2	1	0	1	2
L	a	b	c	d	e	f	g	h	·····	w	x	y	z	Output	Input
H	z	y	x	w	v	u	t	s	·····	d	c	b	a	Input	Output

■ABSOLUTE MAXIMUM RATINGS

(V_{DD}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	−7.0 to +0.3	V
Supply voltage (2)	V5	−30.0 to +0.3	V
Supply voltage (2)	V0,V2,V3*	V5−0.3 to +0.3	V
Input voltage (1)	V_I	V_{SS}−0.3 to +0.3	V
Output voltage (1)	V_O	V_{SS}−0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OSEG}	20	mA
Allowable power dissipation	P_D	300	mW
Operating temperature	T_{opr}	−20 to +75	°C
Storage temperature	T_{stg}	−65 to +150	°C
Soldering temperature·time	T_{sol}	260°C, 10s (at lead)	—

*V0, V2 and V3 must always satisfy the condition: $V_{DD} \geqq V0 \geqq V2 \geqq V3 \geqq V5$.

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(Unless otherwise specified, V_{DD}=V0=0V, V_{SS}=−5.0V±10%, and Ta=−20 to 75°C)

Parameter	Symbol	Conditions	Pin	Min	Typ	Max	Unit
Operating voltage (1)	V_{SS}		V_{SS}	−5.5	−5.0	−4.5	V
Recommended operating voltage Minimum operating voltage	V5		V5	−28.0	—	−12.0 −8.0	V
Operating voltage (2)	—	Recomended value	V0	−2.5	—	0	V
Operating voltage (3)	V2	Recomended value	V2	3/9·V5	—	V0	V
Operating voltage (4)	V3	Recomended value	V3	V5	—	6/9·V5	V
"H" input voltage	V_{IH}		EIO1,EIO2,XSCL, LP,D0 to D3,FR,SHL	0.2V_{SS}	—	—	V
"L" input voltage	V_{IL}			—	—	0.8V_{SS}	V
"H" output voltage	V_{OH}	I_{OH}=−0.6mA	EIO1, EIO2	−0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL}=0.6mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \leqq V_I \leqq 0V$	D0 to D3,XSCL, LP,SHL,FR	—	—	2.0	μA
	$I_{LI/O}$	$V_{SS} \leqq V_I \leqq 0V$	EIO1, EIO2	—	—	5.0	μA
Stand-by current	I_{DDS}	V5=−12.0 to −28.0V $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	V_{DD}	—	—	25	μA
Output resistance	R_{SEG}	$\lvert\Delta V_{on}\rvert$=0.5V, V5 = −20.0V	SEG0 to SEG79	—	1.5	3.5	kΩ
		V5 = −14.0V		—	2.0	4.5	
		V5 = −8.0V		—	3.0	8.0	
Current dissipation (1)	I_{SSO1}	V_{SS}=−5.0V, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$, f_{XSCL}=1.92MHz, f_{LP}=12kHz, Frame period=60Hz, Input data: Inverted bit by bit, No-load	V_{SS}	—	120	500	μA
Current dissipation (2)	I_{SSO2}	V_{SS}=−5.0V, V2=−4.0V, V3=−16.0V, V5=−20.0V, All other conditions are same as I_{SSO1}.	V5	—	20	100	μA
Input capacitance	C_I	Ta=25°C	D0 to D3,XSCL, LP,FR,SHL	—	—	8.0	pF
	$C_{I/O}$		EIO1, EIO2	—	—	15.0	pF

●AC Electrical Characteristics

(V_{SS} = −5.0±10%, Ta = −20 to 75°C)

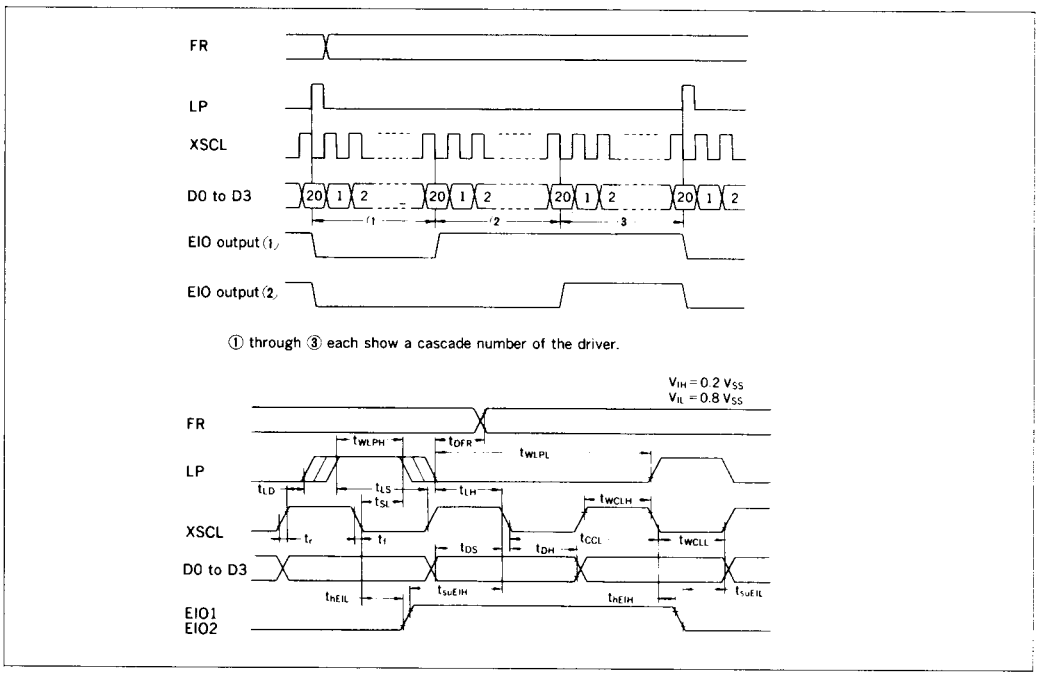
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
XSCL period	t_{CCL}	t_r, $t_f \leqq 10$ns	166	—	—	ns
XSCL "H" pulse width	t_{WCLH}		70	—	—	ns
XSCL "L" pulse width	t_{WCLL}		70	—	—	ns
Data setup time	t_{DS}		60	—	—	ns
Data hold time	t_{DH}		40	—	—	ns
XSCL-rise to LP-rise time	t_{LD}		0	—	—	ns
XSCL-fall to LP-fall time	t_{SL}		70	—	—	ns
LP-rise to XSCL-rise time	t_{LS}		70	—	—	ns
LP-fall to XSCL-fall time	t_{LH}		70	—	—	ns
LP "H" pulse width	t_{WLPH}		70	—	—	ns
LP "L" pulse width	t_{WLPL}		230	—	—	ns
Alloable FR delay time	t_{DFR}		−500	—	500	ns
Enable "H" setup time	t_{suEIH}		40	—	—	ns
Enable "H" hold time	t_{hEIH}		0	—	—	ns
Enable "L" setup time	t_{suEIL}		0	—	—	ns
Enable "L" hold time	t_{hEIL}		0	—	—	ns
Input signal rise time	t_r		—	—	50*	ns
Input signal fall time	t_f		—	—	50*	ns

*The specifications for t_r and t_f are provided to prevent a malfunction which may occur when noise is mixed with a slow-down signal. To assure high-speed XSCL, both t_r and t_f must satisfy the following relation:

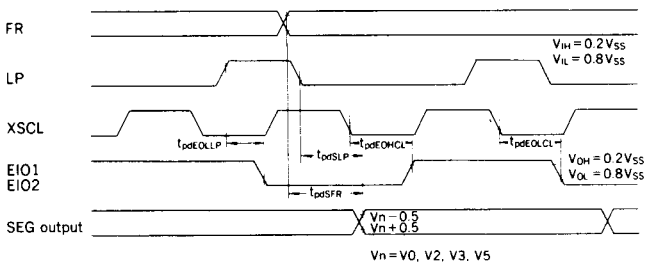
$$t_r, t_f < \frac{t_{CCL} - (t_{WCLH} + t_{WCLL})}{2}$$

●Timing Chart

○Input Timing



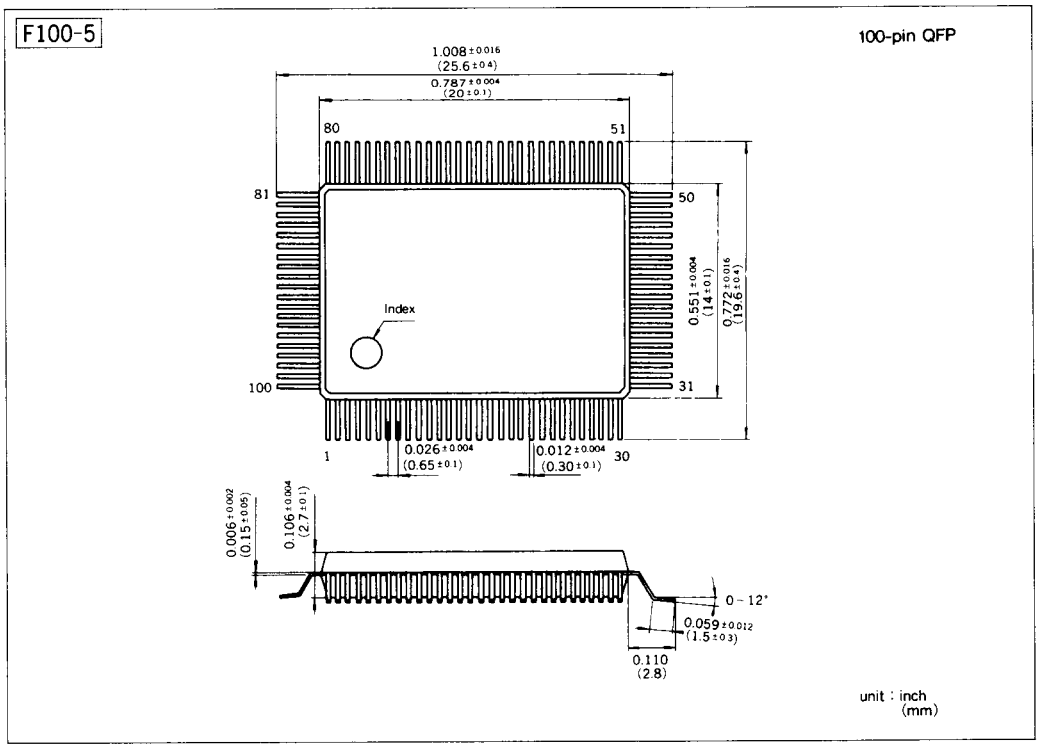
○ Output Timing



($V_{SS} = -5.0 \pm 10\%$, Ta = −20 to 75°C)

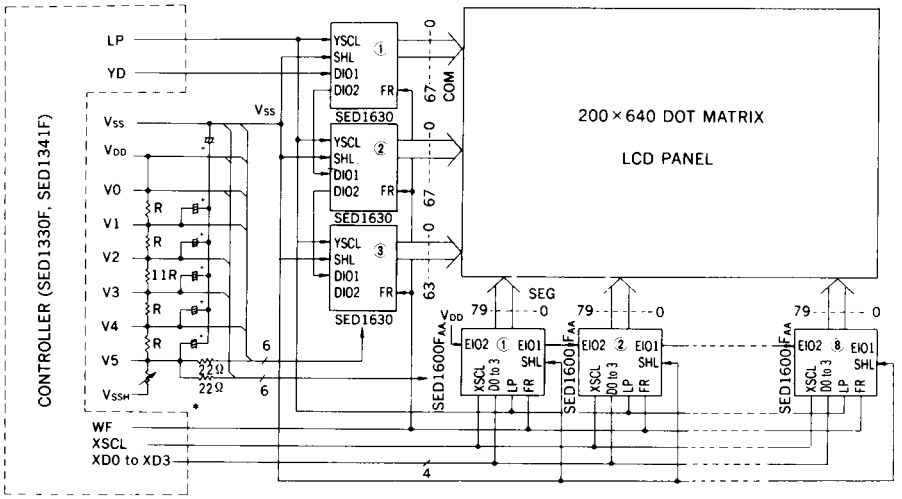
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(LP-rise to disable) time	$t_{pdEOLLP}$	XSCL = "L"	—	—	70	ns
(XSCL-fall to disable) time	$t_{pdEOLCL}$	LP = "H" C_L = 15pF	—	—	70	ns
(XSCL-fall to enable) time	$t_{pdEOHCL}$		—	—	100	ns
(LP-fall to SEG output) time	t_{pdSLP}	V5 = −12.0 to −28.0V	—	—	4.5	μs
(FR to SEG output) delay time	t_{pdSFR}	C_L = 100pF	—	—	4.5	μs

■PACKAGE DIMENSIONS



■EXAMPLE OF APPLICATION (SED1600F$_{AA}$)

for 200×640 DOT MATRIX LCD



*Be sure to connect a current limitter resistor. Also, connect decoupling capacitors (0.01ΩF) near pins V_{SS} and V5 of each LSI for noise protection.