CMOS 80-SEGMENT LCD DRIVER

- **80-bit High Voltage Output**
- **1/100 to 1/300 Display Duty**

■ DESCRIPTION

The SED1600 is a dot matrix LCD segment (column) driver for driving a high-capacity LCD panel at duty cycles higher than 1/100 (up to 1/300). The LSI has a wide range of LCD driving voltages. Due to the architecture of the SED1600, the LCD driving voltage, V0, is isolated from the V_{DD} supply. This provides the ability to adjust the offset bias independently of V_{DD}. These unique features allow the SED1600 to interface with a variety of LCD panels. The SED1600 does not require a controller to output an enable signal to implement daisy chain technology. This provides for easy interfacing with the LCD controllers such as the SED1330, SED1351, SED1335, or the SED1341.

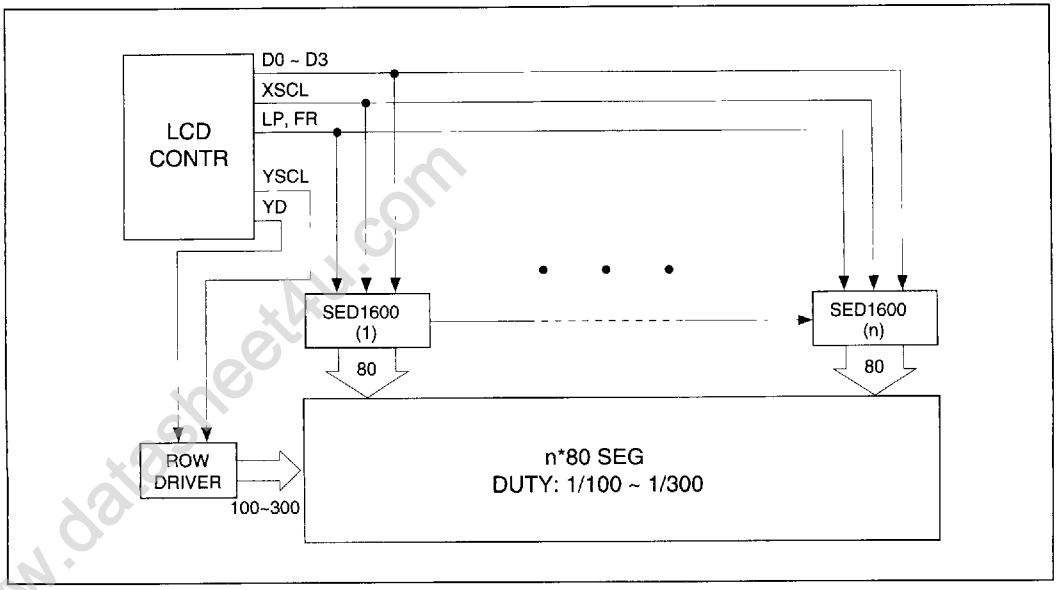
The SED1600 is used in conjunction with the SED1610 (86-row driver), SED1630 (68-bit row driver), SED1631 (100-row driver), SED1632 (86-bit row driver), SED1633 (100-bit row driver), and SED1634 (100-bit driver) to drive a large-capacity dot matrix LCD panel.

■ FEATURES

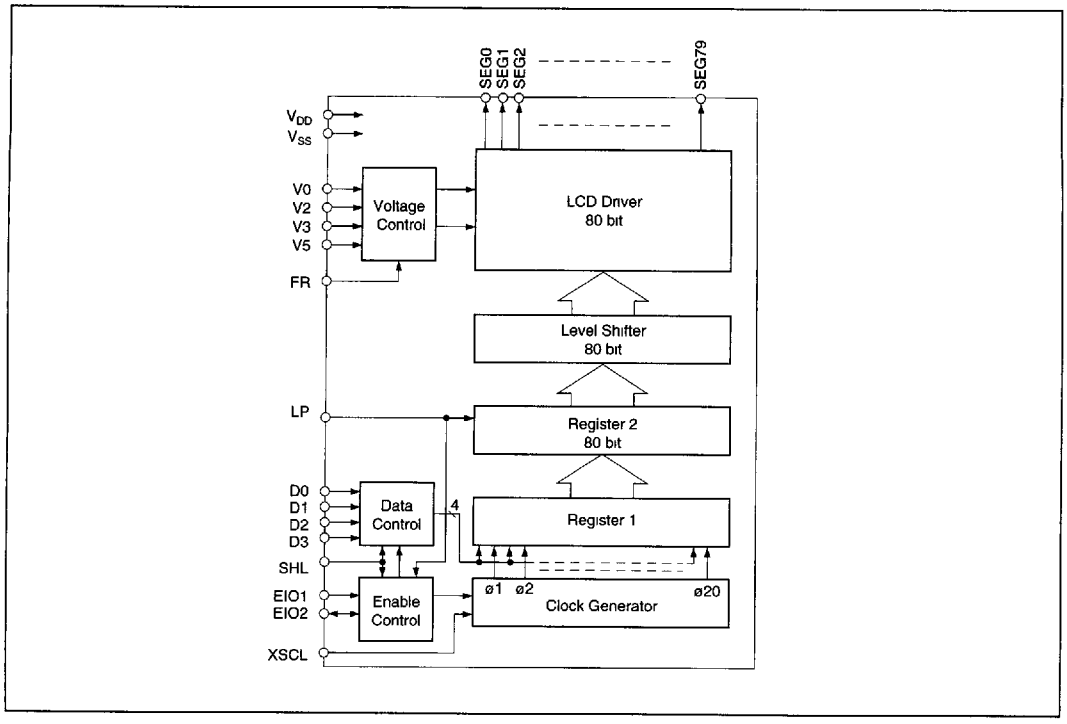
- Low-power CMOS technology
- 80-bit segment (column) driver
- High-speed 4-bit data bus with enable chain technology
- Duty cycle ..... 1/100 to 1/300
- Shift clock frequency ..... 6MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Daisy chain enable support
- Selectable output shift direction
- No enable signal by controller is required
- Wide range of LCD voltage .... –12 to –28V
- Supply voltage ..... 5.0V ± 10%
- Package ..... QFP5-100 pin (F_{AA})

  DIE: Al pad chip (D_{AA})
  Au bump (D_{AB})

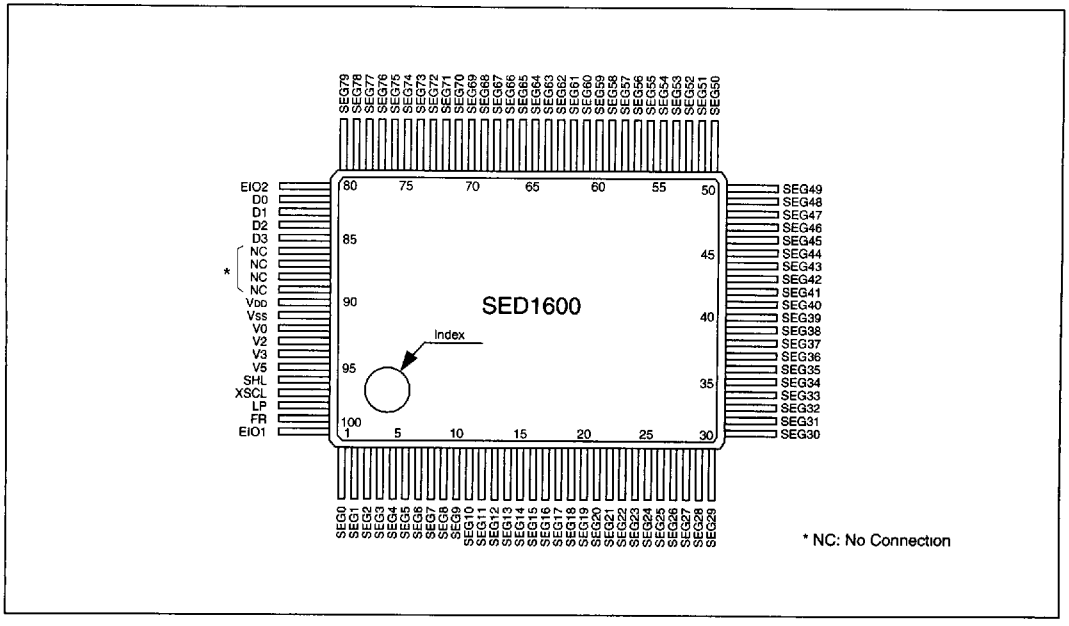
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>SEG0 to SEG79</td><td>O</td><td>LCD driving segment (column) outputs
Each output changes at the falling edge of LP.</td></tr>
<tr><td>D0 TO D3</td><td>I</td><td>Display data inputs.</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock of display data (falling edge trigger).</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse of display data (falling edge trigger).</td></tr>
<tr><td>EI01, EI02</td><td>I/O</td><td>Enable I/O, which is controlled by SHL input . Output is reset by LP, and automatically falls when 80 bits of data are taken in.</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO pin I/O control.
When data (a, b, c, d) (e, f, g, h)·····(w, x, y, z) are input to pins (D3, D2, D1, D0) respectively, the following relation is established between the data and segment outputs:
<table>
<tr><th rowspan="2">SHL</th><th colspan="12">SEG</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th>76</th><th>75</th><th>74</th><th>73</th><th>72</th><th>.....</th><th>3</th><th>2</th><th>1</th><th>0</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>.....</td><td>w</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>u</td><td>t</td><td>s</td><td>.....</td><td>d</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table></td></tr>
<tr><td>FR</td><td>I</td><td>AC signal of LCD driving outputs.</td></tr>
<tr><td>VDD, VSS</td><td>Power Supplies</td><td>Logic circuit power.
VDD: 0 V (GND)
VSS: –5.0 V</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power Supplies</td><td>LCD driving power.
V5: –12 to –28 V
VDD ≥ V0 ≥ V2 > V3 ≥ V5</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(VDD = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	VSS	–7.0 to +0.3	V
Supply voltage (2)	V5	–30.0 to +0.3	V
Supply voltage (2)	V0, V2, V3*	V5 –0.3 to +0.3	V
Input voltage (1)	VI	VSS –0.3 to +0.3	V
Output voltage (1)	VO	VSS –0.3 to +0.3	V
Output current (1)	IO	20	mA
Output current (2)	IOSEG	20	mA
Allowable power dissipation	PD	300	mW
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–65 to +150	°C
Soldering temperature, time	Tsol	260°C, 10 sec (at lead)	—

* V0, V2 and V3 must always satisfy the condition VDD ≥ V0 ≥ V2 ≥ V3 ≥ V5.

● DC Electrical Characteristics

(Unless otherwise specified, V_{DD} = V0 = 0V, V_{SS} = –5.0 V ± 10%, T_a = –20 to 85°C)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Operating voltage	V_{SS}		V_{SS}	–5.5	–5.0	–4.5	V
Recommended op. voltage Minimum operating voltage	V5		V5	–28.0	—	–12.0 –8.0	V
Operating voltage	—	Recommended value	V0	–2.5	—	0	V
Operating voltage	V2	Recommended value	V2	3/9·V5	—	V0	V
Operating voltage	V3	Recommended value	V3	V5	—	6/9·V5	V
"H" input voltage	V_{IH}		EI01, EI02, XSCL, LP, D0 to D3, FR, SHL	0.2V_{SS}	—	—	V
"L" input voltage	V_{IL}			—	—	0.8V_{SS}	V
"H" output voltage	V_{OH}	I_{OH} = –0.6 mA	EI01, EI02	–0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_I \le 0$ V	D0 to D3, LP XSCL, SHL, FR	—	—	2.0	µA
	$I_{LI/O}$	$V_{SS} \le V_I \le 0$ V	EI01, EI02	—	—	5.0	µA
Stand–by current	I_{DDS}	V5 = –12.0 to –28.0 V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{SEG}	|ΔVon| = 0.5V, V5 = –20.0V	SEG0 to SEG79	—	1.5	3.5	kΩ
		|ΔVon| = 0.5V, V5 = –14.0V		—	2.0	4.5	kΩ
		|ΔVon| = 0.5V, V5 = –8.0V		—	3.0	8.0	kΩ
Current dissipation (1)	I_{SSO1}	V_{SS} = –5.0 V, V_{IH} = V_{DD} V_{IL} = V_{SS}, f_{XSCL} =1.92 MHz f_{LP} = 12 kHz, Frame period = 60 Hz; Input data: Inverted bit by bit, No-load	V_{SS}	—	120	500	µA
Current dissipation (2)	I_{SSO2}	V_{SS} = –5.0 V, V2 = –4.0 V V3 = –16.0 V, V5 = –20.0 V All other conditions are same as I_{SSO1}	V5	—	20	100	µA
Input capacitance	C_I	T_a = 25°C	D0 to D3, LP XSCL, SHL, FR	—	—	8.0	pF
	$C_{I/O}$		EI01, EI02	—	—	15.0	pF

● AC Electrical Characteristics

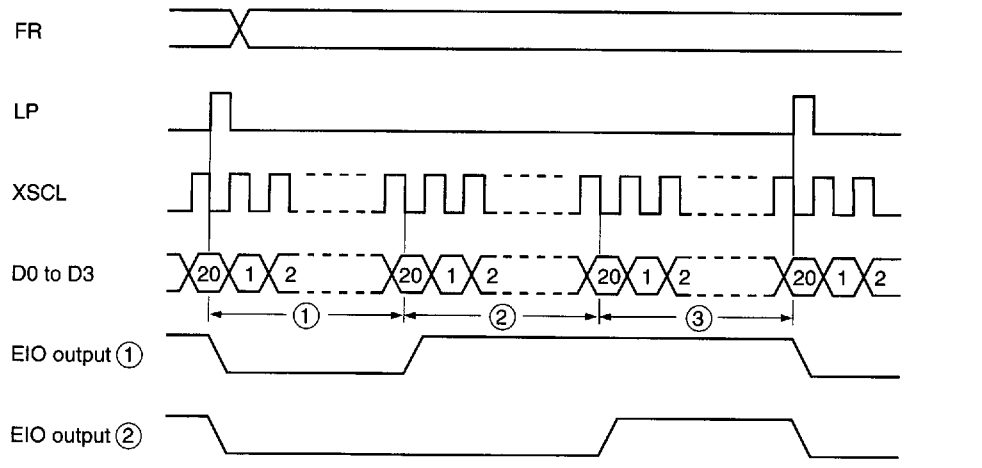
(V_{SS} = –5.0 V ±10%, T_a = –20 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
XSCL period	t_{CCL}	t_r, $t_f \leq 10$ ns	166	—	—	ns
XSCL "H" pulse width	t_{WCLH}		70	—	—	ns
XSCL "L" pulse width	t_{WCLL}		70	—	—	ns
Data setup time	t_{DS}		60	—	—	ns
Data hold time	t_{DH}		40	—	—	ns
XSCL-rise to LP-rise time	t_{LD}		0	—	—	ns
XSCL-fall to LP-fall time	t_{SL}		70	—	—	ns
LP-rise to XSCL-rise time	t_{LS}		70	—	—	ns
LP-fall to XSCL-fall time	t_{LH}		70	—	—	ns
LP "H" pulse width	t_{WLPH}		70	—	—	ns
LP "L" pulse width	t_{WLPL}		230	—	—	ns
Allowable FR delay time	t_{DFR}		–500	—	500	ns
Enable "H" setup time	t_{suEIH}		40	—	—	ns
Enable "H" hold time	t_{hEIH}		0	—	—	ns
Enable "L" setup time	t_{suEIL}		0	—	—	ns
Enable "L" hold time	t_{hEIL}		0	—	—	ns
Input signal rise time	t_r		—	—	50*	ns
Input signal fall time	t_f		—	—	50*	ns

* Note: The specifications for t_r and t_f are provided to prevent a malfunction which may occur when noise is mixed with a slow-down signal. To assure high-speed XSCL, both t_r and t_f must satisfy the following relation:

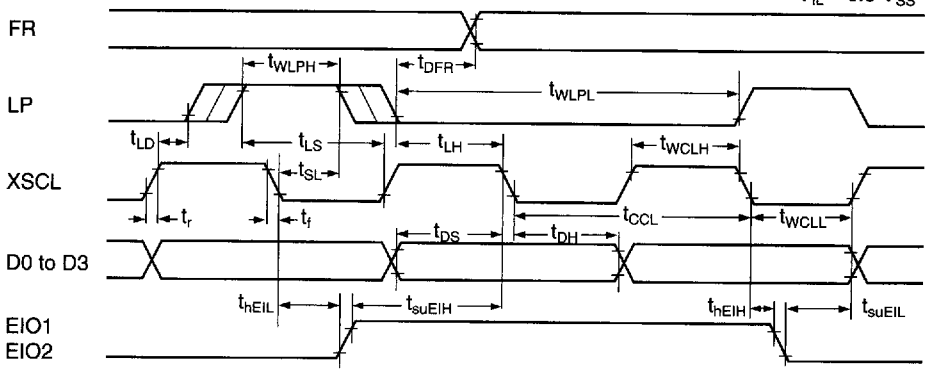
$$t_r, t_f < \frac{t_{CCL} - (t_{WCLH} + t_{WCLL})}{2}$$

● **Timing Chart**
○ **Input Timing**

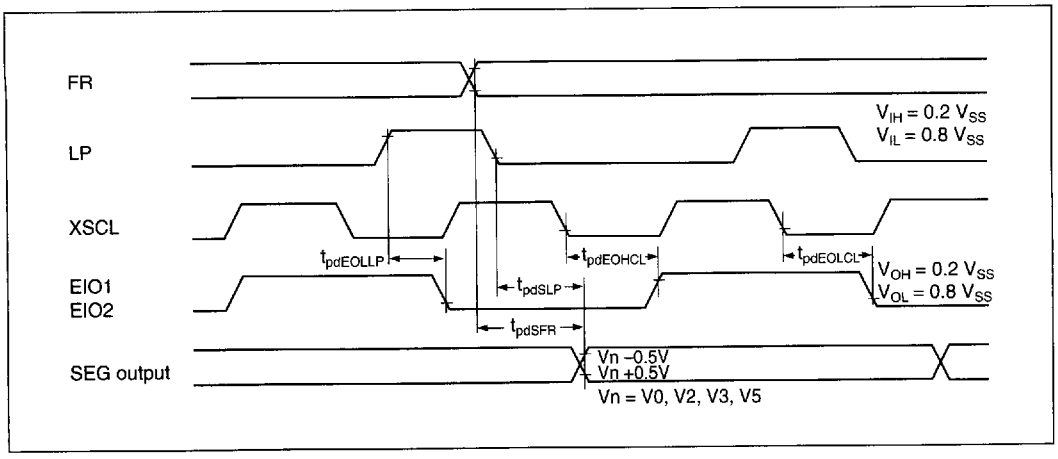


① through ③ each show a cascade number of the driver.

$V_{IH} = 0.2\ V_{SS}$
$V_{IL} = 0.8\ V_{SS}$



○ **Output Timing**

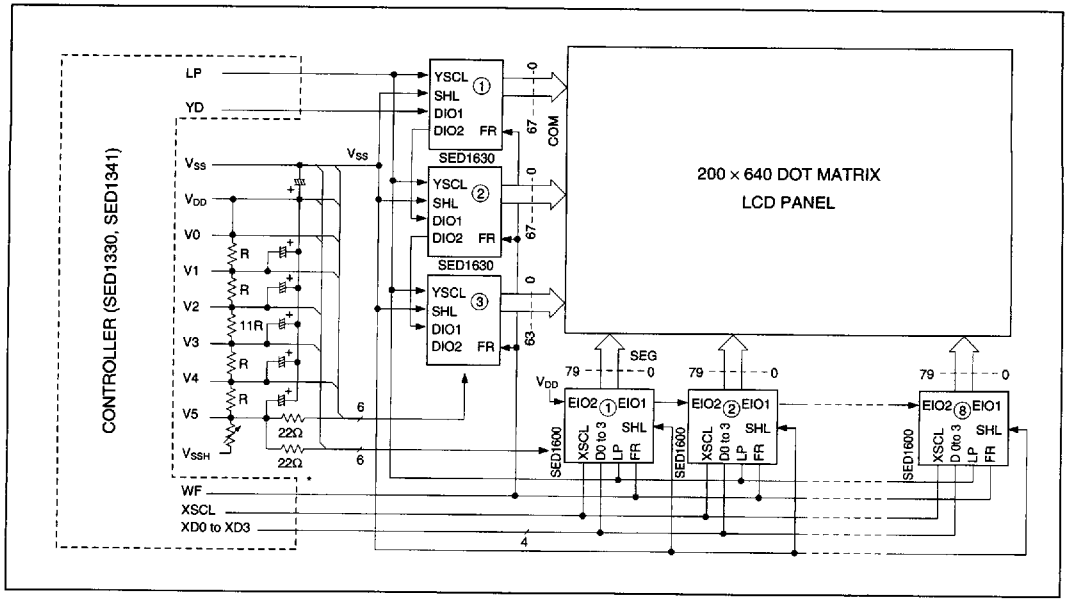


(V_{SS} = −5.0 V ±10%, T_a = −20 to 85°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
(LP-rise to disable) time	$t_{pdEOLLP}$	XSCL = "L"	C_L = 15 pF	—	—	70	ns
(XSCL-fall to disable) time	$t_{pdEOLCL}$	LP = "H"		—	—	70	ns
(XSCL-fall to enable) time	$t_{pdEOHCL}$			—	—	100	ns
(LP-fall to SEG output) time	t_{pdSLP}	V5 = −12.0 to −28.0 V		—	—	4.5	µs
(FR to SEG output) delay time	t_{pdSFR}	C_L = 100 pF		—	—	4.5	µs

■ EXAMPLE OF APPLICATION (SED1600)

(for 200 × 640 DOT MATRIX LCD)

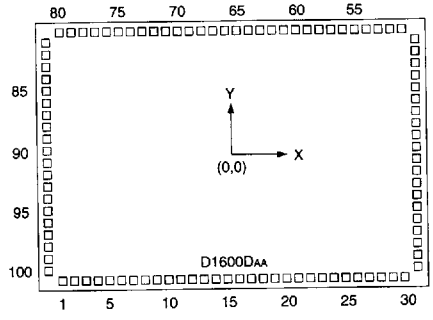


Note:

* Be sure to connect a current limiter resistor. Also, connect decoupling capacitors (0.01μF) near pins Vss and V5 of each LSI for noise protection.

■ PAD LAYOUT / PAD COORDINATION

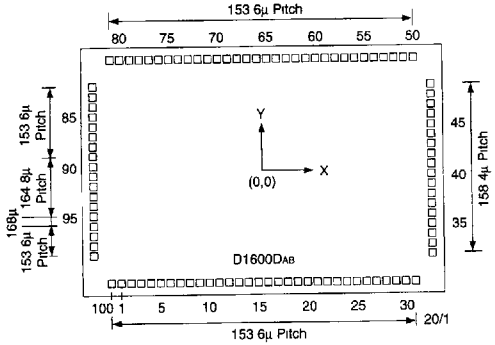
● SED1600DAA (AL PAD)



Chip Specification	Dimension (mm)
Chip size	5.59 × 3.50
Pad pitch	0.160 min.
Chip thickness	0.40 ±0.025
Pad surface area	0.10mm

Pad No	Pad Name	X (μm)	Y (μm)	Pad No	Pad Name	X (μm)	Y (μm)	Pad No	Pad Name	X (μm)	Y (μm)
1	SEG0	−2461	−1588	35	SEG34	2632	−881	69	SEG68	−560	1588
2	SEG1	−2261	−1588	36	SEG35	2632	−721	70	SEG69	−720	1588
3	SEG2	−2069	−1588	37	SEG36	2632	−561	71	SEG70	−880	1588
4	SEG3	−1886	−1588	38	SEG37	2632	−401	72	SEG71	−1040	1588
5	SEG4	−1709	−1588	39	SEG38	2632	−241	73	SEG72	−1203	1588
6	SEG5	−1538	−1588	40	SEG39	2632	−81	74	SEG73	−1366	1588
7	SEG6	−1366	−1588	41	SEG40	2632	79	75	SEG74	−1538	1588
8	SEG7	−1203	−1588	42	SEG41	2632	239	76	SEG75	−1709	1588
9	SEG8	−1040	−1588	43	SEG42	2632	399	77	SEG76	−1885	1588
10	SEG9	−880	−1588	44	SEG43	2632	559	78	SEG77	−2069	1588
11	SEG10	−720	−1588	45	SEG44	2632	719	79	SEG78	−2261	1588
12	SEG11	−560	−1588	46	SEG45	2632	879	80	SEG79	−2461	1588
13	SEG12	−400	−1588	47	SEG46	2632	1039	81	EI02	−2632	1546
14	SEG13	−240	−1588	48	SEG47	2632	1204	82	D0	−2632	1372
15	SEG14	−80	−1588	49	SEG48	2632	1372	83	D1	−2632	1204
16	SEG15	80	−1588	50	SEG49	2632	1546	84	D2	−2632	1039
17	SEG16	240	−1588	51	SEG50	2461	1588	85	D3	−2632	879
18	SEG17	400	−1588	52	SEG51	2261	1588	86	(D4)	−2632	719
19	SEG18	560	−1588	53	SEG52	2069	1588	87	(D5)	−2632	559
20	SEG19	720	−1588	54	SEG53	1885	1588	88	(D6)	−2632	399
21	SEG20	880	−1588	55	SEG54	1709	1588	89	(D7)	−2632	239
22	SEG21	1040	−1588	56	SEG55	1538	1588	90	VDD	−2632	79
23	SEG22	1203	−1588	57	SEG56	1366	1588	91	Vss	−2632	−81
24	SEG23	1366	−1588	58	SEG57	1203	1588	92	V0	−2632	−241
25	SEG24	1538	−1588	59	SEG58	1040	1588	93	V2	−2632	−401
26	SEG25	1709	−1588	60	SEG59	880	1588	94	V3	−2632	−561
27	SEG26	1885	−1588	61	SEG60	720	1588	95	V5	−2632	−721
28	SEG27	2069	−1588	62	SEG61	560	1588	96	SHL	−2632	−881
29	SEG28	2261	−1588	63	SEG62	400	1588	97	XSCL	−2632	−1041
30	SEG29	2461	−1588	64	SEG63	240	1588	98	LP	−2632	−1206
31	SEG30	2632	−1548	65	SEG64	80	1588	99	FR	−2632	−1374
32	SEG31	2632	−1374	66	SEG65	−80	1588	100	EI01	−2632	−1548
33	SEG32	2632	−1206	67	SEG66	−240	1588				
34	SEG33	2632	−1040	68	SEG67	−400	1588				

● SED1600DAB (AU PAD)



Chip Specification	Dimension (mm)
Chip size	5.59 × 3.50
Pad pitch	0.153 min.
Chip thickness	0.525 ±0.025

Pad No	Pad Name	X (μm)	Y (μm)	Pad No	Pad Name	X (μm)	Y (μm)	Pad No	Pad Name	X (μm)	Y (μm)
1	SEG0	−2227	−1578	35	SEG34	2622	−871	69	SEG68	−538	1578
2	SEG1	−2074	−1578	36	SEG35	2622	−713	70	SEG69	−691	1578
3	SEG2	−1920	−1578	37	SEG36	2622	−554	71	SEG70	−845	1578
4	SEG3	−1766	−1578	38	SEG37	2622	−396	72	SEG71	−998	1578
5	SEG4	−1613	−1578	39	SEG38	2622	−238	73	SEG72	−1152	1578
6	SEG5	−1459	−1578	40	SEG39	2622	−79	74	SEG73	−1305	1578
7	SEG6	−1305	−1578	41	SEG40	2622	79	75	SEG74	−1459	1578
8	SEG7	−1152	−1578	42	SEG41	2622	238	76	SEG75	−1613	1578
9	SEG8	−998	−1578	43	SEG42	2622	396	77	SEG76	−1766	1578
10	SEG9	−845	−1578	44	SEG43	2622	554	78	SEG77	−1920	1578
11	SEG10	−691	−1578	45	SEG44	2622	713	79	SEG78	−2074	1578
12	SEG11	−538	−1578	46	SEG45	2622	871	80	SEG79	−2227	1578
13	SEG12	−384	−1578	47	SEG46	2622	1030	81	EI02	−2381	1578
14	SEG13	−230	−1578	48	SEG47	2622	1188	82	D0	−2622	1346
15	SEG14	−77	−1578	49	SEG48	2622	1346	83	D1	−2622	1193
16	SEG15	77	−1578	50	SEG49	2381	1578	84	D2	−2622	1039
17	SEG16	230	−1578	51	SEG50	2227	1578	85	D3	−2622	886
18	SEG17	384	−1578	52	SEG51	2074	1578	86	(D4)	−2622	732
19	SEG18	538	−1578	53	SEG52	1920	1578	87	(D5)	−2622	578
20	SEG19	691	−1578	54	SEG53	1766	1578	88	(D6)	−2622	425
21	SEG20	845	−1578	55	SEG54	1613	1578	89	(D7)	−2622	271
22	SEG21	998	−1578	56	SEG55	1459	1578	90	VDD	−2622	106
23	SEG22	1152	−1578	57	SEG56	1305	1578	91	Vss	−2622	−58
24	SEG23	1305	−1578	58	SEG57	1152	1578	92	V0	−2622	−223
25	SEG24	1459	−1578	59	SEG58	998	1578	93	V2	−2622	−388
26	SEG25	1613	−1578	60	SEG59	845	1578	94	V3	−2622	−553
27	SEG26	1766	−1578	61	SEG60	691	1578	95	V5	−2622	−718
28	SEG27	1920	−1578	62	SEG61	538	1578	96	SHL	−2622	−886
29	SEG28	2074	−1578	63	SEG62	384	1578	97	XSCL	−2622	−1039
30	SEG29	2227	−1578	64	SEG63	230	1578	98	LP	−2622	−1193
31	SEG30	2381	−1578	65	SEG64	77	1578	99	FR	−2622	−1346
32	SEG31	2622	−1346	66	SEG65	−77	1578	100	EI01	−2381	−1578
33	SEG32	2622	−1188	67	SEG66	−230	1578				
34	SEG33	2622	−1030	68	SEG67	−384	1578				