EPSON

SED1606

Dot Matrix High Duty LCD Driver

- 80-bit High Voltage Resistant Output
- 1/100 to 1/300 in Display Duty
- CMOS High Voltage Resistant Process

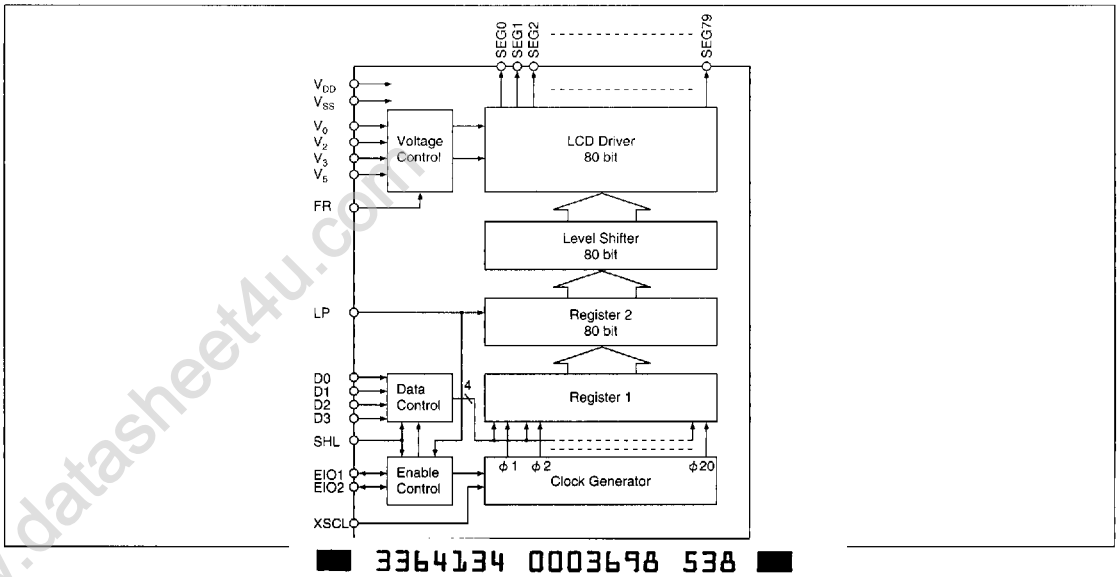
DESCRIPTION

The SED1606 is an 80 output segment (column) driver, used to driver large-capacity dot matrix LCD panels with a duty ratio of 1/300 (from 1/100). It is used in conjunction with the SED1670/71/72 common (row) drivers. The SED1606 has a wide range of driving voltages. The maximum voltage V_0 is isolated from V_{DD} to enable the application of any external LCD driving bias voltage from outside to the SED1606. These unique features enable the SED1606 to operate with a wide variety of LCD panels. The SED1606 requires no enable signal to implement an enable chain technology which provides low power dissipation. This offers simpler interface with the LCD controller SED1330F/SED1351F or a microprocessor.

FEATURES

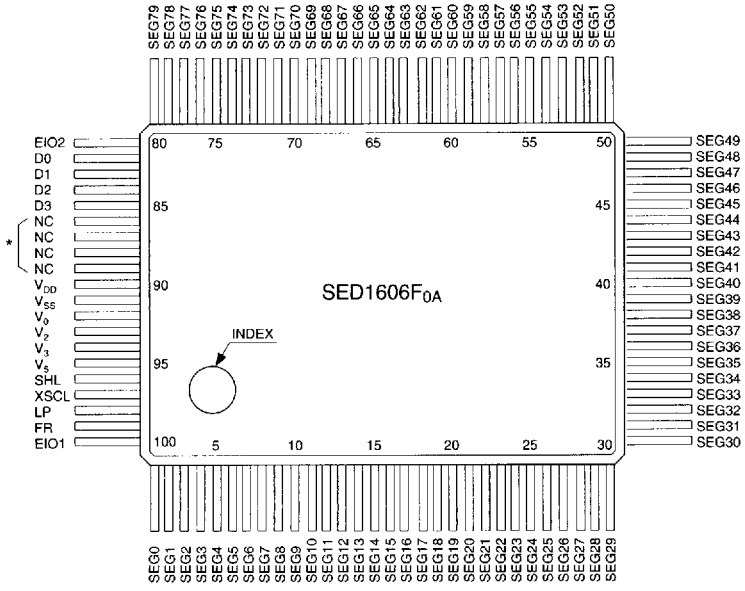
- 80 LCD driving outputs
- Display capacity ..... 640 × 200 × 3 dots when combined with SED1670/71/72
- Wide range of LCD driving voltages ..... 12 to 28V
  (Absolute maximum voltage ..... 30V)
- High-speed, low-power data transfer by 4-bit bus enable chain technology
  Shift clock ..... 6.5MHz Max.
- Enable auto-transfer function to allow cascade connection and low power dissipation (requiring no enable signal to be furnished by a controller)
- Output shift direction pin selectable
- Ability to adjust offset bias of LCD source from V_{DD}
- Power supply for the logic ..... 2.7V to 5.5V
- Silicon gate CMOS process
- Package ..... SED1606F_{0A}: QFP5-100pin (plastic)
  SED1606D_{0A}: Die form (Al pad)
  SED1606D_{0B}: Die form (Au bump)

BLOCK DIAGRAM



■PIN CONFIGURATION

QFP5-100pin



*NC: No Connection

■PIN DESCRIPTION

Pin name	I/O	Function
SEG0 to SEG79	O	LCD driving segment (column) outputs. Each output changes at the falling edge of LP.
D0 to D3	I	Display data inputs.
XSCL	I	Shift clock of display data (falling edge trigger).
LP	I	Latch pulse of display data (falling edge trigger).
EIO1, EIO2	I/O	Enable I/O, which is controlled by SHL input. Output is reset by LP, and automatically falls when 80 bits of data are taken in.
SHL	I	Shift direction selection and EIO pin I/O control. When data (a, b, c, d)(e, f, g, h)·····(w, x, y, z) are input to pins (D3, D2, D1, D0) respectively, the following relation is established between the data and segment outputs:
FR	I	Input for AC comersion of LCD driving outputs.
V_{DD}, V_{SS}	Power supplies	Logic circuit power. V_{DD}: 0V (GND) V_{SS}: -5.0V
V_0, V_2, V_3, V_5	Power supplies	LCD driving power. V_5: -12 to -28V $V_{DD} \geqq V_0 \geqq V_2 \geqq V_3 \geqq V_5$

SHL	SEG													EIO	
	79	78	77	76	75	74	73	72	····	3	2	1	0	1	2
L	a	b	c	d	e	f	g	h	····	w	x	y	z	Output	Input
H	z	y	x	w	v	u	t	s	····	d	c	b	a	Input	Output

■ ABSOLUTE MAXIMUM RATINGS

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage (1)	V_{SS}	-7.0 to+0.3	V
Supply voltage (2)	V_5	-30.0 to+0.3	V
Supply voltage (3)	V_0, V_2, V_3*	V_5-0.3 to+0.3	V
Input voltage (1)	V_I	V_{SS}-0.3 to+0.3	V
Output voltageb (1)	V_O	V_{SS}-0.3 to+0.3	V
Output currentb (1)	I_O	20	mA
Output current (2)	I_{OSEG}	20	mA
Allowable power dissipation	P_D	300	mW
Operating temperature	T_{opr}	-20 to+85	°C
Storage temperature	T_{stg}	-65 to +150	°C
Soldering temperature·time	T_{sol}	260°C, 10s (at lead)	—

*V_0, V_2 and V_3 must always satisfy the condition: $V_{DD} \geqq V_0 \geqq V_2 \geqq V_3 \geqq V_5$

■ ELECTRICAL CHARACTERISTICS

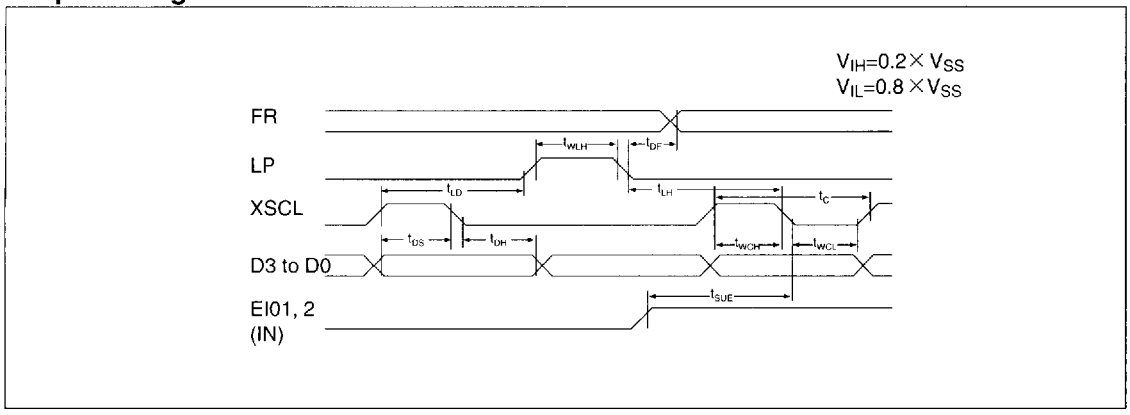
● DC Characteristics

(Unless otherwise specified, V_{DD}=V_0=0V, V_{SS}=-5.0V±10%, and Ta=-40 to 85°C)

Characteristic	Symbol	Condition	Pin	Min.	Typ.	Max.	Unit
Operating voltage (1)	V_{SS}		V_{SS}	-5.5	-5.0	-2.7	V
Recommended operating voltage Minimum operating voltage	V_5		V_5	-28.0	—	-12.0 -8.0	V
Operating voltage (2)	—	Recomended value	V_0	-2.5	—	0	V
Operating voltage (3)	V_2	Recomended value	V_2	3/9·V_5	—	V_0	V
Operating voltage (4)	V_3	Recomended value	V_3	V_5	—	6/9·V_5	V
"H" input voltage	V_{IH}		EIO1, EIO2, XSCL, LP, D0 to D3, FR, SHL	0.2V_{SS}	—	—	V
"L" input voltage	V_{IL}			—	—	0.8V_{SS}	V
"H" output voltage	V_{OH}	I_{OH}=-0.6mA	EIO1, EIO2	-0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL}=0.6mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \leqq V_1 \leqq 0V$	D0 to D3, XSCL, LP, SHL, FR	—	—	2.0	μA
	$I_{LI/O}$	$V_{SS} \leqq V_1 \leqq 0V$	EIO1, EIO2	—	—	5.0	μA
Stand-by current	I_{DDS}	V_5=-12.0 to -28.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}	V_{DD}	—	—	25	μA
Output resistance	R_{SEG}	|⊿Von| =0.5V, V_5	SEG0 to SEG79	—	1.2	1.6	kΩ
Current dissipation (1)	I_{SSO1}	V_{SS}=-5.0V, V_{IH}=V_{DD}, V_{IL}=V_{SS}, f_{XSCL}=2.69MHz, f_{LP}=16.8kHz, Frame period=70Hz, Input data: Inverted bit by bit, No-load	V_{SS}	—	100	200	μA
Current dissipation (2)	I_{SSO2}	V_{SS}=-5.0V, V_2=-9.3V, V_3=-18.6V, V_5=-28.0V, All other conditions are same as I_{SSO1}.	V_5	—	50	80	μA
Input capacitance	C_I	Ta=25°C	D0 to D3, XSCL, LP, FR, SHL	—	—	8.0	pF
	$C_{I/O}$		EIO1, EIO2	—	—	15.0	pF

● AC Electrical Characteristics

○ Input timing characteristics



(V_{DD}=0V, V_{SS}=-5.0V±0.5V, Ta=-40 to 85°C)

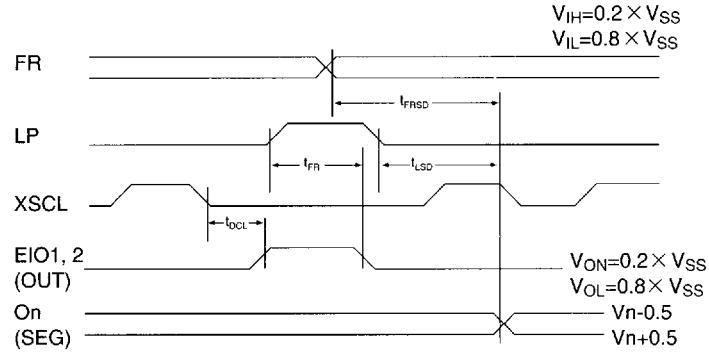
Parameter	Symbol	Condition	Min.	Typ.	Unit
XSCL period	t_C	—	100	—	ns
XSCL "H" pulsewidth	t_{WCH}	—	30	—	ns
XSCL "L" pulsewidth	t_{WCL}	—	30	—	ns
Data setup time	t_{DS}	—	20	—	ns
Data hold time	t_{DH}	—	10	—	ns
XSCL-rise to LP-rise time	t_{LD}	—	0	—	ns
LP-fall to XSCL-fall time	t_{LH}	—	40	—	ns
LP "H" pulsewidth	t_{WLH}	*3	40	—	ns
Allowable FR delay time	t_{DF}	—	-900	+900	ns
EIO setup time	t_{SUE}	—	35	—	ns

(V_{DD}=0V, V_{SS}=-4.5V to -2.7V, Ta=-40 to 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Unit
XSCL period	t_C	V_{SS}=-2.7V*1	153	—	ns
		V_{SS}=-3.0V*2	153	—	
XSCL"H"pulsewidth	t_{WCH}	—	50	—	ns
XSCL"L"pulsewidth	t_{WCL}	—	50	—	ns
Data setup time	t_{DS}	—	30	—	ns
Data hold time	t_{DH}	—	15	—	ns
XSCL-rise to LP-rise time	t_{LD}	—	0	—	ns
LP-fall to XSCL-fall time	t_{LH}	V_{SS}=-2.7V	75	—	ns
		V_{SS}=-3.0V	65	—	
LP "H" pulsewidth	t_{WLH}	V_{SS}=-2.7V*3	75	—	ns
		V_{SS}=-3.0V*3	65	—	
Allowable FR delay time	t_{DF}	—	-900	+900	ns
EIO setup time	t_{SUE}	V_{SS}=-2.7V	60	—	ns
		V_{SS}=-3.0V	51	—	

*1 Equivalent to 6.5MHz
*2 Equivalent to 7.5MHz
*3 t_{WLH} stipulates the time when LP is "H" and XSCL is "L".
*4 t_r and t_f of input signal are stipulated by unit of 20 ns.
*5 At a high-speed operation, t_r and $fr=\{t_C-(t_{DCL}+t_{SUE})\}/2$

○ Output Timing Characteristics



(V_{DD}=0V, V_{SS}=-5.0V±0.5V, V_5=-12.0 to -28.0V)

Parament	Symbol	Condition	Min.	Max.	Unit
EIO reset time	t_{ER}	C_L=15pF (EIO)	—	90	ns
EIO output delay time	tDCL		—	55	ns
LP to SEG output delay time	t_{LSD}	C_L=15pF (On)	—	200	ns
FR to SEG output delay time	t_{FRSD}		—	400	ns

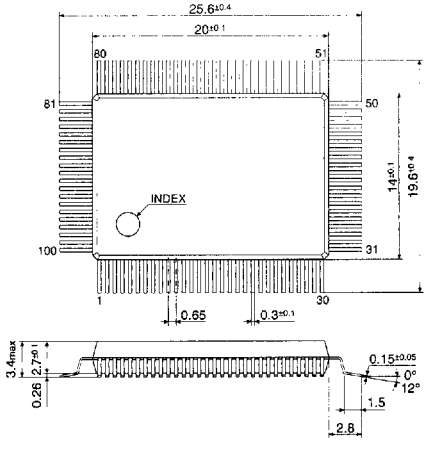
(V_{DD}=0V, V_{SS}=-4.5V to 2.7V, V_5=-12.0 to -28.0V)

Parament	Symbol	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	C_L=15pF (EIO)		—	150	ns
EIO output delay time	tDCL		V_{SS}=-2.7V	—	88	ns
			V_{SS}=-3.0V	—	77	ns
LP to SEG output delay time	t_{LSD}	C_L=100pF (On)		—	400	ns
FR to SEG output delay time	t_{FRSD}			—	800	ns

*1 t_r and t_f of input signal are stipulated by unit of 20ns.
*2 At a high-speed operation, t_r and fr={t_C-(t_{DCL}+t_{SUE})}/2

■PACKAGE DIMENSIONS

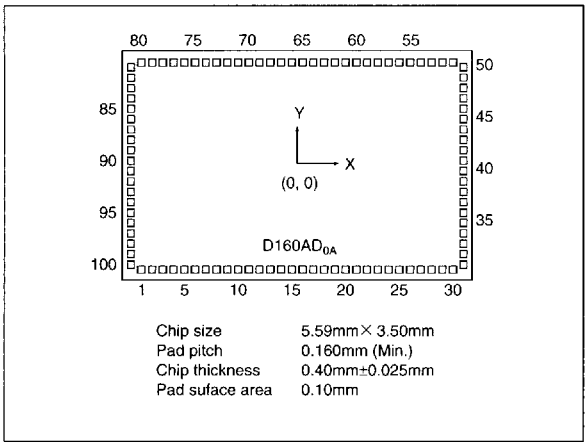
Plastic QFP5-100pin



Unit: mm

■PAD LAYOUT/PAD COORDINATES

● SED1606D$_{0A}$

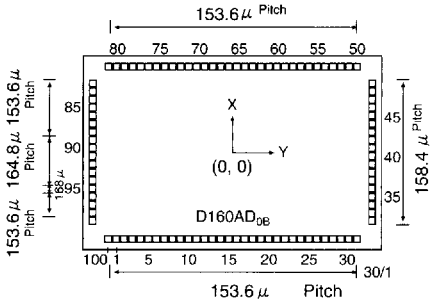


Chip size	5.59mm× 3.50mm
Pad pitch	0.160mm (Min.)
Chip thickness	0.40mm±0.025mm
Pad suface area	0.10mm

Unit: μm

PAD No	PAD Name	COORDINATES X	COORDINATES Y
1	SEG0	-2461	-1588
2	SEG1	-2261	
3	SEG2	-2069	
4	SEG3	-1886	
5	SEG4	-1709	
6	SEG5	-1538	
7	SEG6	-1366	
8	SEG7	-1203	
9	SEG8	-1040	
10	SEG9	-880	
11	SEG10	-720	
12	SEG11	-560	
13	SEG12	-400	
14	SEG13	-240	
15	SEG14	-80	
16	SEG15	80	
17	SEG16	240	
18	SEG17	400	
19	SEG18	560	
20	SEG19	720	
21	SEG20	880	
22	SEG21	1040	
23	SEG22	1203	
24	SEG23	1366	
25	SEG24	1538	
26	SEG25	1709	
27	SEG26	1885	
28	SEG27	2069	
29	SEG28	2261	
30	SEG29	2461	
31	SEG30	2632	-1548
32	SEG31	2632	-1374
33	SEG32	2632	-1206
34	SEG33	2632	-1041
35	SEG34	2632	-881
36	SEG35		-721
37	SEG36		-561
38	SEG37		-401
39	SEG38		-241
40	SEG39		-81
41	SEG40		79
42	SEG41		239
43	SEG42		399
44	SEG43		559
45	SEG44		719
46	SEG45		879
47	SEG46		1039
48	SEG47		1204
49	SEG48		1372
50	SEG49		1546
51	SEG50	2461	1586
52	SEG51	2261	
53	SEG52	2069	
54	SEG53	1885	
55	SEG54	1709	
56	SEG55	1538	
57	SEG56	1366	
58	SEG57	1203	
59	SEG58	1040	
60	SEG59	880	
61	SEG60	720	
62	SEG61	560	
63	SEG62	400	
64	SEG63	240	
65	SEG64	80	
66	SEG65	-80	
67	SEG66	-240	
68	SEG67	-400	
69	SEG68	-560	1588
70	SEG69	-720	
71	SEG70	-880	
72	SEG71	-1040	
73	SEG72	-1203	
74	SEG73	-1366	
75	SEG74	-1538	
76	SEG75	-1709	
77	SEG76	-1885	
78	SEG77	-2069	
79	SEG78	-2261	
80	SEG79	-2461	
81	EIO2	-2632	1546
82	D0		1372
83	D1		1204
84	D2		1039
85	D3		879
86	(D4)		719
87	(D5)		559
88	(D6)		399
89	(D7)		239
90	V_{DD}		79
91	V_{SS}		-81
92	V0		-241
93	V2		-401
94	V3		-561
95	V5		-721
96	SHL		-881
97	XSCL		-1041
98	LP		-1206
99	FR		-1374
100	EIO1		-1548

● SED1606D$_{0B}$



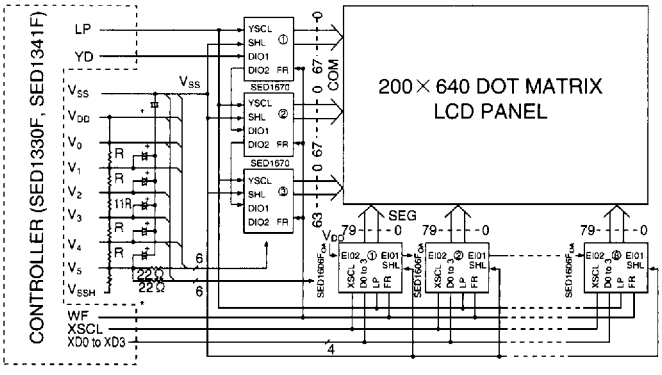
Chip size	5.59mm× 3.50mm
Pad pitch	0.153mm (Min.)
Chip thickness	0.525mm±0.025

Unit: μm

PAD No	PAD Name	Actual dimensions X	Actual dimensions Y
1	O0	-2227	-1578
2	O1	-2074	
3	O2	-1920	
4	O3	-1766	
5	O4	-1612	
6	O5	-1459	
7	O6	-1305	
8	O7	-1152	
9	O8	-998	
10	O9	-845	
11	O10	-691	
12	O11	-537	
13	O12	-384	
14	O13	-230	
15	O14	-76	
16	O15	77	
17	O16	231	
18	O17	384	
19	O18	538	
20	O19	692	
21	O20	845	
22	O21	999	
23	O22	1152	
24	O23	1306	
25	O24	1460	
26	O25	1613	
27	O26	1767	
28	O27	1921	
29	O28	2074	
30	O29	2228	
31	O30	2381	
32	O31	2622	-1346
33	O32	2622	-1186
34	O33	2622	-1029
35	O34	2622	-871
36	O35		-713
37	O36		-554
38	O37		-396
39	O38		-238
40	O39		-79
41	O40		79
42	O41		238
43	O42		396
44	O43		554
45	O44		713
46	O45		871
47	O46		1030
48	O47		1188
49	O48		1346
50	O49	2381	1578
51	O50	2227	
52	O51	2074	
53	O52	1920	
54	O53	1766	
55	O54	1613	
56	O55	1459	
57	O56	1305	
58	O57	1152	
59	O58	998	
60	O59	845	
61	O60	691	
62	O61	538	
63	O62	384	
64	O63	230	
65	O64	77	
66	O65	-77	
67	O66	-230	
68	O67	-384	
69	O68	-538	1578
70	O69	-691	
71	O70	-845	
72	O71	-998	
73	O72	-1152	
74	O73	-1305	
75	O74	-1459	
76	O75	-1613	
77	O76	-1766	
78	O77	-1920	
79	O78	-2074	
80	O79	-2227	
81	EIO2	-2381	
82	D0	-2622	1346
83	D1		1193
84	D2		1039
85	D3		886
86			732
87			578
88			425
89			271
90	V_{DD}		106
91	V_{SS}		-58
92	V0		-223
93	V2		-388
94	V3		-553
95	V5		-718
96	SHL	-2611	-886
97	XSCL		-1039
98	LP		-1193
99	FR		-1346
100	EIO1	-2381	-1578

■LCD PANEL CONNECTION EXAMPLE (SED1606F)

for 200 × 640 DOT MATRIX LCD



*Be sure to connect a current limitter resistor. Also, connect decoupling capacitors (0.01ΩF) near pins V_{SS} and V_5 of each LSI for noise protection.