SED1722/24

T-52-13-07

CMOS LCD DRIVER

- **Large-Capacity LCD Panel**
- **Wide Range of Liquid Crystal Drive Voltage**
- **80 / 100 Output Driver**

■ DESCRIPTION

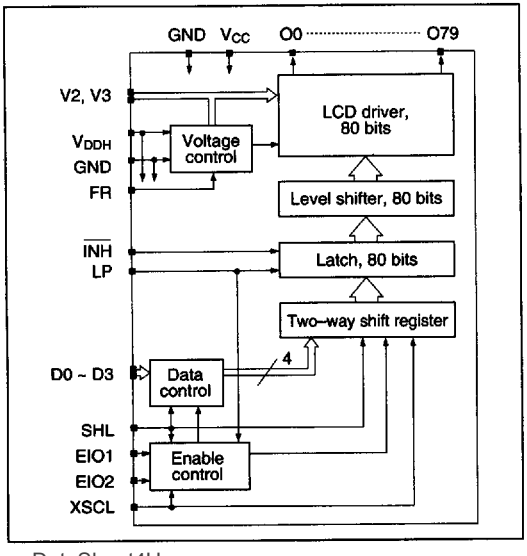
The SED1722 and the SED1724 are 80-output segment (column) driver for driving high-resolution dot-matrix LCD (liquid crystal display). The SED1722 and SED1724 feature a wide range of LCD drive voltages. These drivers use a high speed daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver. The SED1733 is a 100-output common (row) driver, designed for use in conjunction with the SED1722/24 column drivers.

■ FEATURES

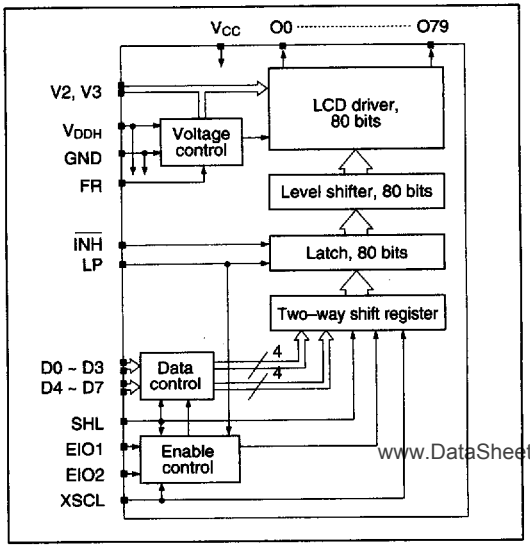
- High voltage silicon gate CMOS process
- Number of output terminals to drive LCD 80
- Display capacity (in combination with SED1733) ..... SED1722: 1120 x 780 dots
  SED1724: 1920 x 960 dots
- A wide range of liquid crystal driving voltage ..... +14V to +40V
- High speed data transfer is possible by 4-bit (SED1722) and 8-bit (SED1724) parallel input.
  Shift clock frequency ..... 12.0MHz (Max.)
- Support zero-bias display disable function
- Support high-speed daisy-chain data transfer which reduce power consumption
- Low output impedance 1kΩ
- The enable automatic transfer facility has realized cascade connection and power reduction. (Enable signals need not be generated by controller.)
- Selectable output shift direction.
- Logic circuit power supply ..... 5.0V±10%
- Packages ..... Aluminum pad: SED1722D0A / SED1724D0A
  QFP5-100pin: SED1722F0A / SED1724F0A

■ BLOCK DIAGRAM

● **SED1722**



● **SED1724**



■ PIN DESCRIPTION

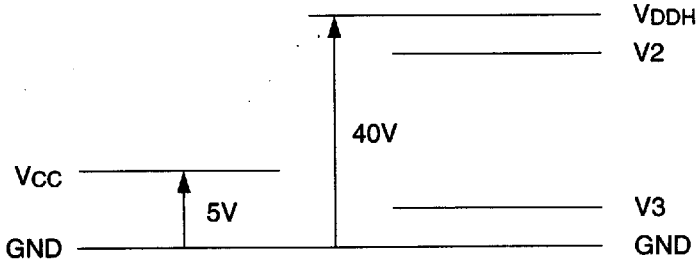
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Q'ty</th></tr>
<tr><td>O0 to 79</td><td>O</td><td>To output the driving segment (column).
The output changes at the LP fall edge.</td><td>80</td></tr>
<tr><td>D0 to D3
(SED1722)</td><td>I</td><td>To input display data.
H: Selection data, L: Non-selection data</td><td>4</td></tr>
<tr><td>D0 to D7
(SED1724)</td><td>I</td><td>To input display data.
H: Selection data, L: Non-selection data</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>To input shift clock for display data (fall edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>To input latch pulse for display data (fall edge trigger)</td><td>1</td></tr>
<tr><td>EI01
EI02</td><td>I/O</td><td>Enable input and output:
Input or output is set on the SHL input level.
Output is reset by an input to LP and falls to "L" automatically when 80-bit data is completely fetched in.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>To select shift direction and to input input-output control data for the EIO terminal.
<In the case of SED1724>
When the data are input to (D0, D1,.. D7) terminals in the order of (a, b, .. g, h), (i,.. o, p) ... (s, t,.. y, z), relations between data and segment outputs come to be as per the following table:
<table>
<tr><td rowspan="2">SHL</td><td colspan="10">O (SEG Output)</td><td colspan="2">EIO</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>.....</td><td>77</td><td>78</td><td>79</td><td>1</td><td>2</td></tr>
<tr><td>H</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>.....</td><td>x</td><td>y</td><td>z</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>.....</td><td>c</td><td>b</td><td>a</td><td>Output</td><td>Input</td></tr>
</table>
Note: The relations between data and segment outputs are set irrespectively to number of shift locks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>To input AC signal for LCD driving output.</td><td>1</td></tr>
<tr><td>Vcc, GND</td><td>Power Supply</td><td>Logic power supply, GND: 0 V, Vcc: +5 V</td><td>2</td></tr>
<tr><td>VDDH</td><td>Power Supply</td><td>Power supply for LCD driving circuit
VDDH: +14 V to 40 V, (Liquid crystal driving selection level)</td><td>1</td></tr>
<tr><td>V2, V3</td><td>Power Supply</td><td>Power supply for driving liquid crystal
VDDH ≥ V2 ≥ 7/9 VDDH, 2/9 VDDH ≥ V3 ≥ GND</td><td>2</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>Forced blank input
Output on the "L" level are forced to non-selection level.</td><td>1</td></tr>
</table>

■ ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{CC}	-0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	-0.3 to +45.0	V
Supply voltage (3)	V2, V3	-0.3 to V_{DDH} +0.3	V
Input voltage	V_I	-0.3 to V_{CC} +0.3	V
Output voltage	V_O	-0.3 to V_{CC} +0.3	V
EIO output current	I_{O1}	20	mA
LCD circuit output current	I_{O2}	20	mA
Operating temperature	T_{opr}	-20 to +75	°C
Storage temperature	T_{stg}	-65 to +150	°C

Note 1. Let the V2 and V3 voltages maintain the condition, $V_{DDH} \geq V2 \geq V3 \geq GND$, all the time.



Note 2. If the logic circuit power supply comes to float power-supply voltage supply voltage is applied to the liquid crystal driving circuit, the LSI may be broken permanently. So, prevent the logic circuit power supply from floating.
Pay special attention to the power supply sequence when the system is switched on or off.

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

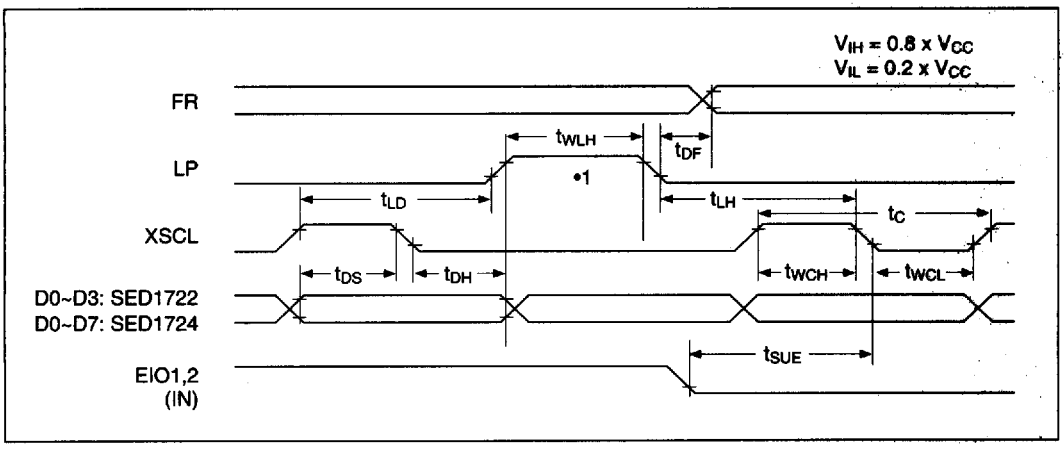
(Unless otherwise specified, GND=0V, V_{CC}= +5.0V±10%, T_a= -20 to 75°C)

Parameter	Symbol	Condition	Terminal	Min	Typ	Max	Unit
Supply voltage (1)	V_{CC}		V_{CC}	4.5	5.0	5.5	V
Recommended supply voltage	V_{DDH}		V_{DDH}	14.0	—	40.0	V
Operable voltage	V_{DDH}	Function	V_{DDH}	8.0	—	—	V
Supply voltage (2)	V2	Recommendation value	V2	7/9V_{DDH}	—	V_{DDH}	V
Supply voltage (3)	V3	Recommendation value	V3	GND	—	2/9V_{DDH}	V
High level input voltage	V_{IH}		EIO1, EIO2, D0 to D3: (SED1722) D0 to D7 (SED1724), XSCL, SHL, FR, LP, INH	0.8V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}			GND	—	0.2V_{CC}	V
High level output voltage	V_{OH}	I_{OH} = -0.6 mA	EIO1, EIO2	V_{CC} -0.4	—	V_{CC}	V
Low level output voltage	V_{OL}	I_{OL} = 0.6 mA		GND	—	0.4	V
Input leak current	I_{LI}	GND ≥ V_{IN} ≥ V_{CC}	D0 to D3: (SED1722) D0 to D7 (SED1724), SHL, XSCL, LP, FR, INH	—	—	2.0	µA
Input-output leak current	$I_{LI/O}$	GND ≥ V_{IN} ≥ V_{CC}	EIO1, EIO2	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = 14.0 to 40.0 V, V_{IH} = V_{CC}, V_{IL} = GND	GND	—	—	25	µA
Output resistance.	R_{SEG}	ΔVON = 0.5V, V_{DDH}=+30.0V	*1 O0 to O79	—	0.7	1.8	kΩ
		ΔVON = 0.5V, V_{DDH}=+20.0V		—	0.8	2.2	kΩ
		ΔVON = 0.5V, V_{DDH}=+14.0V		—	1.0	2.6	kΩ
Current consumed (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} =5.38 MHz, f_{LP} =33.6 kHz, f_{FR} =70 Hz; Input data: To be inverted 1 bit/1H. No load	V_{CC}	—	0.5	1.5	mA
Current consumed (2)	I_{DDH}	V_{CC} = +5.0 V, V3 = +4.0 V, V2 = +26.0 V, V_{DDH} =+30.0V Other conditions are same as those of I_{CC}	V_{DDH}	—	0.2	1.5	mA
Input terminal capacity	C_I	Freq.=1 MHz, T_a = 25°C	D0 to D3: (SED1722) D0 to D7 (SED1724), SHL, XSCL, LP, FR, INH	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

*1 The output resistance is specified within the ranges of the supply voltages (2) and (3).

● AC Electrical Characteristics

○ Input Timing Characteristics

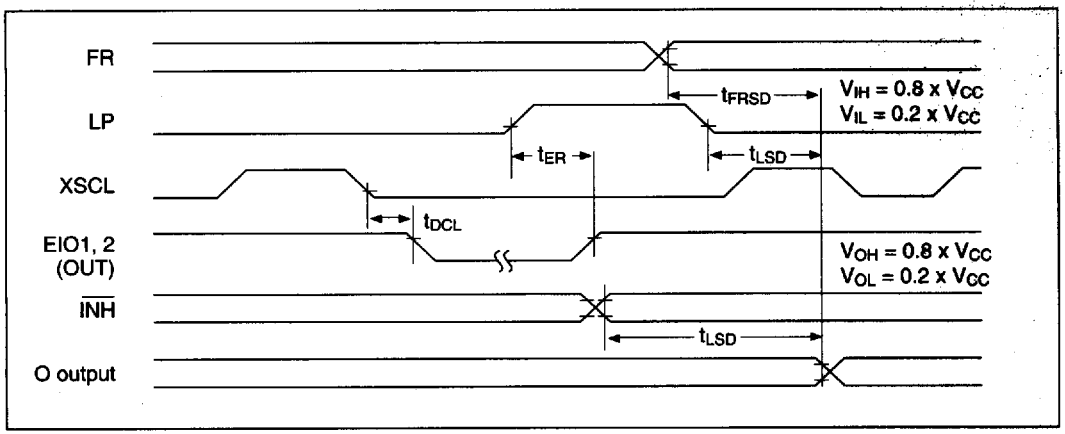


(VCC = 5.0 V ±10%, Ta = -20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
XSCL cycle	tC		83	—	—	ns
XSCL high level pulse width	tWCH		30	—	—	ns
XSCL low level pulse width	tWCL		30	—	—	ns
Data setup time	tDS		30	—	—	ns
Data hold time	tDH		20	—	—	ns
XSCL to LP rise time	tLD		0	—	—	ns
LP to XSCL fall time	tLH		200	—	—	ns
LP high level pulse width	tWLH	see note	70	—	—	ns
FR delay allowable time	tDF		-300	—	300	ns
EIO setup time	tSUE		36	—	—	ns

Note: tWLH is the time when LP is "H" and XSCL is "L"

○ Output Timing Characteristics

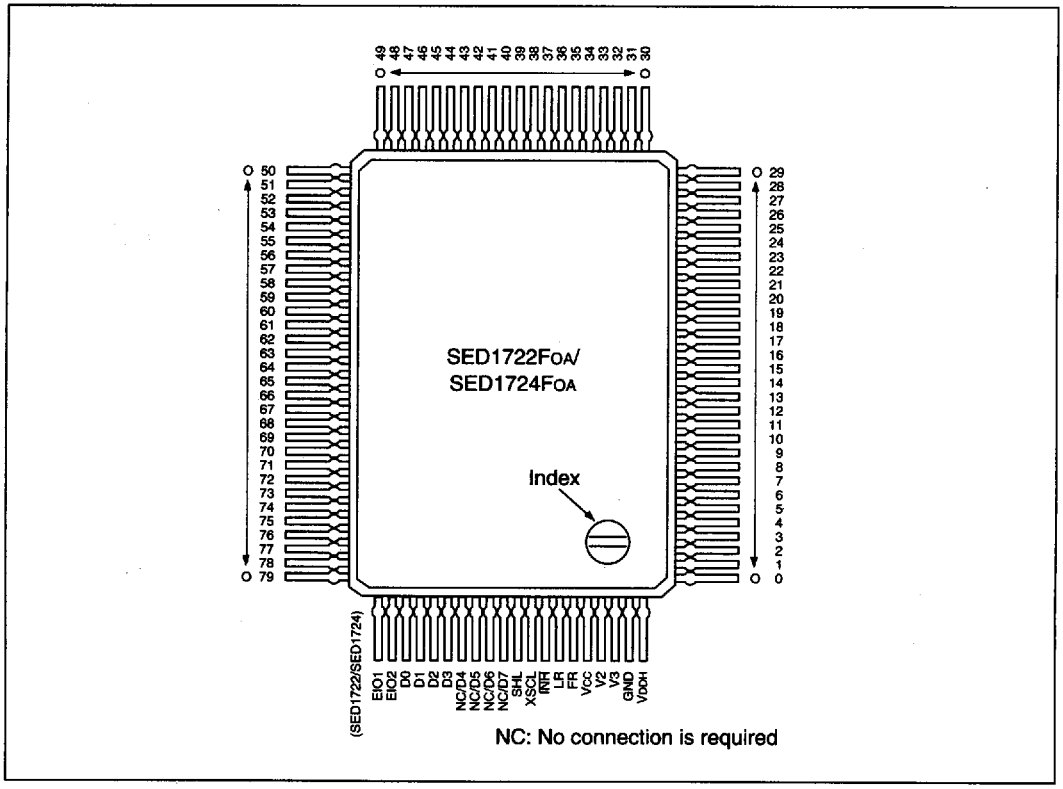


(V_{CC} = +5.0 V ±10%, V_{DDH} = 14.0 to 40.0 V, T_a = -20 to 75°C)

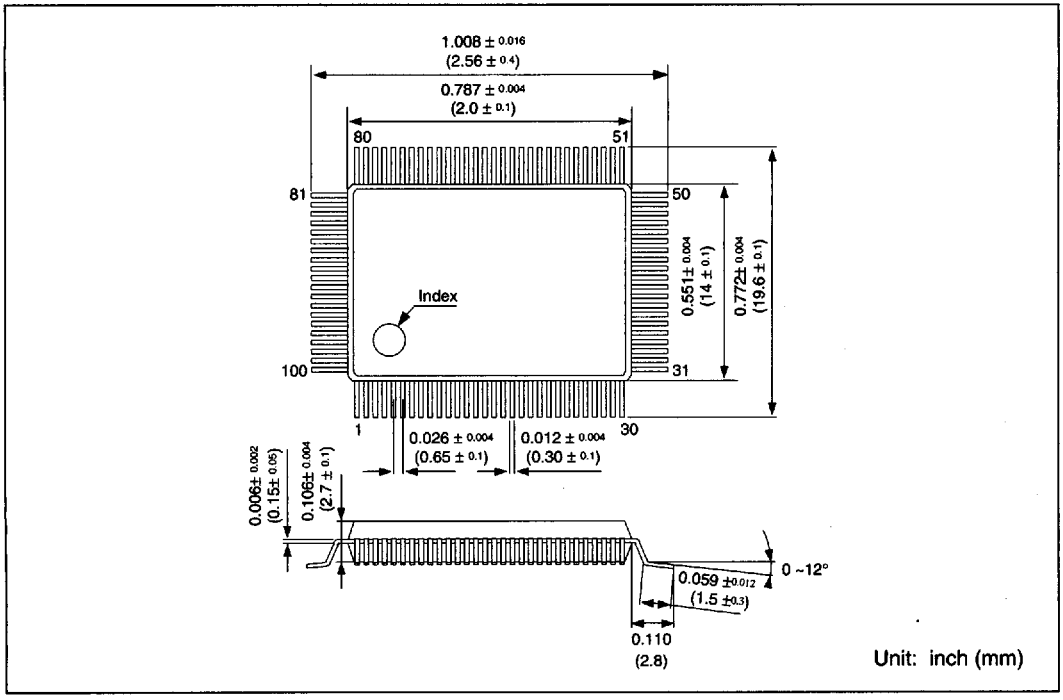
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
EIO reset time	t_{ER}	C_L = 15 pF	—	—	120	ns
EIO output delay time	t_{DCL}		—	—	45	ns
LP to output delay time	t_{LSD}	C_L = 100 pF	—	—	0.5	µs
FR to output delay time	t_{FRSD}		—	—	0.7	µs
$\overline{INH}$ to output delay time	t_{pdINH}		—	—	0.5	µs

■ PACKAGE DIMENSIONS

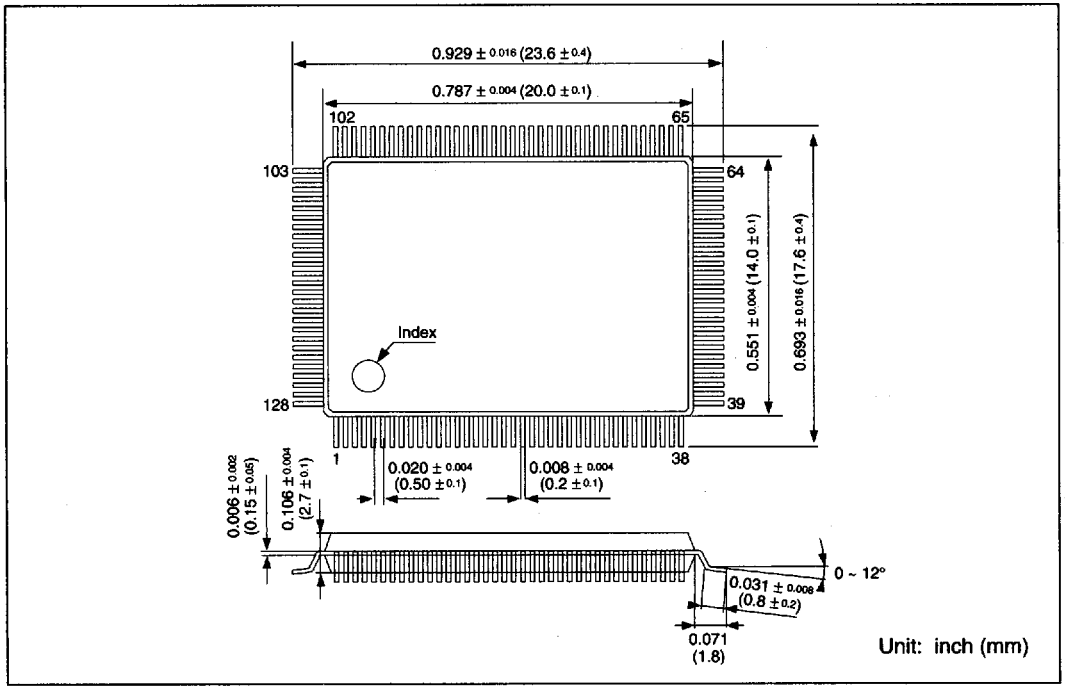
● SED1722F0A, SED1724F0A



● **Plastic QFP5-100pin**

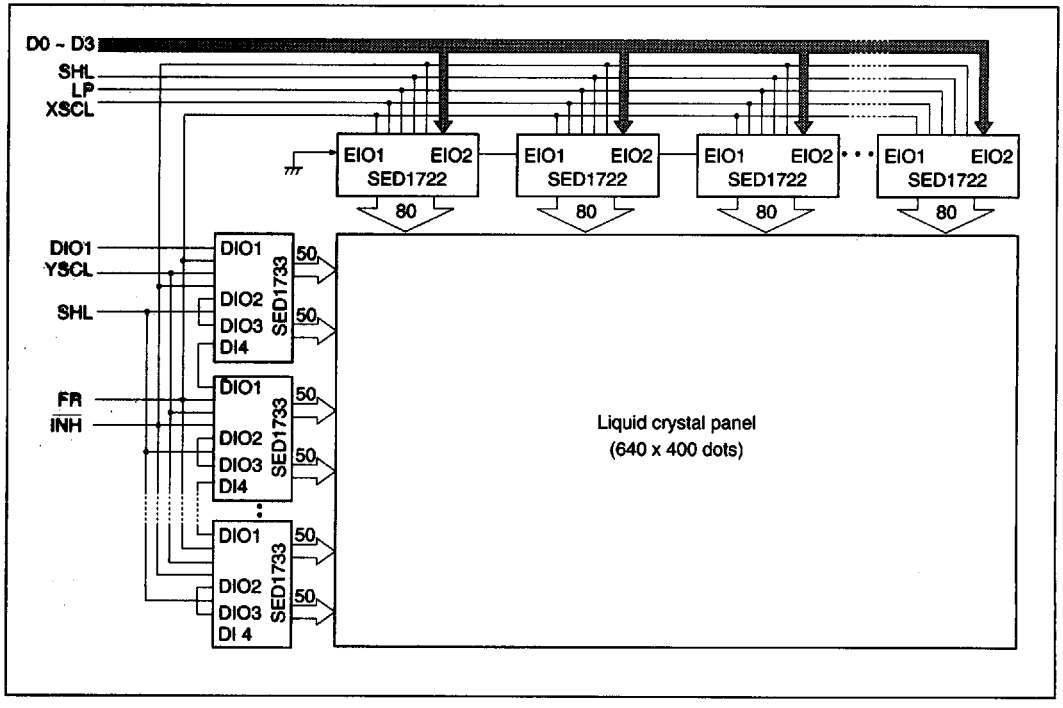


● **Plastic QFP5-128pin-S1**

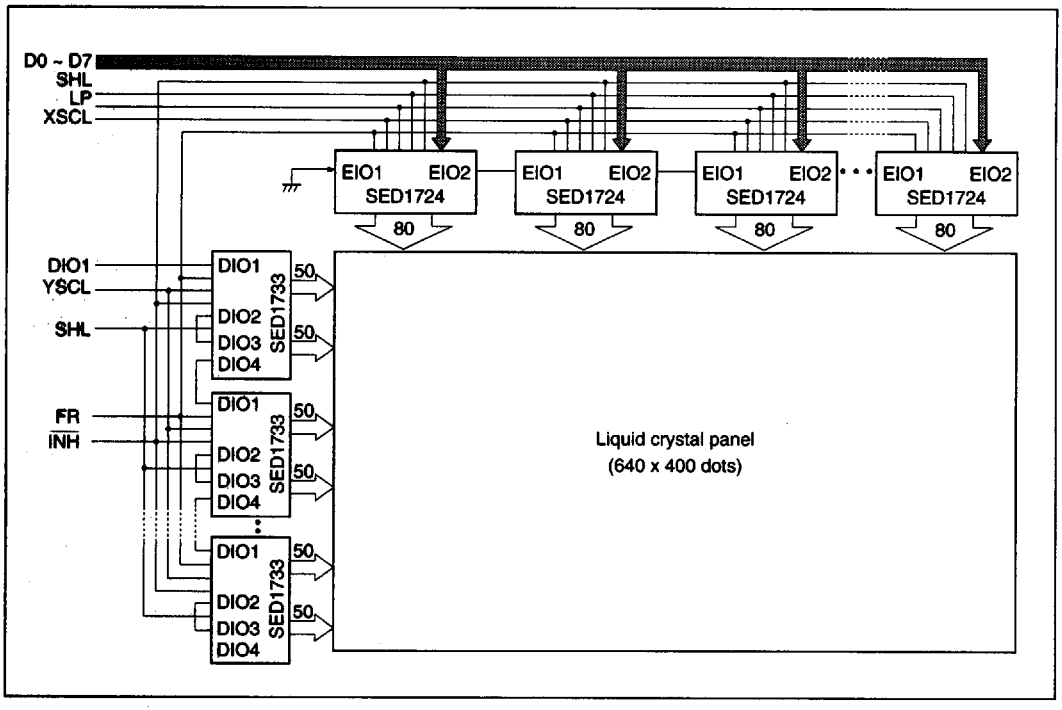


■ EXAMPLE OF REFERENCE CIRCUIT

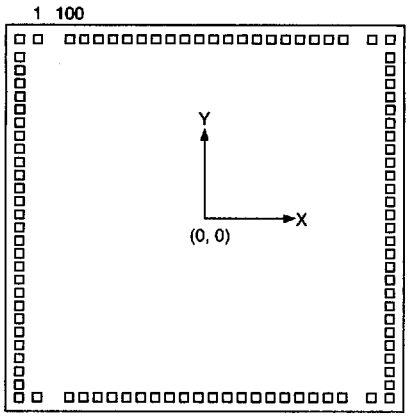
(Combination of SED1722 with SED1733)



(Combination of SED1724 with SED1733)



■ PAD LAYOUT (SED1722D0A, SED1724D0A)



Chip Dimensions	5.81 mm x 5.20 mm
Pad pitch	0.160 mm (Min.)
Chip thickness	0.400 ±0.025 mm
Aluminum pad opening	100 µm x 100 µm (all terminals)

■ PAD COORDINATION

Pad Number	Pad Name	X (µm)	Y (µm)
1	O 50	-2488	2432
2	O 51	-2488	2432
3	O 52	-2738	2222
4	O 53	-2738	2022
5	O 54	-2738	1835
6	O 55	-2738	1660
7	O 56	-2738	1485
8	O 57	-2738	1310
9	O 58	-2738	1135
10	O 59	-2738	960
11	O 60	-2738	785
12	O 61	-2738	610
13	O 62	-2738	435
14	O 63	-2738	260
15	O 64	-2738	85
16	O 65	-2738	-85
17	O 66	-2738	-260
18	O 67	-2738	-435
19	O 68	-2738	-610
20	O 69	-2738	-785
21	O 70	-2738	-960
22	O 71	-2738	-1135
23	O 72	-2738	-1310
24	O 73	-2738	-1485
25	O 74	-2738	-1660
26	O 75	-2738	-1835
27	O 76	-2738	-2022
28	O 77	-2738	-2222
29	O 78	-2738	-2432
30	O 79	-2488	-2432
31	EIO2	-2000	-2432
32	EIO1	-1750	-2432
33	D0	-1500	-2432
34	D1	-1300	-2432
35	D2	-1100	-2432
36	D3	-900	-2432
37	NC/D4	-700	-2432
38	NC/D5	-500	-2432
39	NC/D6	-300	-2432
40	NC/D7	-100	-2432
41	SHL	100	-2432
42	XSCL	300	-2432
43	$\overline{INH}$	500	-2432
44	LP	700	-2432
45	FR	900	-2432
46	VCC	1100	-2432
47	V2	1300	-2432
48	V3	1500	-2432
49	GND	1750	-2432
50	VDDH	2000	-2432
51	O 0	2488	-2432
52	O 1	2738	-2432
53	O 2	2738	-2222
54	O 3	2738	-2022
55	O 4	2738	-1835
56	O 5	2738	-1660
57	O 6	2738	-1485
58	O 7	2738	-1310
59	O 8	2738	-1135
60	O 9	2738	-960
61	O 10	2738	-785
62	O 11	2738	-610
63	O 12	2738	-435
64	O 13	2738	-260
65	O 14	2738	-85
66	O 15	2738	85
67	O 16	2738	260
68	O 17	2738	435
69	O 18	2738	610
70	O 19	2738	785
71	O 20	2738	960
72	O 21	2738	1135
73	O 22	2738	1310
74	O 23	2738	1485
75	O 24	2738	1660
76	O 25	2738	1835
77	O 26	2738	2022
78	O 27	2738	2222
79	O 28	2738	2432
80	O 29	2488	2432
81	O 30	2000	2432
82	O 31	1750	2432
83	O 32	1500	2432
84	O 33	1300	2432
85	O 34	1100	2432
86	O 35	900	2432
87	O 36	700	2432
88	O 37	500	2432
89	O 38	300	2432
90	O 39	100	2432
91	O 40	-100	2432
92	O 41	-300	2432
93	O 42	-500	2432
94	O 43	-700	2432
95	O 44	-900	2432
96	O 45	-1100	2432
97	O 46	-1300	2432
98	O 47	-1500	2432
99	O 48	-1750	2432
100	O 49	-2000	2432