**SEFM8N18**
**SEFMN820**
**SEFP8N18**
**SEFP8N20**

# N-CHANNEL POWER MOS TRANSISTORS

## HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

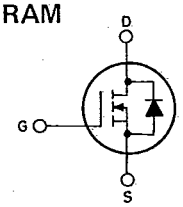
| $V_{DSS}$ | $R_{DS\ (ON)}$ | $I_D$ |
|---|---|---|
| 180V/200V | 0.4 Ω | 8 A |

## ABSOLUTE MAXIMUM RATINGS

| | | SEFM or SEFP 8N18 | SEFM or SEFP 8N20 |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 180V | 200V |
| $V_{DGR}$ | Drain-gate voltage ($R_{GS}$ = 20KΩ) | 180V | 200V |
| $V_{GS}$ | Gate-source voltage | ±20V | |
| $I_D$ | Drain current (continuous) $T_{case}$ = 25°C | 8A | |
| $I_{DM}$(•) | Drain current (pulsed) | 25A | |
| $I_{GM}$ | Gate current (pulsed) | 1.5A | |
| $P_{tot}$ | Total power dissipation at $T_{case}$ = 25°C | 75W | |
| | Derating factor | 0.6W/°C | |
| $T_{stg}$ | Storage temperature | -65 to 150°C | |
| $T_j$ | Max. operating junction temperature | 150°C | |

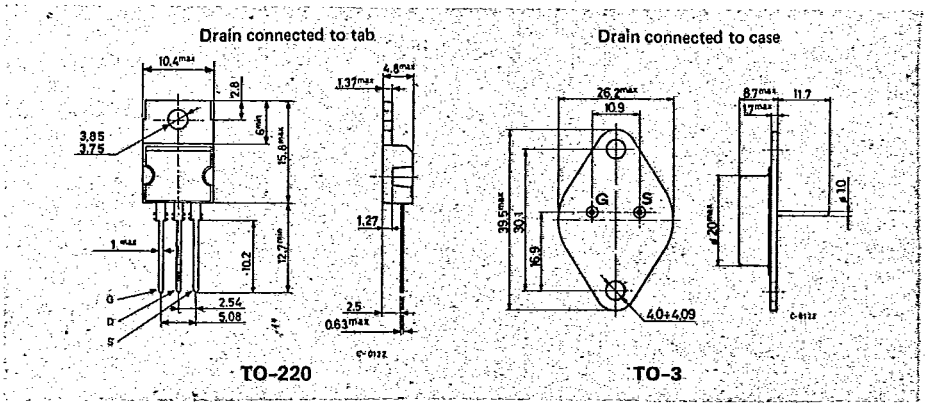
(•) Pulse width limited by safe operating area

## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm



## THERMAL DATA

| | | | |
|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max. | 1.67°C/W |
| $T_L$ | Maximum lead temperature for soldering purpose | | 275°C |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **OFF** | | | | | | |
| $V_{(BR)\ DSS}$ | Drain-source breakdown voltage | $I_D$ = 5 mA $V_{GS}$ = 0<br>for SEFM8N18/SEFP8N18<br>for SEFM8N20/SEFP8N20 | <br>180<br>200 | | | <br>V<br>V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 0.85 Rated $V_{DSS}$<br>$T_j$ = 100°C | | | 250<br>2.5 | µA<br>mA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±20 V | | | 500 | nA |
| **ON*** | | | | | | |
| $V_{GS\ (th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$ $I_D$ = 1 m A<br>$T_j$ = 100°C | 2<br>1.5 | | 4.5<br>4.0 | V<br>V |
| $R_{DS\ (on)}$ | Static drain-source on resistance | $V_{GS}$ = 10V $I_D$ = 4 A | | 0.27 | 0.4 | Ω |
| $V_{DS\ (on)}$ | Drain-source On voltage | $V_{GS}$ = 10V $I_D$ = 8 A<br>$V_{GS}$ = 10V $I_D$ = 4 A<br>$T_j$ = 100°C | | | 4<br>3.2 | V<br>V |
| $g_{fs}$ | Forward transconductance | $V_{DS}$ = 15V $I_D$ = 4 A | 3 | | | mho |
| **DYNAMIC** | | | | | | |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ = 25 V f = 1 MHz<br>$V_{GS}$ = 0 | | 980<br>200<br>80 | 1200<br>260<br>100 | pF<br>pF<br>pF |

## ELECTRICAL CHARACTERISTICS (continued)

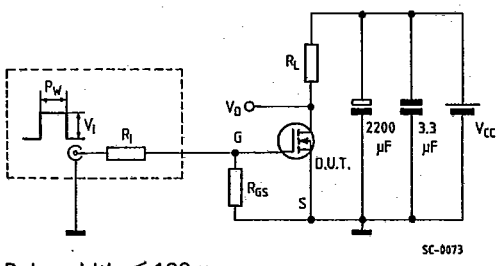
| Parameter | | Test conditions | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|---|
| **SWITCHING** | | | | | | |
| $t_{d\ (on)}$ | Turn-on delay time | $V_{CC}$ = 25 V | | 40 | | ns |
| $t_r$ | Rise time | $I_D$ = 0.5 Rated $I_D$ | | 150 | | ns |
| $t_{d\ (off)}$ | Turn-off delay time | $R_{GS}$ = 50 Ω $R_i$ = 50 Ω | | 100 | | ns |
| $t_f$ | Fall time | (see test circuit) | | 100 | | ns |
| **SOURCE DRAIN DIODE** | | | | | | |
| $V_{SD}$ | Forward on voltage | $I_{SD}$ = Rated $I_D$ $V_{GS}$ = 0 | | 2.0 | | V |
| $t_{on}$ | Forward Turn-on time | | | 250 | | ns |
| $t_{rr}$ | Reverse recovery time | | | 325 | | ns |

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

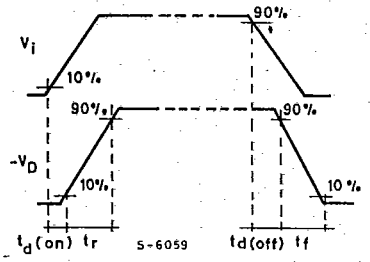
**For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP363 Datasheet.**

## SWITCHING TIMES RESISTIVE LOAD

**Test circuit**




**Waveforms**




Pulse width ≤ 100 μs
Duty cycle ≤ 2%
$V_i$ = 10V