

4GB DDR2 – SDRAM registered DIMM

240 Pin RDIMM

SEP04G72G1AH2MT-xxR

4GByte in FBGA Technology

RoHS compliant

Options:

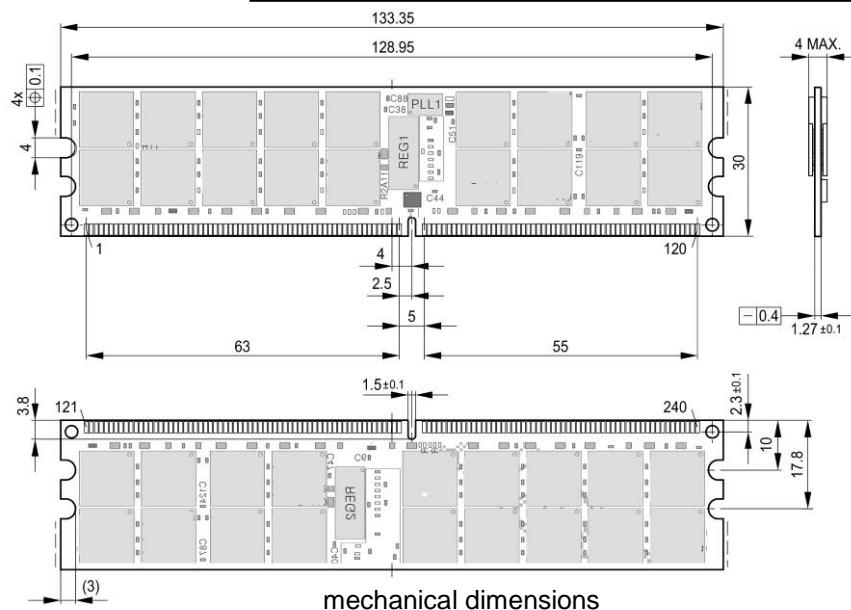
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|---------------------------------|-------------------|-------------|
| ▪ Data Rate / Latency | | Marking |
| DDR2 667 MT/s CL5 | | -30 |
| DDR2 800 MT/s CL6 | | -25 |
| ▪ Module Density | | |
| 4GByte with 36 dies and 2 ranks | | |
| ▪ Standard Grade | (T _C) | 0°C to 85°C |
| | (T _A) | 0°C to 70°C |

Environmental Requirements:

- Operating temperature (T_C)
Standard Grade 0°C to 85°C
- Operating Humidity
10% to 90% relative humidity, noncondensing
- Operating Pressure
105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
-55°C to 100°C
- Storage Humidity
5% to 95% relative humidity, noncondensing
- Storage Pressure
1682 PSI (up to 5000 ft.) at 50°C

Features:

- 240-pin 72-bit Dual-In-Line Double Data Rate Synchronous DRAM Module for server applications
- Module organization: dual rank 512M x 64
- V_{DD} = 1.8V ±0.1V, V_{DDQ} 1.8V ±0.1V
- 1.8V I/O (SSTL_18 compatible)
- Auto Refresh (CBR) and Self Refresh 8k Refresh every 64ms
- Serial Presence Detect with EEPROM
- Gold-contact pad
- This module is fully pin and functional compatible to the JEDEC PC2-6400 spec. and JEDEC- Standard MO-237. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]
- **DDR2 - SDRAM component MICRON MT47H256M4CF-25 DIE-Revision H**
- 256Mx4 DDR2 SDRAM in FBGA-60 package
- Four bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Eight internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency – 1 t_{CK}
- Programmable burst length: 4 or 8
- Adjustable data-output drive strength
- On-die termination (ODT)



This Swissbit module is an industry standard 240-pin 8-byte DDR2 SDRAM Dual-In-line Memory Module (DIMM) which is organized as x72 high speed CMOS memory arrays. The module uses internally configured quad-bank DDR2 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR2 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR2 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR2 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving "power-down" mode. All inputs and all full drive-strength outputs are SSTL_18 compatible.

The DDR2 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I²C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the DIMM manufacturer (swissbit) to identify the module type, the module's organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR2 SDRAMs used	Row Addr.	Device Bank Select	Column Addr.	Refresh	Module Bank Select
512M x 72bit	36 x 256M x 4bit (1Gbit)	14	BA0, BA1, BA2	11	8k	S0#, S1#

Module Dimensions

in mm

133.33 (long) x 30(high) x 4 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SEP04G72G1AH2MT-30R	4GByte	5.3 GB/s	3.0ns/667MT/s	5-5-5
SEP04G72G1AH2MT-25R	4GByte	6.4 GB/s	2.5ns/800MT/s	6-6-6

Pin Name

A0 – A13	Address Inputs
BA0, BA1, BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
CB0 – CB7	Check Bits
DM0 – DM8	Input Data Mask
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 – CKE1	Clock Enable
CK0 – CK1	Clock Input, positive line
CK0# – CK1#	Clock Input, negative line
DQS0 – DQS17	Data Strobe, positive line
DQS0# – DQS17#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
S0# – S1#	Chip Select

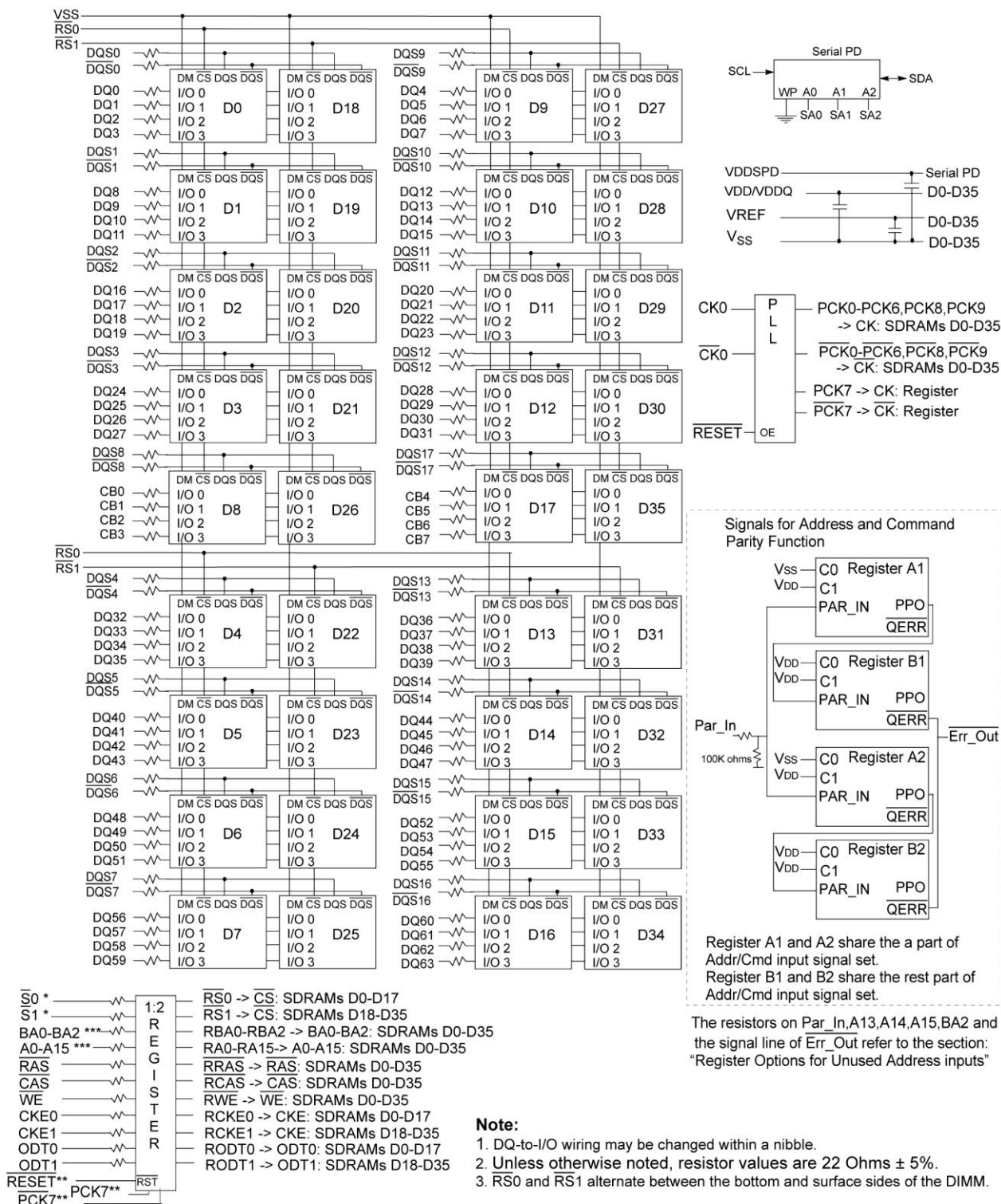
Reset#	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQs are High-Z.
PAR_IN	Parity bit for the address and control bus.
ERR_OUT	Parity error found on the address and control bus.
V _{DD} / V _{DDQ}	Supply Voltage (1.8V± 0.1V)
V _{REF}	Input / Output Reference
V _{SS}	Ground
V _{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0, ODT1	On-Die Termination
NC	No Connection

Pin Configuration

PIN #	Front Side	PIN #	Front Side	PIN #	Back Side	PIN #	Back Side
1	V _{REF}	61	A4	121	V _{SS}	181	V _{DDQ}
2	V _{SS}	62	V _{DDQ}	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	V _{DD}	124	V _{SS}	184	V _{DD}
5	V _{SS}	65	V _{SS}	125	DM0 DQS9	185	CK0
6	DQS0#	66	V _{SS}	126	NC DQS9#	186	CK0#
7	DQS0	67	V _{DD}	127	V _{SS}	187	V _{DD}
8	V _{SS}	68	NC PAR_IN	128	DQ6	188	A0
9	DQ2	69	V _{DD}	129	DQ7	189	V _{DD}
10	DQ3	70	A10	130	V _{SS}	190	BA1
11	V _{SS}	71	BA0	131	DQ12	191	V _{DDQ}
12	DQ8	72	V _{DDQ}	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	V _{SS}	193	CS0#
14	V _{SS}	74	CAS#	134	DM1 DQS10	194	V _{DDQ}
15	DQS1#	75	V _{DDQ}	135	NC DQS10#	195	ODT0
16	DQS1	76	CS1#	136	V _{SS}	196	A13
17	V _{SS}	77	ODT1	137	NC	197	V _{DD}
18	RESET#	78	V _{DDQ}	138	NC	198	V _{SS}
19	NC	79	V _{SS}	139	V _{SS}	199	DQ36
20	V _{SS}	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	V _{SS}
22	DQ11	82	V _{SS}	142	V _{SS}	202	DM4 DQS13
23	V _{SS}	83	DQS4#	143	DQ20	203	NC DQS13#
24	DQ16	84	DQS4	144	DQ21	204	V _{SS}
25	DQ17	85	V _{SS}	145	V _{SS}	205	DQ38
26	V _{SS}	86	DQ34	146	DM2 DQS11	206	DQ39
27	DQS2#	87	DQ35	147	NC DQS11#	207	V _{SS}
28	DQS2	88	V _{SS}	148	V _{SS}	208	DQ44
29	V _{SS}	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	V _{SS}

PIN #	Front Side	PIN #	Front Side	PIN #	Back Side	PIN #	Back Side
31	DQ19	91	V _{SS}	151	V _{SS}	211	DM5 DQS14
32	V _{SS}	92	DQS5#	152	DQ28	212	NC DQS14#
33	DQ24	93	DQS5	153	DQ29	213	V _{SS}
34	DQ25	94	V _{SS}	154	V _{SS}	214	DQ46
35	V _{SS}	95	DQ42	155	DM3 DQS12	215	DQ47
36	DQS3#	96	DQ43	156	NC DQS12#	216	V _{SS}
37	DQS3	97	V _{SS}	157	V _{SS}	217	DQ52
38	V _{SS}	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	V _{SS}
40	DQ27	100	V _{SS}	160	V _{SS}	220	NC
41	V _{SS}	101	SA2	161	CB4	221	NC
42	CB0	102	NC	162	CB5	222	V _{SS}
43	CB1	103	V _{SS}	163	V _{SS}	223	DM6 DQS15
44	V _{SS}	104	DQS6#	164	DM8 DQS17	224	NC DQS15#
45	DQS8#	105	DQS6	165	NC DQS17#	225	V _{SS}
46	DQS8	106	V _{SS}	166	V _{SS}	226	DQ54
47	V _{SS}	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	V _{SS}
49	CB3	109	V _{SS}	169	V _{SS}	229	DQ60
50	V _{SS}	110	DQ56	170	V _{DD}	230	DQ61
51	V _{DD}	111	DQ57	171	CKE1	231	V _{SS}
52	CKE0	112	V _{SS}	172	V _{DD}	232	DM7 DQS16
53	V _{DD}	113	DQS7#	173	NC	233	NC DQS16#
54	BA2	114	DQS7	174	NC	234	V _{SS}
55	NC ERR_OUT	115	V _{SS}	175	V _{DD}	235	DQ62
56	V _{DDQ}	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	V _{SS}
58	A7	118	V _{SS}	178	V _{DD}	238	V _{DDSPD}
59	V _{DD}	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

**FUNCTIONAL BLOCK DIAGRAM 4096MB DDR2 ECC Registered DIMM,
2 RANKS AND 36 COMPONENTS**



* S0 connects to DCS and S1 connects to CSR on a pair of Registers. S1 connects to DCS and S0 connects to CSR on another pair of Registers.
 ** RESET, PCK7 and PCK7 connect to all Registers. Other signals connect to one pair of four Registers.
 *** A13-15, BA2 have the optional pull down resistors(100K ohms), which is not indicated here.

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
V_{DD} Supply Voltage relative to V_{SS}	V_{DD}	-1.0	2.3	V
I/O V_{DD} Supply Voltage relative to V_{SS}	V_{DDQ}	-0.5	2.3	V
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	2.3	V
INPUT LEAKAGE CURRENT Any input $0V \leq V_{IN} \leq V_{DD}$, V_{REF} pin $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = $0V$)	I_I			μA
Command/Address RAS#, CAS#, WE#, S#, CKE		-64	64	
CK, CK#		-32	32	
DM		-2	2	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$)	I_{OZ}	-5	5	μA
DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level	I_{VREF}	-16	16	μA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V
I/O Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V
I/O Termination Voltage (system)	V_{TT}	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.125$		$V_{DDQ} + 0.3$	V
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.125$	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.25$	-	V
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.25$	V

CAPACITANCE

At DDR2 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

 (0°C ≤ T_{CASE} ≤ +85°C ; V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

Parameter & Test Condition	Symbol	max.		Unit	
		6400-CL6	5300-CL5		
OPERATING CURRENT *) : One device bank Active-Precharge; t _{RC} = t _{RC} (I _{DD}); t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	1296	1206	mA	
OPERATING CURRENT :*) One device bank; Active-Read-Precharge; I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RAS} = t _{RAS} MIN (I _{DD}), t _{RCD} = t _{RCD} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I _{DD4W}	I _{DD1}	1476	1386	mA	
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t _{CK} = t _{CK} (I _{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	I _{DD2P}	252	252	mA	
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	I _{DD2Q}	864	864	mA	
PRECHARGE STANDBY CURRENT: All device banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD2N}	1008	864	mA	
ACTIVE POWER-DOWN CURRENT: All device banks open; t _{CK} = t _{CK} (I _{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	I _{DD3P}	Fast PDN Exit MR[12] = 0	720	540	mA
		Slow PDN Exit MR[12] = 1	360	360	
ACTIVE STANDBY CURRENT: All device banks open; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD3N}	1188	1080	mA	
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD4R}	2286	2106	mA	

Parameter & Test Condition	Symbol	max.		Unit
		6400-CL6	5300-CL5	
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD4W}	2376	2196	mA
BURST REFRESH CURRENT: t _{CK} = t _{CK} (I _{DD}); refresh command at every t _{RFC} (I _{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD5}	2736	2646	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE ≤ 0.2V; All other Control and Address bus inputs are floating at V _{REF} ; DQ's are floating at V _{REF}	I _{DD6}	252	252	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = t _{RCD} (I _{DD}) - 1 x t _{CK} (I _{DD}); t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RRD} = t _{RRD} (I _{DD}), t _{RCD} = t _{RCD} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I _{DD7}	3906	3456	mA

*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I _{DD} MEASUREMENT CONDITIONS			
SYMBOL	6400-CL6	5300-CL5	Unit
CL (I _{DD})	6	5	t _{CK}
t _{RCD} (I _{DD})	15	15	ns
t _{RC} (I _{DD})	60	60	ns
t _{RRD} (I _{DD})	7.5	7.5	ns
t _{CK} (I _{DD})	2.5	3.0	ns
t _{RAS} MIN (I _{DD})	45	45	ns
t _{RAS} MAX (I _{DD})	70'000	70'000	ns
t _{RP} (I _{DD})	15	15	ns
t _{RFC} (I _{DD})	127.5	127.5	ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (0°C ≤ T_{CASE} ≤ + 85°C ; V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS		6400-CL6		5300-CL5		Unit	
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
Clock cycle time	CL = 6	t _{CK} (6)	2.5	8.0	-	-	ns
	CL = 5	t _{CK} (5)	3.0	8.0	3.0	8.0	
	CL = 4	t _{CK} (4)	3.75	8.0	3.75	8.0	
	CL = 3	t _{CK} (3)	-	-	5.0	8.0	
CK high-level width	t _{CH}	0.48	0.52	0.45	0.55	t _{CK}	
CK low-level width	t _{CL}	0.48	0.52	0.45	0.55	t _{CK}	
Half clock period	t _{HP}	min (t _{CH} , t _{CL})	-	min (t _{CH} , t _{CL})	-	ps	
Access window (output) of DQ _s from CK/CK#	t _{AC}	-0.40	+0.40	-0.45	+0.45	ns	
Data-out high-impedance window from CK/CK#	t _{HZ}	-	t _{AC} max	-	+0.45 (= t _{AC} max)	ns	
Data-out low-impedance window from CK/CK#	t _{LZ}	t _{AC} min	t _{AC} max	-0.45 (= t _{AC} min)	+0.45 (= t _{AC} max)	ns	
DQ and DM input setup time relative to DQS	t _{DSa}	0.05	-	0.10	-	ns	
DQ and DM input hold time relative to DQS	t _{DHa}	0.125	-	0.30	-	ns	
DQ and DM input pulse width (for each input)	t _{DIPW}	0.35	-	0.35	-	t _{CK}	
Data hold skew factor	t _{QHS}	-	0.3		0.34	ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t _{QH}	t _{HP} - t _{QHS}	-	t _{HP} - t _{QHS}	-	ns	
Data valid output window	t _{DVW}	t _{QH} - t _{DQSQ}	-	t _{QH} - t _{DQSQ}	-	ns	
DQS input high pulse width	t _{DQSH}	0.35	-	0.35	-	t _{CK}	
DQS input low pulse width	t _{DQSL}	0.35	-	0.35	-	t _{CK}	
DQS -DQ skew, DQS to last DQ valid, per group, per access	t _{DQSQ}	-	0.2	-	0.24	ns	
DQS read preamble	t _{RPRE}	0.9	1.1	0.9	1.1	t _{CK}	
DQS read postamble	t _{RPST}	0.4	0.6	0.4	0.6	t _{CK}	
DQS write preamble	t _{WPRE}	0.35	-	0.35	-	t _{CK}	
DQS write preamble setup time	t _{WPRES}	0	-	0	-	ns	
DQS write postamble	t _{WPST}	0.4	0.6	0.4	0.6	t _{CK}	
Positive DQS latching edge to associated clock edge	t _{DQSS}	- 0.25	+ 0.25	- 0.25	+ 0.25	t _{CK}	
Write command to first DQS latching transition		WL- t _{DQSS}	WL+ t _{DQSS}	WL- t _{DQSS}	WL+ t _{DQSS}	t _{CK}	
Address and control input pulse width (for each input)	t _{IPW}	0.6	-	0.6	-	t _{CK}	
Address and control input setup time	t _{ISa}	0.175	-	0.4	-	ns	

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.8\text{V} \pm 0.1\text{V}, V_{\text{DD}} = +1.8\text{V} \pm 0.1\text{V})$

AC CHARACTERISTICS		6400-CL6		5300-CL5		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
Address and control input hold time	t_{IH}	0.25	-	0.4	-	ns
CAS# to CAS# command delay	t_{CCD}	2	-	2	-	t_{CK}
ACTIVE to ACTIVE (same bank) command period	t_{RC}	60	-	60	-	ns
ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command	t_{RRD}	7.5	-	7.5	-	ns
ACTIVE to READ or WRITE delay	t_{RCD}	15	-	15	-	ns
Four bank Activate period	t_{FAW}	37.5	-	37.5	-	ns
ACTIVE to PRECHARGE command	t_{RAS}	45	70'000	40	70'000	ns
Internal READ to precharge command delay	t_{RTP}	7.5	-	7.5	-	ns
Write recovery time	t_{WR}	15	-	15	-	ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{\text{WR}} + t_{\text{RP}}$	-	$t_{\text{WR}} + t_{\text{RP}}$	-	ns
Internal WRITE to READ command delay	t_{WTR}	7.5	-	7.5	-	ns
PRECHARGE command period	t_{RP}	15	-	15	-	ns
PRECHARGE ALL command period	t_{RPA}	$t_{\text{RP}} + t_{\text{CK}}$	-	$t_{\text{RP}} + t_{\text{CK}}$	-	ns
LOAD MODE command cycle time	t_{MRD}	2	-	2	-	t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{\text{IS}} + t_{\text{CK}} + t_{\text{IH}}$		$t_{\text{IS}} + t_{\text{CK}} + t_{\text{IH}}$		
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t_{RFC}	127.5	70'000	127.5	70'000	ns
Average periodic refresh interval ($0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$)	t_{REFI}	-	7.8	-	7.8	μs
($85^{\circ}\text{C} \leq T_{\text{CASE}} \leq 95^{\circ}\text{C}$)	$t_{\text{REFI(IT)}}$	-	3.9	-	3.9	
Exit SELF REFRESH to non-READ command	t_{XSNR}	$t_{\text{RFC}}(\text{min}) + 10$	-	$t_{\text{RFC}}(\text{min}) + 10$	-	ns
Exit SELF REFRESH to READ command	t_{XSRD}	200	-	200	-	t_{CK}
Exit SELF REFRESH timing reference	t_{ISXR}	t_{IS}	-	t_{IS}	-	ps
ODT turn-on delay	t_{AOND}	2	2	2	2	t_{CK}
ODT turn-on	t_{AON}	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 1,000$	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 600$	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 600$	ps
ODT turn-on (power-down mode)	t_{AONPD}	$t_{\text{AC}}(\text{min}) + 2,000$	$2 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min}) + 2,000$	$2 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	ps
ODT turn-off (power-down mode)	t_{AOFPD}	$t_{\text{AC}}(\text{min}) + 2,000$	$2.5 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min}) + 2,000$	$2.5 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	ps
ODT to power-down entry latency	t_{ANPD}	3	-	3	-	t_{CK}

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.8\text{V} \pm 0.1\text{V}, V_{\text{DD}} = +1.8\text{V} \pm 0.1\text{V})$

AC CHARACTERISTICS		6400-CL6		5300-CL5		Unit
Parameter	Symbol	MIN	MAX	MIN	MAX	
ODT power-down exit latency	t_{AXPD}	8	-	8	-	t_{CK}
ODT enable from MRS command	T_{MOD}	12	-	12	-	ns
Exit active power-down to READ command, MR [bit 12 = 0]	t_{XARD}	2	-	2	-	t_{CK}
Exit active power-down to READ command, MR [bit 12 = 1]	t_{XARDS}	8 – AL	-	7 – AL	-	t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2	-	2	-	t_{CK}
CKE minimum high/low time	t_{CKE}	3	-	3	-	t_{CK}

Register Specifications

Parameter	Symbol	Pins	Conditions	Min	Max	Units
DC high-level input voltage	$V_{\text{IH(DC)}}$	Address, control, command	SSTL_18	$V_{\text{REF(DC)}} + 125$	$V_{\text{DDQ}} + 250$	mV
DC low-level input voltage	$V_{\text{IL(DC)}}$	Address, control, command	SSTL_18	0	$V_{\text{REF(DC)}} - 125$	mV
AC high-level input voltage	$V_{\text{IH(AC)}}$	Address, control, command	SSTL_18	$V_{\text{REF(DC)}} + 250$	V_{DD}	mV
AC low-level input voltage	$V_{\text{IL(AC)}}$	Address, control, command	SSTL_18	0	$V_{\text{REF(DC)}} - 250$	mV
Output high voltage	V_{OH}	Parity output	LVC MOS	1.2	-	V
Output low voltage	V_{OL}	Parity output	LVC MOS	-	0.5	V
Input current	I_{I}	All pins	$V_{\text{I}} = V_{\text{DDQ}}$ or V_{SSQ}	-5	+5	μA
Static standby	I_{DD}	All pins	$\text{RESET}\# = V_{\text{SSQ}}$ ($I_{\text{O}} = 0$)	-	100	μA
Static operating	I_{DD}	All pins	$\text{RESET}\# = V_{\text{SSQ}}$; $V_{\text{I}} = V_{\text{IH(AC)}}$ or $V_{\text{IL(DC)}}$ $I_{\text{O}} = 0$	-	40	mA
Dynamic operating (clock tree)	I_{DDD}	n/a	$\text{RESET}\# = V_{\text{DD}}$, $V_{\text{I}} = V_{\text{IH(AC)}}$ or $V_{\text{IL(AC)}}$, $I_{\text{O}} = 0$; CK and CK# switching 50% duty cycle	-	Varies by manufacturer	μA
Dynamic operating (per each input)	I_{DDD}	n/a	$\text{RESET}\# = V_{\text{DD}}$, $V_{\text{I}} = V_{\text{IH(AC)}}$ or $V_{\text{IL(AC)}}$, $I_{\text{O}} = 0$; CK and CK# switching 50% duty cycle; One data input switching at $t_{\text{CK}}/2$, 50% duty cycle	-	Varies by manufacturer	μA
Input capacitance (per device, per pin)	C_{I}	Data	$V_{\text{I}} = V_{\text{REF}} \pm 250\text{mV}$; $V_{\text{DDQ}} = 1.8\text{V}$	2.5	3.5	pF
Input capacitance (per device, per pin)	C_{I}	RESET#	$V_{\text{I}} = V_{\text{DDQ}}$ or V_{SSQ}	-	Varies by manufacturer	pF

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC standard JESD82.

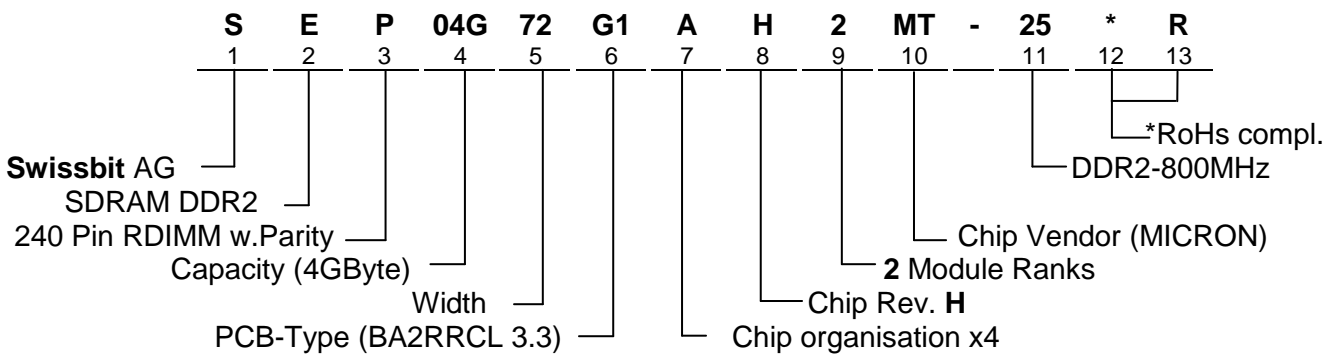
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	6400-CL6	5300-CL5
0	NUMBER OF SPD BYTES USED	0x80	
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08	
2	FUNDAMENTAL MEMORY TYPE	0x08	
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0E	
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0B	
5	DIMM HIGHT AND MODULE RANKS	0x61	
6	MODULE DATA WIDTH	0x48	
7	MODULE DATA WIDTH (continued)	0x00	
8	MODULE VOLTAGE INTERFACE LEVELS (V_{DDQ})	0x05	
9	SDRAM CYCLE TIME, (t_{CK}) [max CL]	0x25	0x30
10	SDRAM ACCESS FROM CLOCK, (t_{AC}) [max CL]	0x40	0x45
11	MODULE CONFIGURATION TYPE	0x06	
12	REFRESH RATE / TYPE	0x82	
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x04	
14	ERROR- CHECKING SDRAM DATA WIDTH	0x04	
15	Reserved	0x00	
16	BURST LENGTHS SUPPORTED	0x0C	
17	NUMBER OF BANKS ON SDRAM DEVICE	0x08	
18	CAS LATENCIES SUPPORTED	0x70	0x38
19	MODULE THICKNESS	0x01	
20	DDR2 DIMM TYPE	0x01	
21	SDRAM MODULE ATTRIBUTES	0x05	
22	SDRAM DEVICE ATTRIBUTES: Weak Driver and 50 Ω ODT and Supports PASR	0x03	
23	SDRAM CYCLE TIME, (t_{CK}) [max CL – 1]	0x30	0x3D
24	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 1]	0x40	0x45
25	SDRAM CYCLE TIME, (t_{CK}) [max CL – 2]	0x3D	0x50
26	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 2]	0x40	0x45
27	MINIMUM ROW PRECHARGE TIME, (t_{RP})	0x3C	
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t_{RRD})	0x1E	
29	MINIMUM RAS# TO CAS# DELAY, (t_{RCD})	0x3C	
30	MINIMUM RAS# PULSE WIDTH, (t_{RAS})	0x2D	
31	MODULE BANK DENSITY	0x02	

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	5300-CL5	
32	ADDRESS AND COMMAND SETUP TIME, (t _{ISB})	0x17	0x20
33	ADDRESS AND COMMAND HOLD TIME, (t _{IHB})	0x25	0x27
34	DATA / DATA MASK INPUT SETUP TIME, (t _{DSB})	0x05	0x10
35	DATA / DATA MASK INPUT HOLD TIME, (t _{DHB})	0x12	0x17
36	WRITE RECOVERY TIME, (t _{WR})	0x3C	
37	WRITE to READ Command Delay, (t _{WTR})	0x1E	
38	READ to PRECHARGE Command Delay, (t _{RTP})	0x1E	
39	Mem Analysis Probe	0x00	
40	Extension for Bytes 41 and 42	0x00	
41	MIN ACTIVE AUTO REFRESH TIME, (t _{RC})	0x3C	
42	MINIMUM AUTO REFRESH TO ACTIVE / AUTO REFRESH COMMAND PERIOD, (t _{RFC})	0x7F	
43	SDRAM DEVICE MAX CYCLE TIME, (t _{CKMAX})	0x80	
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME, (t _{DQSQ})	0x14	0x18
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR, (t _{QHS})	0x1E	0x22
46	PLL Relock Time	0x0F	
47-61	Optional Features, not supported	0x00	
62	SPD REVISION	0x13	
63	CHECKSUM FOR BYTES 0-62	0xEC	0x11
64-66	MANUFACTURER'S JEDEC ID CODE	0x7F	
67	MANUFACTURER'S JEDEC ID CODE (continued)	0xDA	
68-71	RESERVED	0x00	
72	MANUFACTURING LOCATION	X	
73-90	MODULE PART NUMBER (ASCII)	"SEP04G72G1AH2MT-XX"	
91	PCB IDENTIFICATION CODE	0x01	
92	IDENTIFICATION CODE (continued)	0x00	
93	YEAR OF MANUFACTURE IN BCD	X	
94	WEEK OF MANUFACTURE IN BCD	X	
95-98	MODULE SERIAL NUMBER	X	
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	0x00	
128-255	Open for customer use	0xFF	

Part Number Code



* optional / additional information

Revision History		
Revision	Changes	Date
1.0	Initial Revision	11.09.2009
1.1	new Speed-Grades added	07.01.2010
1.2	I _{DD} Specification corrected	14.02.2014

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CE Declaration of Conformity

We

Manufacturer: Swissbit AG
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Switzerland

declare under our sole responsibility that the product

Product Type: 4GB DDR2 RDIMM
Brand Name: SWISSMEMORY™
Product Series: DDR2 RDIMM
Part Number: SEP04G72G1AH2MT-xxR

to which this declaration relates is in conformity with the following directives:

2002/96/EC Category 3 (WEEE)

following the provisions of Directive

Restriction of the use of certain hazardous substances 2011/65/EU

Swissbit AG, February 2014



Manuela Kögel
Head of Quality Management