SYNCOAM Co., Ltd

Version : 1.2

SEPS200A

128 x 64 Dots, Mono PM-OLED Display Driver and Controller

1. FEATURES

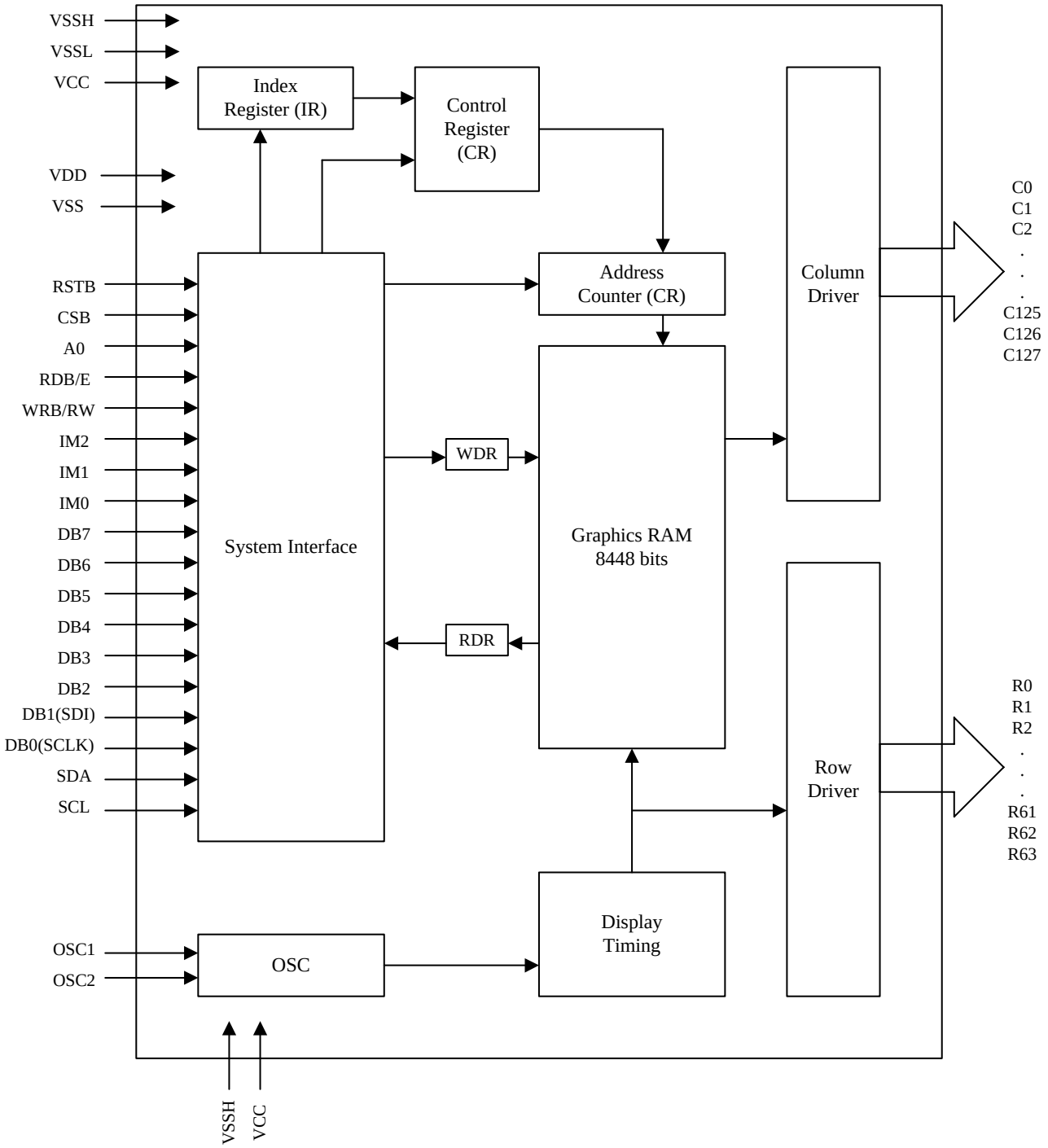
- Support maximum 128 x 64 dot MONO matrix panel
- Embedded 128 x 64 bits SRAM
- Power Supply
  - VDD : 1.6V ~ 3.6V for I/O and IC Logic (single power)
  - VCC : 7.0V ~ 18.0V for Panel Driving
- Column maximum Source Current : 255 uA
- Row maximum Sink Current : 33 mA
- Interface
  - 8-bits 6800-series parallel Interface
  - 8-bits 8080-series parallel Interface
  - SPI (serial Peripheral Interface)
  - I^2C Interface
- On-Chip Oscillator
- Various Instruction Set
  - Screen Saver (Horizontal and Vertical scrolling)
  - Window address function to specify a rectangular area on the internal RAM
  - Row re-mapping and Column re-mapping
  - Programmable frame frequency and multiplexing ratio
  - 256-step contrast control

2. GENERAL DESCRIPTION

The SEPS200A is a single-chip CMOS OLED/PLED drive with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 128 columns, 64 Rows that can support a maximum display resolution of 128 x 64. It is designed for Common Cathode type OLED panel.

3. BLOCK DIAGRAM

Figure 3-1 : Block Diagram



4. PIN DESCRIPTION

Table 4-1 : Pin Description

Pin Name	I/O	Connected	Description
IM[2:0]	I	VSS/VDD	MCU bus interface selection pin
CSB	I	MPU	Selects the SEPS200A. Low : SEPS200A is selected and can be accessed High : SEPS200A is not selected and cannot be accessed
A0	I	MPU	Selects the data / command. Low : command High : parameter / data
RDB/E	I	MPU	For an 80-series bus interface, serves as a read strobe signal, and reads data at the low level. For a 68-series bus interface, serves as an enable signal to activate data read/write operation. When using SPI, fix it to VDD or VSS level
WRB/RW	I	MPU	For an 80-series bus interface, serves as a write strobe signal, and writes data at the low level. For a 68-series bus interface, serves as a signal to select data read/ write operation. Low : write, High : read When using SPI, fix it to VDD or VSS level
SCL	I	MPU	I2C Clock Pin
SDA	I/O	MPU	I2C Data In/Out Pin
DB[7:4] DB[3]/R/W DB[2]/SDO DB[1]/SDI DB[0]/SCLK	I/O	MPU	Serves as an 8-bit bi-directional data bus. 8-bit bus interface : DB[7:0] **For a clock-synchronous serial interface, serves as the serial data input pin (SDI).** SDO : serial data output (floating @ serial mode) SDI : serial data input SCLK : serial clock
OSC1	I	-	When the external clock mode is selected, OSC1 is used external clock input.
OSC2	O		
RSTB	I	MPU	Reset control (active low).
C[127:0]	O	PANEL	OLED Display column outputs.
R[63:0]	O	PANEL	OLED Display row outputs.
OSC_TEST	O	OPEN	TEST Pin
PSELB[1:0]	I	VSS	TEST Pin
TEST[3:0]	O	OPEN	TEST Pin
TESTH[3:0]	O	OPEN	TEST Pin
IREF	-	Resistor	Refer to page 42
VDD	P	POWER	Logic power supply (1.6V ~3.6V).
VCC	P	POWER	Data driver power supply (7V ~ 18V)
VCCR	P	POWER	Generated power for scan off
VCCM	P	POWER	Generated power for logic
VDDL	P	POWER	Generated power for logic
VCCL	P	POWER	Generated power for analog circuit
VSS	P	POWER	This is a ground pin.
VSSH	P	POWER	This is a ground pin..
VSSL	P	POWER	This is an analog ground pin. In case of COG, connect to VSS on the FPCB to prevent a noise.
VSZH	P	POWER	Tie zener diode

5. FUNCTIONAL BLOCK DESCRIPTIONS

5.1 MCU Interface selection

SEPS200A MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 5-1.

Table 5.1-1 : MCU bus interface pin selection

IM2	IM1	IM0	Interface Mode	Pins
0	0	0	80	DB7-DB0
0	0	1	68	DB7-DB0
0	1	1	SPI	DB1(SDI) -DB0(SCLK)
1	1	1	I^2C	SDA, SCL

Table 5.1-2 : MCU Interface assignment under different bus interface mode

			Data/Command Interface								Control Signal				
	SDA	SCL	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	WRB(RW)	RDB(E)	CSB	A0	RSTB
8-bit 8080	Tie Low		DB[7:0]								WRB	RDB	CSB	A0	RSTB
8-bit 6800	Tie Low		DB[7:0]								RW	E	CSB	A0	RSTB
SPI	Tie Low		Tie Low				R/W	SDO	SDI	SCLK	Tie Low		CSB	A0	RSTB
I^2C	SDA	SCL	Tie Low								Tie Low			Tie Low Tie High	RSTB

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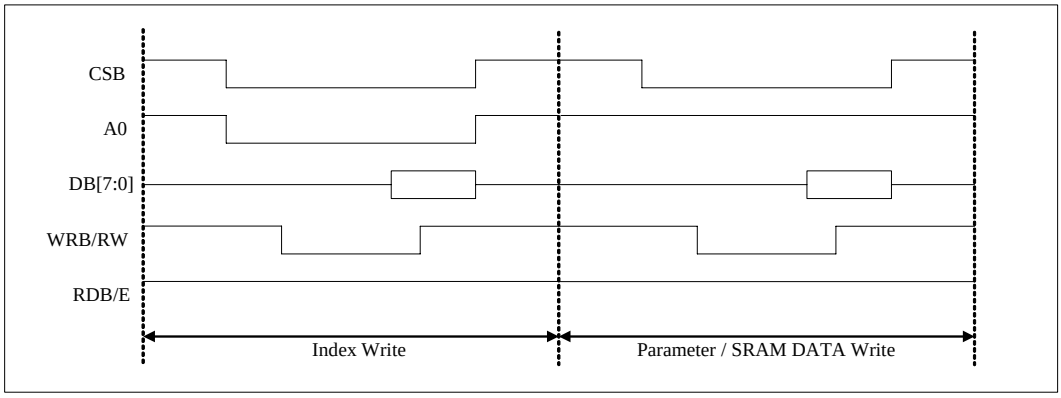
5.1.1 MCU Parallel 8080-series Interface

SEPS200A MCU interface consist of 8 data pins and 5 control pins.

Table 5.1.1-1 : Control pins of 8080 interface

CSB	A0	WRB	RDB	Operation
0	0	0	1	Write command
0	0	1	0	Read status
0	1	0	1	Write data
0	1	1	0	Read data

Figure 5.1.1-1 : 80 SYSTEM 8-bit bus interface



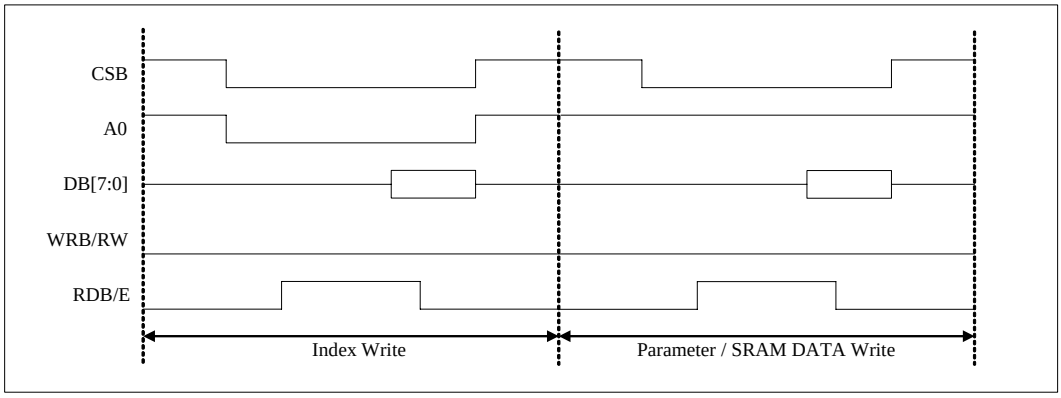
5.1.2 MCU Parallel 6800-series Interface

SEPS200A MCU interface consist of 8 data pins and 5 control pins.

Table 5.1.2-1 : Control pins of 6800 interface

CSB	A0	RW	E	Operation
0	0	0	1	Write command
0	0	1	1	Read status
0	1	0	1	Write data
0	1	1	1	Read data

Figure 5.1.2-1 : 68 SYSTEM 8-bit bus interface



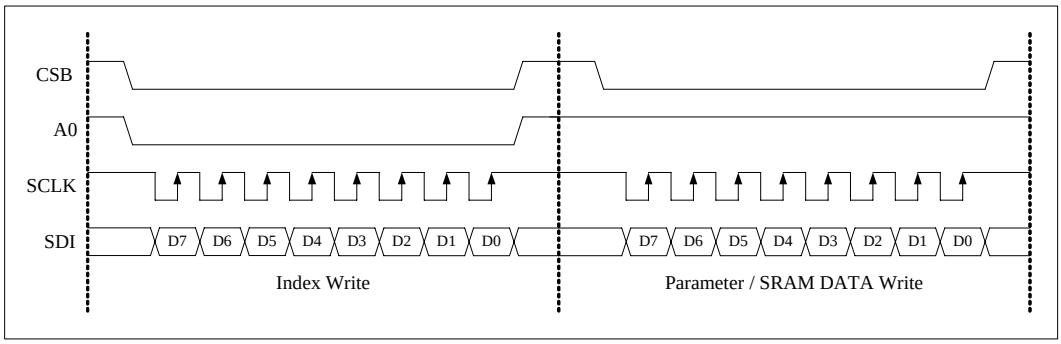
5.1.3 Serial Peripheral Interface (SPI)

The serial interface consist of serial clock SCLK, serial data SDI, A0, CSB. When chip is not selected, internal shift register and counter are reset to initial value. Input data through SDI pin are latched at the rising edge of serial clock(SCLK) in the sequence of MSB first and converted to 8 – bit parallel data and handled at the rising edge of last serial clock. Serial data input (SDI) are identified to display data or command by A0 bit data at the rising of first serial clock(SCLK).

Table 5.1.3-1 : Control pins of SPI interface

CSB	A0	Function
L	L	Command
L	H	Parameter/ Data

Figure 5.1.3-1 : SPI SYSTEM 8-bit bus interface

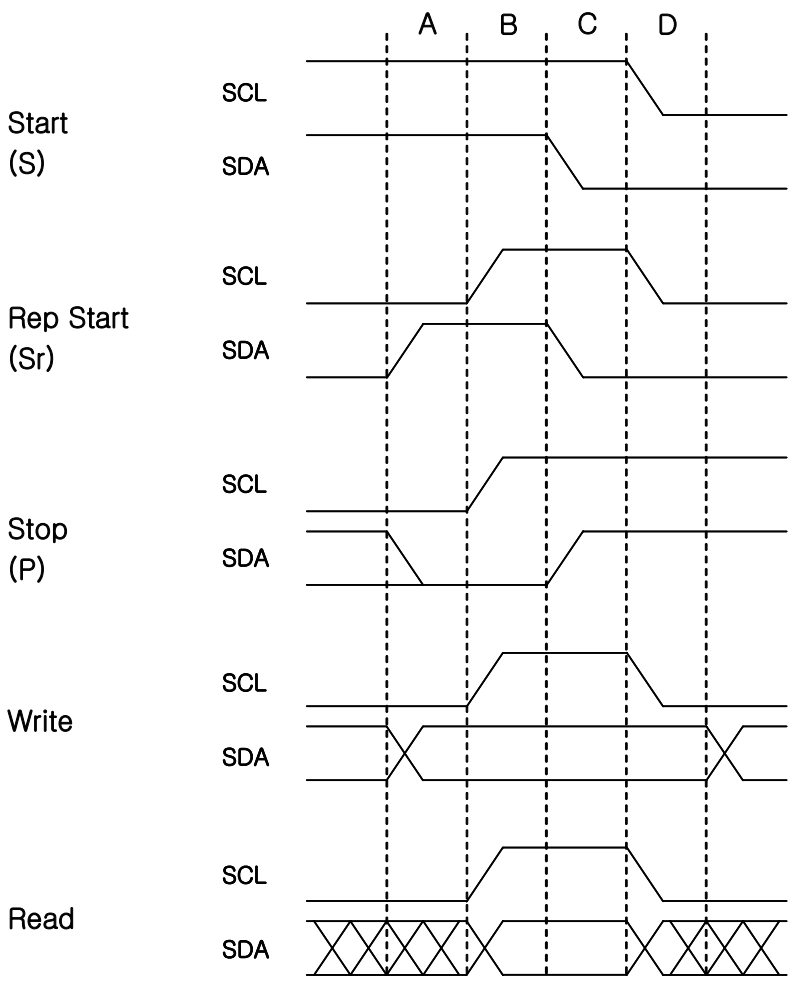


5.1.4 MCU I²C Interface

Bit Transfer

The Bit Transfer handles the actual transmission of data and the generation of the specific levels for START, Repeated START, and STOP signals by controlling the SCL and SDA lines.

Figure 5.1.4-1



Data validity:

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW

START and STOP conditions:

Within the procedure of the I2C, unique situations arise which are defined as START(S) and STOP(P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. The bus stays busy if a repeated START(Sr) is generated instead of a STOP condition.

Byte Format

The Byte Format handles I2C traffic at the byte level. It takes data from the Command Register and translates it into sequences based on the transmission of a single byte.

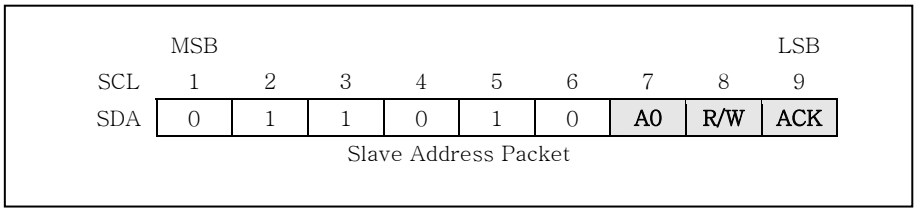
Table 5.1.4-1 : Mode pins of I2C interface

R/W	MODE	Co	MODE	D/C	MODE
0	Write	0	Continuation.	0	Command
1	Read	1	Not Continuation	1	Data

Slave Address Packet:

The first byte of data transferred by the master immediately after the START signal is the slave address. No two slaves in the system can have the same address. Only the slave with an address that matches the one transmitted by the master will respond by returning an acknowledge bit by pulling the SDA low at the 9th SCL clock cycle.

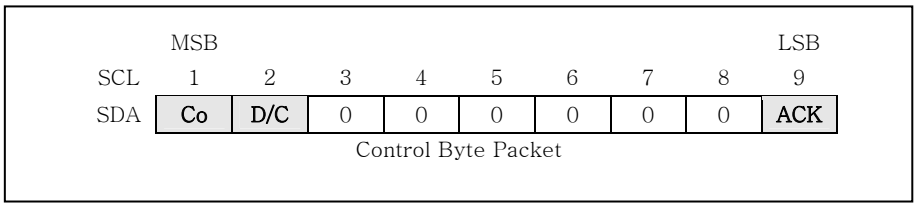
Figure 5.1.4-2 : Slave Address Packet



Control Byte Packet:

Once successful slave addressing has been achieved, Each transferred byte is address of command register or memory. It is followed by a D/C bit on the second SCL clock cycle. One-Byte address, Multi-Byte Write can proceed on a Co bit on the first SCL clock cycle.

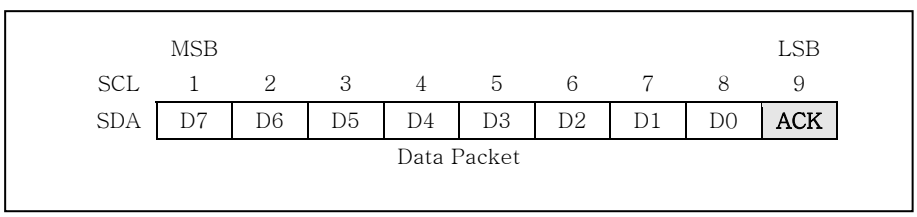
Figure 5.1.4-3 : Control Byte Packet



Data Packet:

The data transfer can proceed on a byte-by-byte basis in the direction specified by the RW bit sent by the master. Each transferred byte is followed by an acknowledge bit on the 9th SCL clock cycle. If the slave signals a No Acknowledge, the master can generate a STOP signal to abort the data transfer.

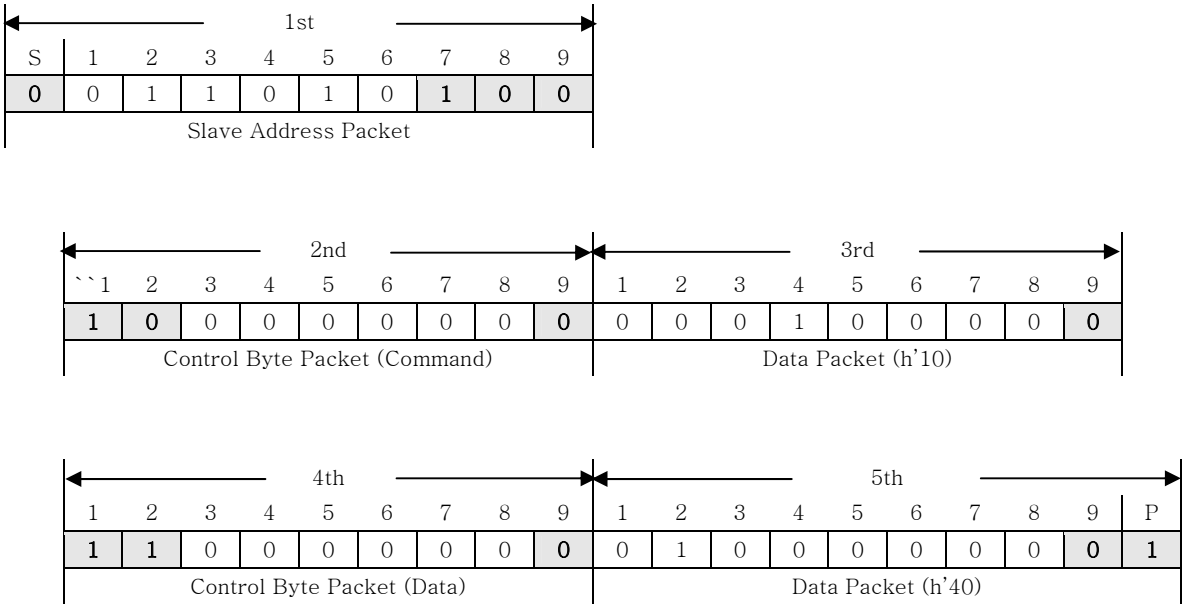
Figure 5.1.4-4 : Data PAcket

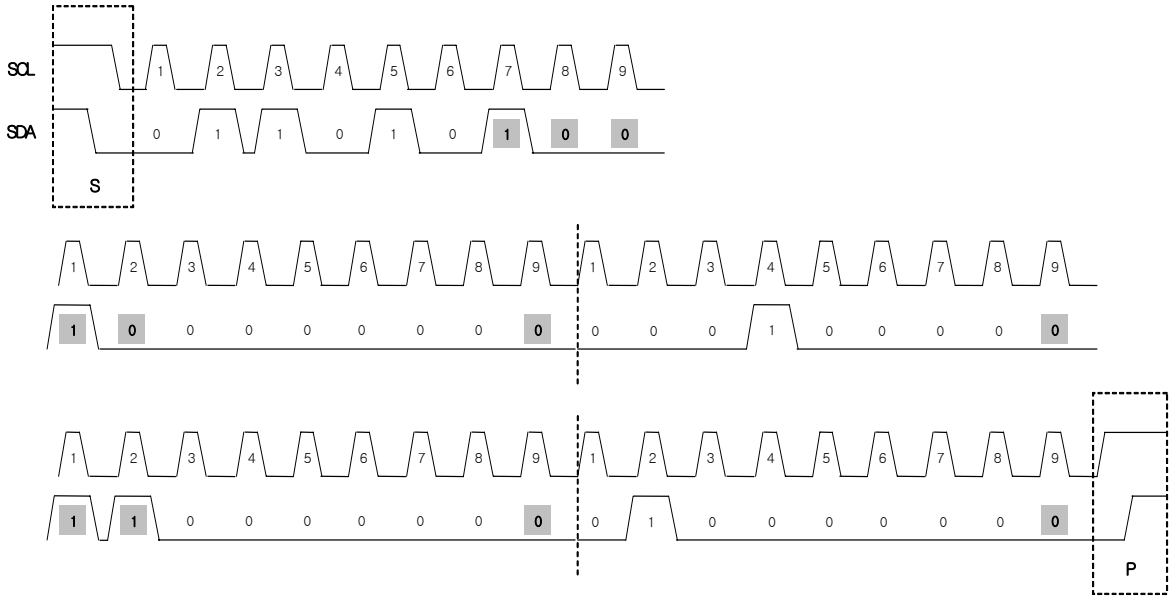


Example1

Write 1 byte of data to a command register

Figure 5.1.4-5 : Sequence Write 1byte of data to a command register

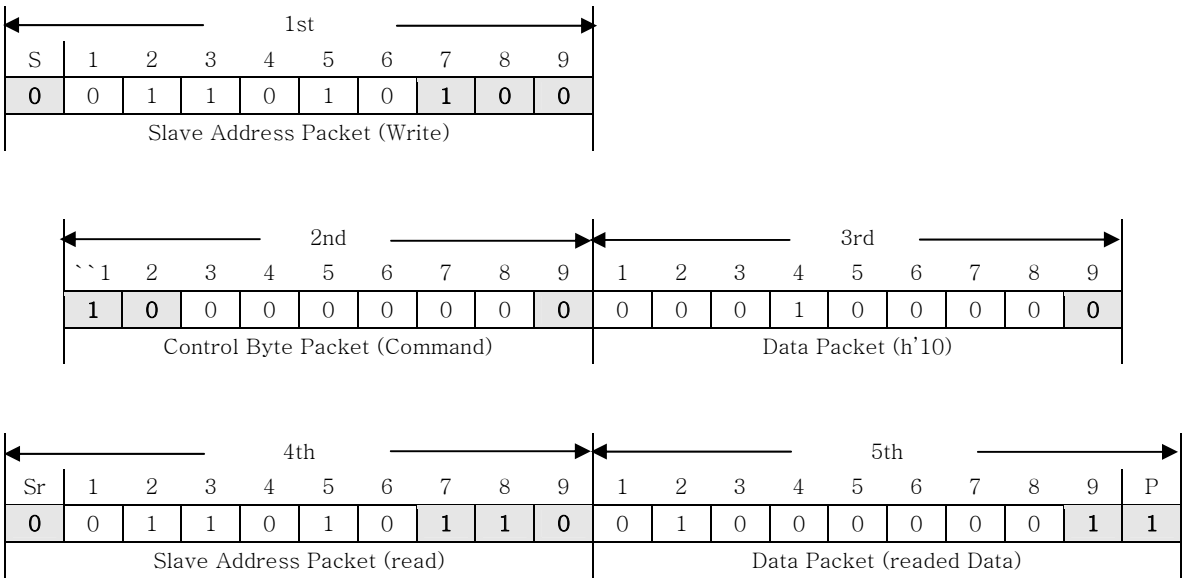


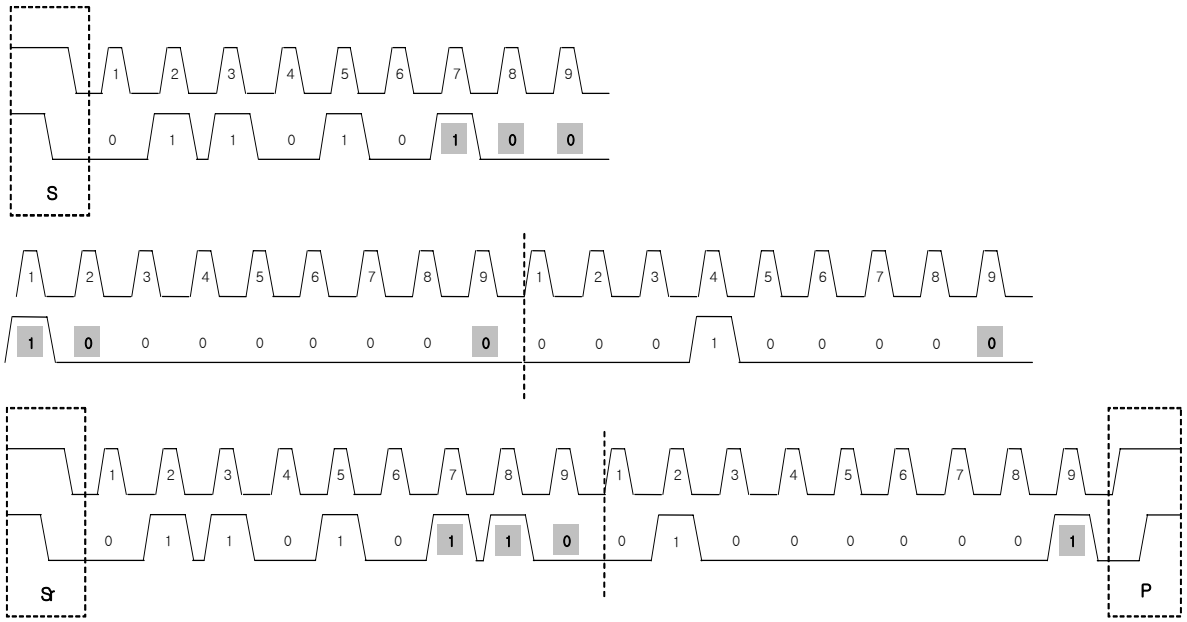


Example2

Read 1 byte of data from a command register

Figure 5.1.4-6 : Sequence Read 1 byte of data from a command register

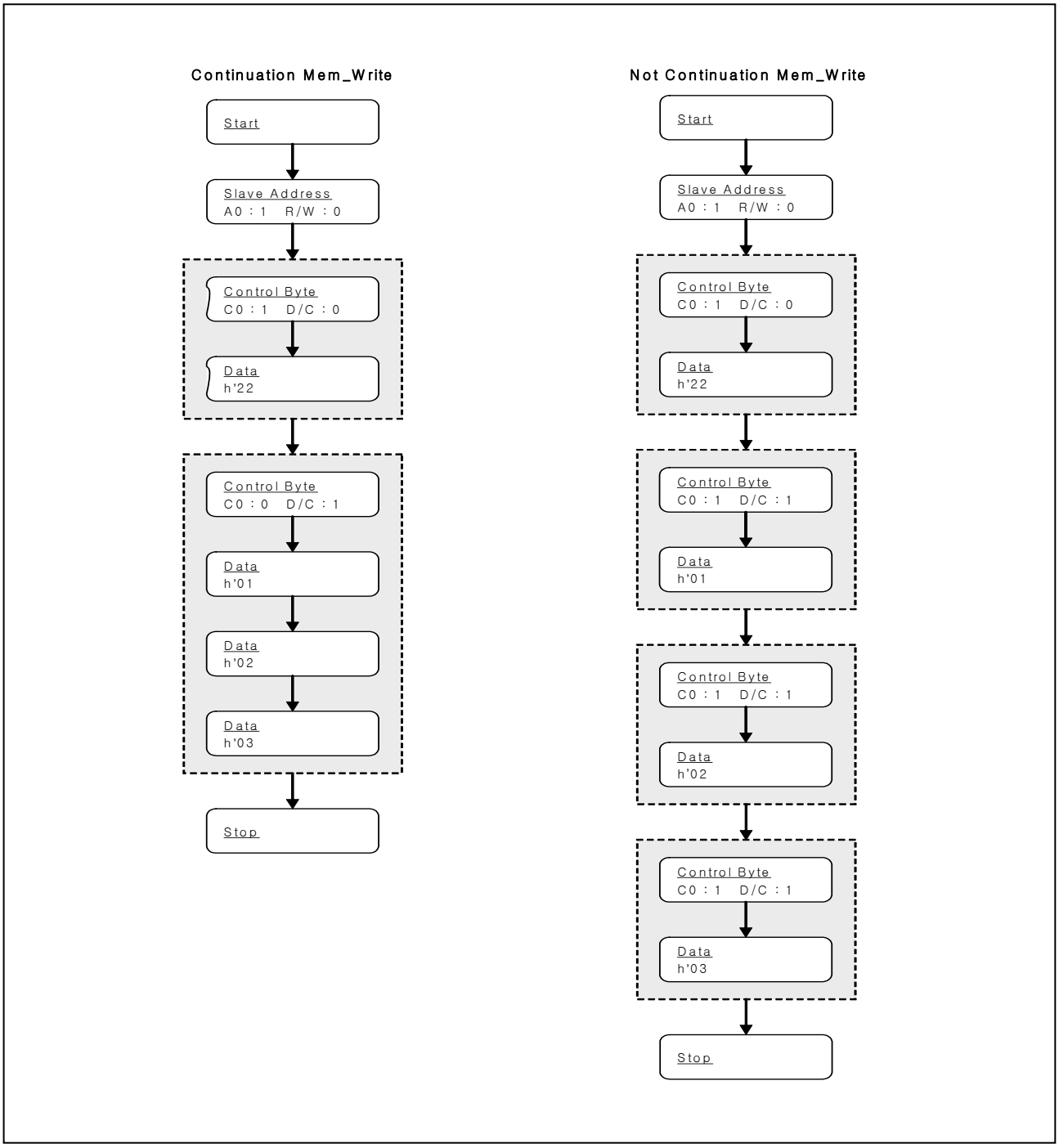




Example3

Combined format sequence
1) Continuation Write data to a memory
2) Not continuation Write data to a memory

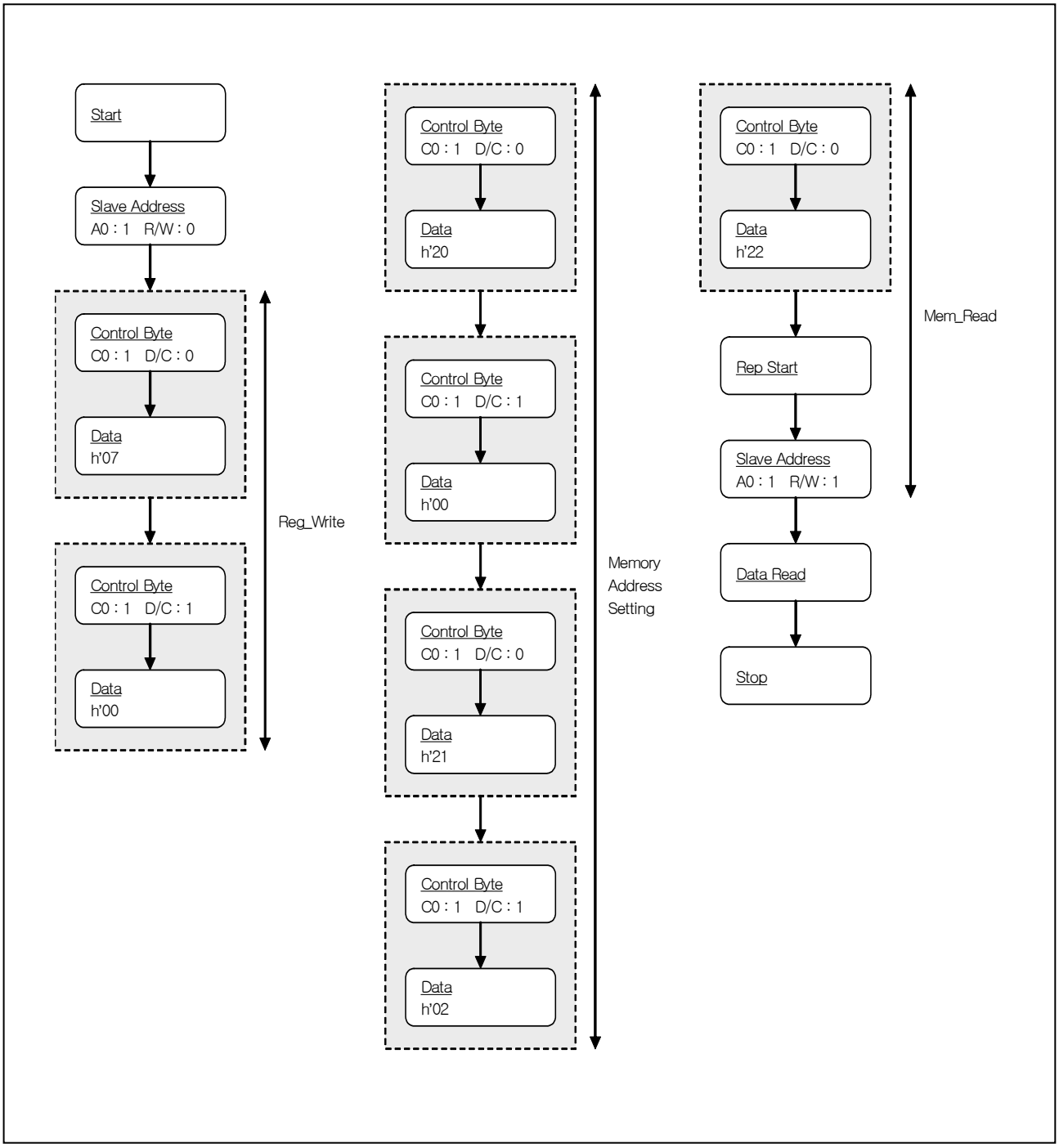
Figure 5.1.4-7 : Combined format sequence1



Example4

Combined format sequence
1) Write data to a command register
2) Read data from a memory

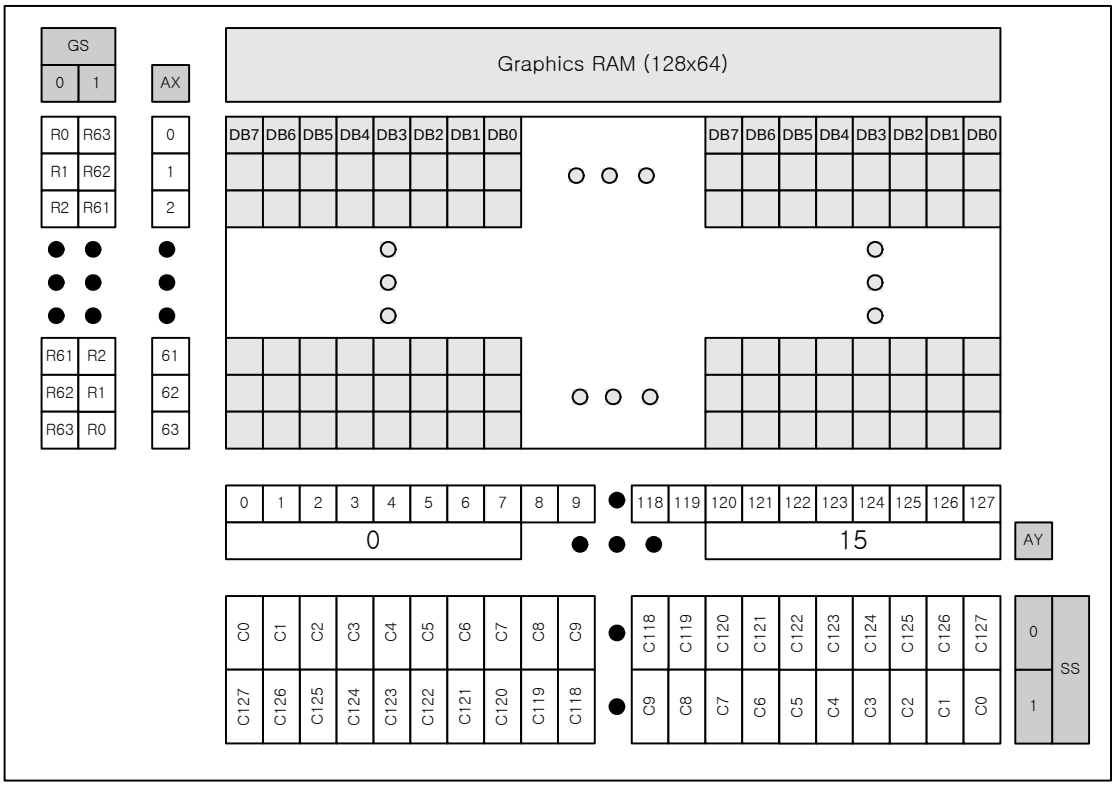
Figure 5.1.4-8 : Combined format sequence2



5.1.5 Graphic Display Data RAM (GRAM)

The GRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the GRAM is 128 x 64 bits

Figure 5.1.5-1 : GRAM structure of 200A



5.1.6 Power On and OFF sequence

Power On Sequence

1. VDD Power On.
2. After VDD becomes stable, wait for 100ms(t1), and then set RSTB pin LOW (logic low) for at least 1us (t2), and then HIGH(logic high).
3. After RSTB pin HIGH, wait for at least 10ms (t3). Then Standby Mode Off and VCC Power on.
4. After Standby Mode Off, wait for at least 10ms(t4). Then Display On.

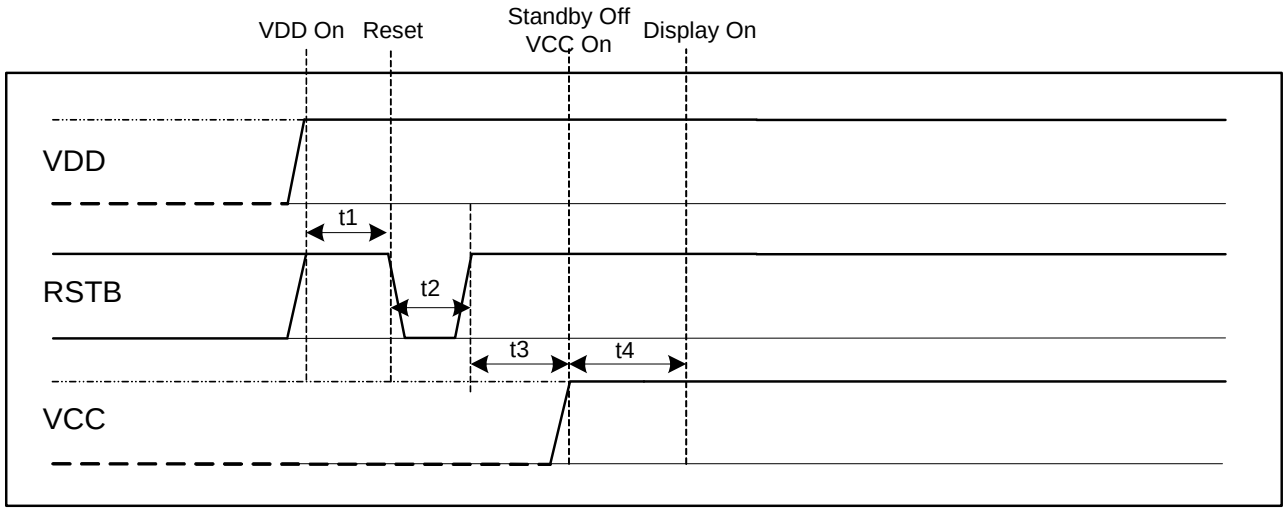


Figure 5.1.6-1 : GRAM structure of 200A

Power Off Sequence

1. Display Off.
2. VCC Power Off.
3. Wait for at least 100ms(tOFF). Then VDD Power Off.

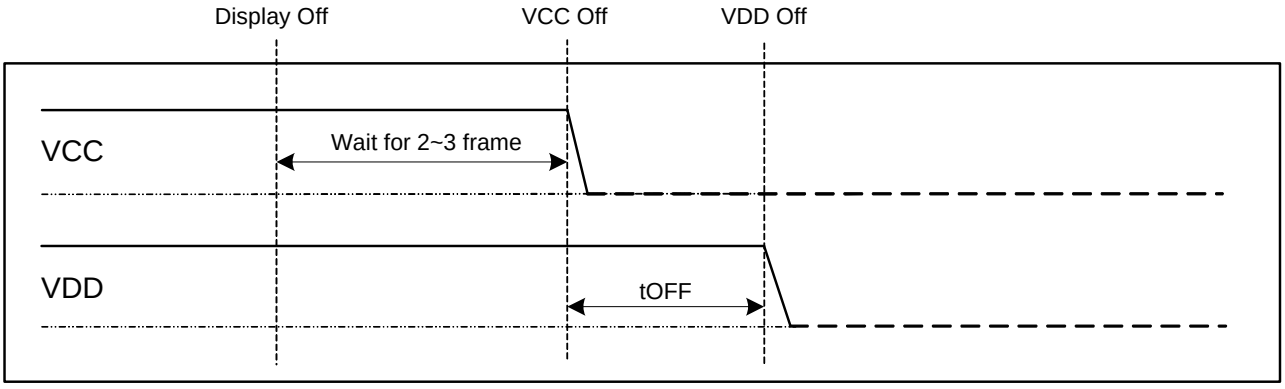
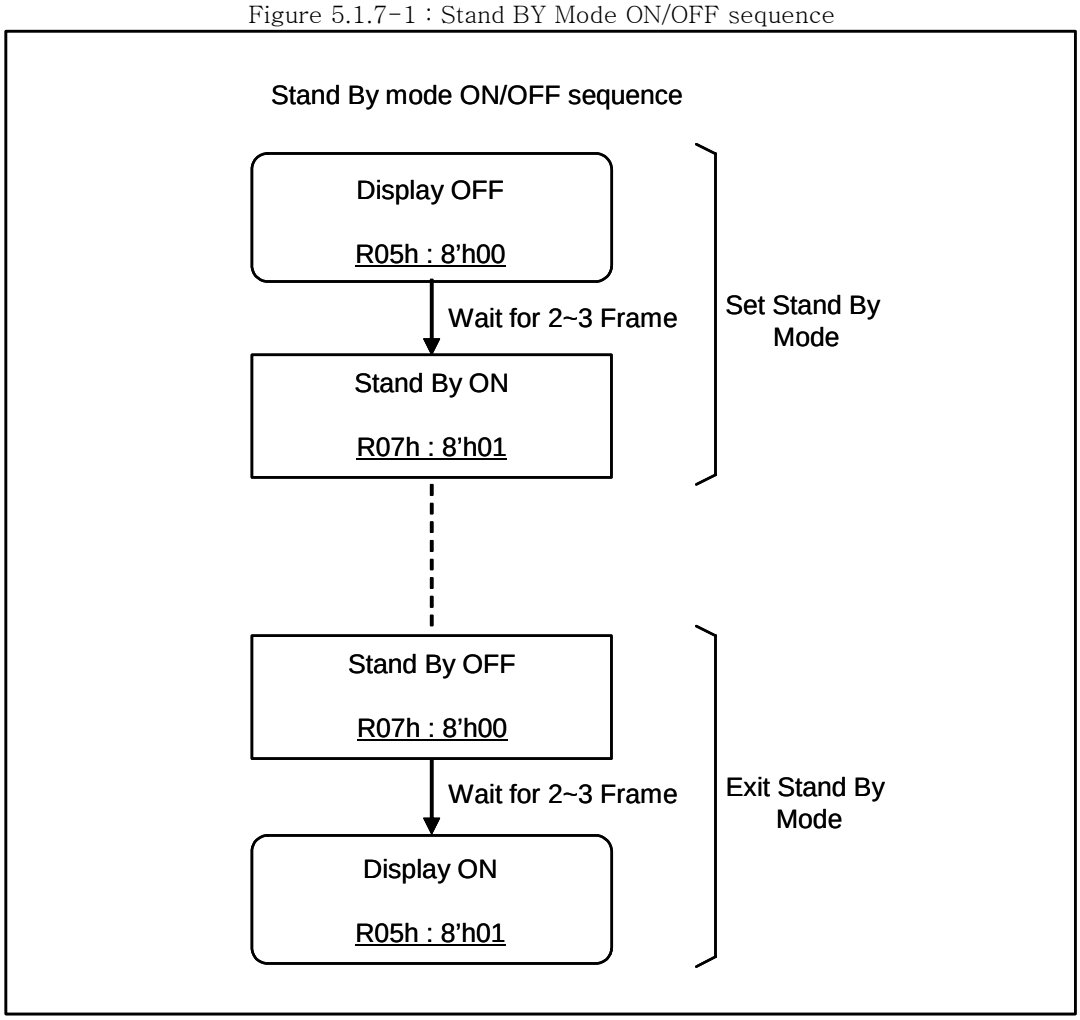


Figure 5.1.6-2 : GRAM structure of 200A

5.1.7 Stand BY Mode ON/OFF sequence

Figure 5.1.7-1 : Stand BY Mode ON/OFF sequence



6. COMMAND TABLE

Table 6-1 : Command Table

	Main Category		Sub Category	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
1	Display Control	01h	Soft Reset	0	0	0	0	0	0	0	SRST (0)
		02h	Driver Output Control 1	0	0	NL5 (1)	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (1)	NL0 (1)
		03h	Driver Output Control 2	0	0	0	0	0	0	GS (0)	SS (0)
		04h	Entry Mode	0	0	0	0	0	0	ID1 (1)	ID0 (1)
		05h	Display Control	0	0	REV (0)	FULLH (0)	0	0	0	DISON (0)
		06h	Frame Cycle Control	SELCLK (0)	FR2 (0)	FR1 (1)	FR0 (0)	OSC_DIV3 (0)	OSC_DIV2 (0)	OSC_DIV1 (0)	OSC_DIV0 (0)
		07h	Power Control	0	0	0	0	0	0	0	STB (1)
2	Power Control	10h	Pre-Charge Current	PRECUR7 (0)	PRECUR6 (1)	PRECUR5 (0)	PRECUR4 (0)	PRECUR3 (0)	PRECUR2 (0)	PRECUR1 (0)	PRECUR0 (0)
		11h	Pre-Charge Time	0	0	0	0	PRECLK3 (1)	PRECLK2 (0)	PRECLK1 (0)	PRECLK0 (1)
		12h	Dis-Charge Time	0	0	0	0	DISCLK3 (1)	DISCLK2 (0)	DISCLK1 (0)	DISCLK0 (1)
		13h	Driving Current	DRVCUR7 (1)	DRVCUR6 (0)	DRVCUR5 (0)	DRVCUR4 (0)	DRVCUR3 (0)	DRVCUR2 (0)	DRVCUR1 (0)	DRVCUR0 (0)
		14h	Scan Off	0	0	0	0	SCANOFF 3(0)	SCANOFF 2(0)	SCANOFF 1(0)	SCANOFF 0(0)
3	RAM Access	20h	RAM Address Set	0	0	AX5 (0)	AX4 (0)	AX3 (0)	AX2 (0)	AX1 (0)	AX0 (0)
		21h	RAM Address Set	0	0	0	0	AY3 (0)	AY2 (0)	AY1 (0)	AY0 (0)
		22h	RAM Data Write/Read	RAM Write Data/RAM Read Data							
4	Coordinate Control	30h	Row Scan Start	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
		31h	Vertical Scroll Control	0	0	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
		32h	Screen Start Drive Position	0	0	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)
		33h	Screen End Drive Position	0	0	SE15 (1)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)
		34h	Horizontal RAM Start address	0	0	0	0	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
		35h	Horizontal RAM End Address	0	0	0	0	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
		36h	Vertical RAM Start Address	0	0	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
		37h	Vertical RAM End Address	0	0	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
5	Screen Saver Control	50h	Screen Saver Control	0	0	0	0	0	0	SSLP (0)	SSON (0)
		51h	Saver Sleep Timer	SSST7 (0)	SSST6 (0)	SSST5 (0)	SSST4 (0)	SSST3 (0)	SSST2 (0)	SSST1 (0)	SSST0 (0)
		52h	Saver Update Timer	SSUT7 (0)	SSUT6 (0)	SSUT5 (0)	SSUT4 (0)	SSUT3 (0)	SSUT2 (0)	SSUT1 (0)	SSUT0 (0)
		53h	Saver Mode	0	0	0	0	0	0	SSUD (0)	SSLR (0)
		54h	Saver Moving Step	SSSV3 (0)	SSSV2 (0)	SSSV1 (0)	SSSV0 (0)	SSSH3 (0)	SSSH2 (0)	SSSH1 (0)	SSSH0 (0)
6		72h	Iref resistor	0	0	0	IREF (1)	0	0	0	0

6.1 Reset Function

1. Soft Reset (SRST = “0”)
2. Driver Output Control 1 (NL5-0 = “111111”)
3. Driver Output Control 2 (SM = “0”, GS = “0”, SS = ”0”)
4. Entry Mode (ID1-0 = ”11”)
5. Display Control (REV = ”0”, FULLH = ”0”, DISON= ”0”)
6. Frame Cycle Control (SELCLK = ”0”, FR2-0 = ”010”, OSC_DIV3-0 = ”0000”)
7. Power Control (STB = ”1”)
8. Pre-Charge Current (PRECUR7-0 = ”01000000”)
9. Pre-Charge Time (PRECLK3-0 = ”1001”)
10. Dis-Charge Time (DISCLK3-0 = ”1001”)
11. Driving Current (DRVCUR7-0 = ”10000000”)
12. Scan Off (SCANOFF3-0 = ”0000”)
13. RAM Address Set (AX5-0 = ”000000”)
14. RAM Address Set (AY3-0 = ”0000”)
15. Row Scan Start (SCN5-0 = ”000000”)
16. Vertical Scroll Control (VL5-0 = ”000000”)
17. Screen Start Drive Position (SS15-0 = ”000000”)
18. Screen End Drive Position (SE15-0 = ”111111”)
19. Horizontal RAM Start Address (HSA3-0 = ”0000”)
20. Horizontal RAM End Address (HEA3-0 = ”1111”)
21. Vertical RAM Start Address (VSA5-0 = ”000000”)
22. Vertical RAM End Address (VEA5-0 = ”111111”)
23. Screen Saver Control (SSLP = ”0”, SSON = ”0”)
24. Saver Sleep Timer (SSST7-0 = ”00000000”)
25. Saver Update Timer (SSUT7-0 = ”00000000”)
26. Saver Mode (SSUD = ”0”, SSLR = ”0”)
27. Saver Moving Step (SSSV3-0 = ”0000”, SSSH3-0 = ”0000”)
28. Iref resister (IREF = ‘1’) ** R72h 0x10

7. COMMAND DESCRIPTION

7.1 Display Control

7.1.1 Soft Rest (R01h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1								SRST (0)

Table 7.1.1-1 : Soft Reaet

Soft Reset	Actions						
ON	Standby	Display	OSC	GRAM	ALL Reg	Row	Col
	ON	OFF	STOP	Keep	Default	GND	Zener

7.1.2 Driver Output Control 1 (R02h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1			NL5 (1)	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (1)	NL0 (1)

NL5-0 : Set the number of gate lines for driving display panel at an interval of 1 line as the following table. The Gram addressing mapping is independent from the number of gate lines set with the NL 5-0 bits.

Table 7.1.2-1 : Driver Output Control 1

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	Lines	Driven gate lines
0	0	0	0	0	0	setting disabled	Setting disabled	Setting disabled
		. . .				. . .	. . .	. . .
0	0	1	1	1	0	setting disabled	Setting disabled	Setting disabled
0	0	1	1	1	1	128x16	16	R0~R15
0	1	0	0	0	0	128x17	17	R0~R16
0	1	0	0	0	1	128x18	18	R0~R17
						. . .	. . .	. . .
0	1	1	1	1	1	128x32	32	R0~R31
						. . .	. . .	. . .
1	1	1	1	1	0	128x63	63	R0~R62
1	1	1	1	1	1	128x64	64	R0~R63

7.1.3 Driver Output Control 2 (R03h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1						SM (0)	GS (0)	SS (0)

SS : Select the shift direction of outputs from the source pins.
When SS = “0” output from C0 to C127
When SS = “1” output from C127 to C0

GS : Set the shift direction of outputs from the gate driver.

SM : Set the scan order by the gate driver.

Table 7.1.3-1

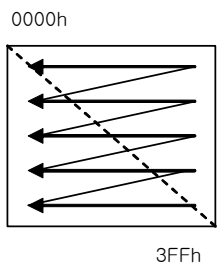
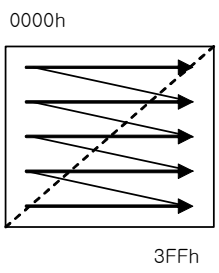
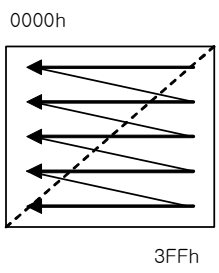
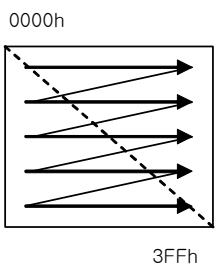
SM	GS	Row Scan Order						
0	0	0	1	2	3	. . .	62	63
0	1	63	62	61	60	. . .	1	0
1	0	1	0	3	2	. . .	63	62
1	1	62	63	60	61	. . .	0	1

7.1.4 Entry Mode (R04h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1							ID1 (1)	ID0 (1)

ID 1-0 : The address counter is automatically increment by 1 as writing data to the internal GRAM when ID 1-0 = "1". The address counter is automatically decrement by 1 as writing data to the internal GRAM when ID 1-0 = "0".

Figure 7.1.4-1 : Address transition direction

ID 1-0 = "00" horizontal : decrement vertical : decrement	ID 1-0 = "01" horizontal : increment vertical : decrement	ID 1-0 = "10" horizontal : decrement vertical : increment	ID 1-0 = "11" horizontal : increment vertical : increment
			

7.1.5 Display Control (R05h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1			REV (0)	FULLH (0)				DISON (0)

REV : This command sets the display to be either normal or inverse. IN normal display a RAM data of 1 indicates an "ON" pixel while in inverse display a RAM data of 0 indicates an "ON" pixel.

Table 7.1.5-1

REV	GRAM	DISPLAY
0	0	0
0	1	1
1	0	1
1	1	0

FULLH : Command forces the entire display to be "ON" regardless of the contents of the display data RAM.

Table 7.1.5-2

FULLH	GRAM	DISPLAY
0	0	0
0	1	1
1	0	1
1	1	1

DISON : This command is used to turn panel display ON or OFF.

Table 7.1.5-3

DISON	DISPLAY
0	OFF
1	ON

7.1.6 Frame Cycle Control (R06h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1	SELCLK (0)	FR2 (0)	FR1 (1)	FR0 (0)	OSC_ DIV3(0)	OSC_ DIV2(0)	OSC_ DIV1(0)	OSC_ DIV0(0)

Table 7.1.6-1 : OSC selection

SELCLK	0	1
Mode	Internal Oscillator	External Source

Table 7.1.6-2 : OSC frequency setting

FR2	FR1	FR0	Frame Rate
0	0	0	65Hz
0	0	1	75Hz
0	1	0	90Hz (default)
0	1	1	105Hz
1	0	0	120Hz
1	0	1	120Hz
1	1	0	120Hz
1	1	1	120Hz

Table 7.1.6-3 : Display frequency divide ration

OSC_DIV3	OSC_DIV2	OSC_DIV1	OSC_DIV0	OSC CLK
0	0	0	0	1/1
0	0	0	1	1/2
0	0	1	0	1/3
0	0	1	1	1/4
0	1	0	0	1/5
0	1	0	1	1/6
0	1	1	0	1/7
0	1	1	1	1/8
1	0	0	0	1/9
1	0	0	1	1/10
1	0	1	0	1/11
1	0	1	1	1/12
1	1	0	0	1/13
1	1	0	1	1/14
1	1	1	0	1/15
1	1	1	1	1/16

7.1.7 Power Control (R07h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1								STB (1)

Table 7.1.7-1

STB	Function	Actions						
1	STANDBY ON	Display	OSC	GRAM	ALL Reg	Latched Data	Row	Col
		OFF	STOP	Keep	Keep	Clear	GND	Zener
0	STANDBY OFF	OFF	START	Keep	Keep	Clear	GND	Zener

7.2 Power Control

7.2.1 Pre-Charge Current (R10h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1	PRE CUR7(0)	PRE CUR6(1)	PRE CUR5(0)	PRE CUR4(0)	PRE CUR3(0)	PRE CUR2(0)	PRE CUR1(0)	PRE CUR0(0)

Table 7.2.1-1

PRECUR[7:0]	0	1	2	3	. . .	128	129	. . .	254	255
Oupput Current[uA]	0	4	8	12	. . .	512	516	. . .	1016	1020

7.2.2 Pre-Charge Time (R11h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1					PRE CLK3(1)	PRE CLK2(0)	PRE CLK1(0)	PRE CLK0(1)

Table 7.2.2-1

PRECLK[3:0]	0	1	2	3	. . .	7	8	. . .	14	15
Pre-charge time [clock]	0	1	2	3	. . .	7	8	. . .	14	15

7.2.3 Dis-Charge Time (R12h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1					DIS CLK3(1)	DIS CLK2(0)	DIS CLK1(0)	DIS CLK0(1)

Table 7.2.3-1

DISCLK[3:0]	0	1	2	3	. . .	7	8	. . .	14	15
Dis-charge time [clock]	Disable	Disable	2	3	. . .	7	8	. . .	14	15

7.2.4 Driving Current (R13h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1	DRV CUR7(1)	DRV CUR6(0)	DRV CUR5(0)	DRV CUR4(0)	DRV CUR3(0)	DRV CUR2(0)	DRV CUR1(0)	DRV CUR0(0)

Table 7.2.4-1

DRVCUR[7:0]	0	1	2	3	. . .	128	129	. . .	254	255
Oupput Current[uA]	0	1	2	3	. . .	128	129	. . .	254	255

7.2.5 Scan Off (R14h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1					SCAN OFF3(0)	SCAN OFF2(0)	SCAN OFF1(0)	SCAN OFF0(0)

Table 7.2.5-1

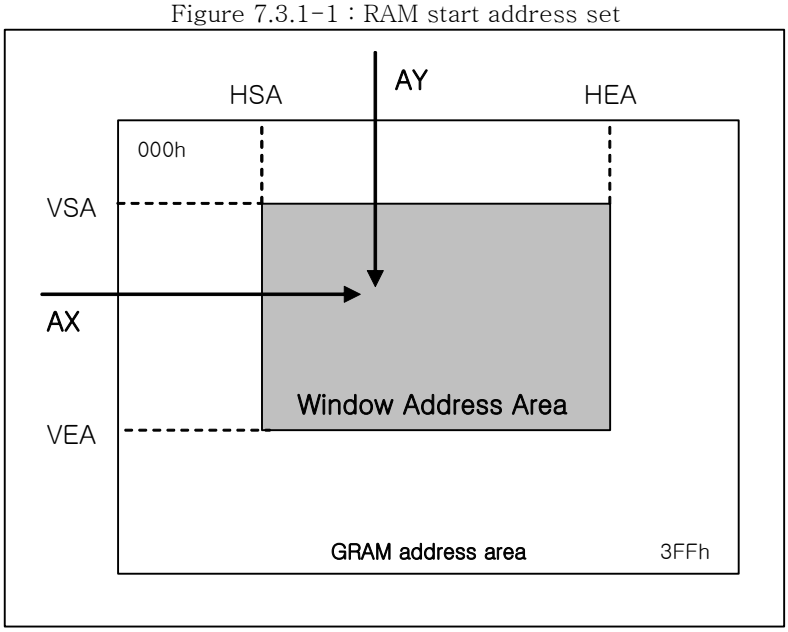
SCANOFF [3:0]	0	1	2	. . .	15
VCCR	VCC * 0.9625	VCC * 0.9250	VCC * 0.8875	. . .	VCC* 0.4000

7.3 RAM Access

7.3.1 RAM Address Set (R20h, R21h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1			AX5 (0)	AX4 (0)	AX3 (0)	AX2 (0)	AX1 (0)	AX0 (0)
						AY3 (0)	AY2 (0)	AY1 (0)	AY0 (0)

Figure 7.3.1-1 : RAM start address set



AX 5-0, AY 3-0 : Represent the RAM address set in the address counter initially. The RAM address is automatically updated according to the ID bits as data are written to the RAM. The address is not automatically updated when reading data from the RAM.

7.3.2 RAM Data Write/Read (R22h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1	RAM Write Data/RAM Read Data							

7.4 Coordinate Control

7.4.1 Row Scan Start (R30h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1			SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)

SCN 5-0 : The SEPS200A allows specifying the gate line from which the gate driver starts scan by setting the SCN 4-0 bits

Table 7.4.1-1

						Scan Start Position (Gate line)	
SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	GS = "0"	GS = "1"
0	0	0	0	0	0	R0	R63
0	0	0	0	0	1	R1	R62
0	0	0	0	1	0	R2	R61
0	0	0	0	1	1	R3	R60
0	0	0	1	0	0	R4	R59
						. . .	. . .
1	0	0	0	0	0	R32	R31
						. . .	. . .
1	1	1	1	1	0	R62	R1
1	1	1	1	1	1	R63	R0

7.4.2 Vertical Scroll Control (R31h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1			VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)

VL 5-0 : The start position for displaying the image is shifted vertically by the number of lines set with the VL 5-0 bits.

Table 7.4.2-1

VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0 lines
0	0	0	0	0	1	1 lines
0	0	0	0	1	0	2 lines
0	0	0	0	1	1	3 lines
0	0	0	1	0	0	4 lines
						. . .
1	0	0	0	0	0	32 lines
						. . .
1	1	1	1	1	0	62 lines
1	1	1	1	1	1	63 lines

7.4.3 Screen Start Drive Position, Screen End Drive Position (R32h, R33h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1			SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)
				SE15 (1)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)

SS1 5-0 : Set the position of the start line from which display starts.

SE1 5-0 : Set the position of the end line at which display ends.

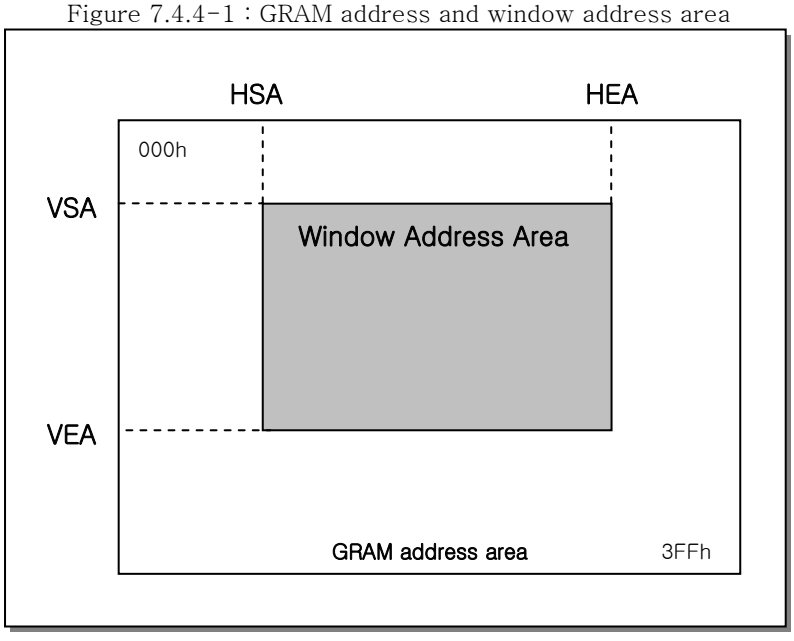
7.4.4 Horizontal RAM Address Postion (R34h, R35h), Veritical RAM Address Postion (R36h, R37h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1					HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
						HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
				VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
				VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)

HSA 3-0/HEA 3-0 : HSA 3-0 and HEA 3-0 represent the respective address at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure “00h”<=HSA 3-0 < HEA 3-0 <= “Fh”

VSA 5-0/VEA 5-0 : VSA 5-0 and VEA 5-0 represent the respective address at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting these bits, be sure “00h”<=VSA 5-0 < VEA 5-0 <= “3Fh”

Figure 7.4.4-1 : GRAM address and window address area



7.5 Screen Saver

7.5.1 Screen Saver Control (R50h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1							SSLP (0)	SSON (0)

Table 7.5.1-1

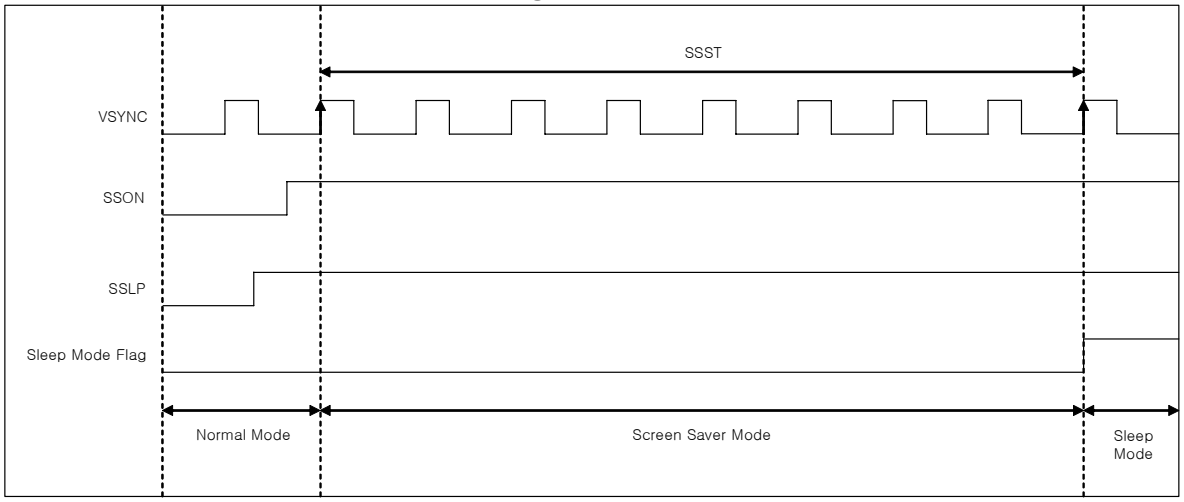
SSON	Saver Mode on/off	SSLP	Saver Sleep Mode
0	OFF	0	OFF
1	ON	1	ON

7.5.2 Screen Saver Sleep Timer (R51h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1	SSST7 (0)	SSST6 (0)	SSST5 (0)	SSST4 (0)	SSST3 (0)	SSST2 (0)	SSST1 (0)	SSST0 (0)

SSST 7-0 : Screen Saver Sleep Timer.

Figure 7.5.2-1



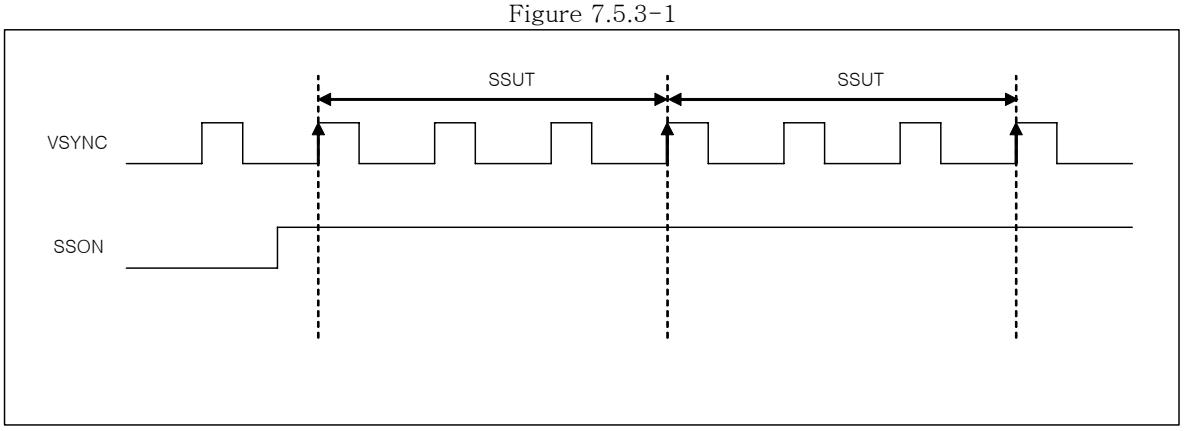
< SSST = '00000111>

7.5.3 Saver Update Timer (R52h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1	SSUT7 (0)	SSUT6 (0)	SSUT5 (0)	SSUT4 (0)	SSUT3 (0)	SSUT2 (0)	SSUT1 (0)	SSUT0 (0)

SSUT 7-0 : Screen Saver Update Timer.

Figure 7.5.3-1



< SSUT = '00000010' >

7.5.4 Saver Mode (R53h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1							SSUD (0)	SSLR (0)

Table 7.5.4-1

SSUD	Saver Mode	SSLR	Saver Mode
0	Up Scroll	0	Left Panning
1	Down Scroll	1	Right Panning

7.5.5 Saver Moving Step (R54h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1	SSSV3 (0)	SSSV2 (0)	SSSV1 (0)	SSSV0 (0)	SSSH3 (0)	SSSH2 (0)	SSSH1 (0)	SSSH0 (0)

Table 7.5.5-1

SSSH3-0	Horizontal Moving	SSSV3-0	Vertical Moving
0	OFF	0	OFF
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15

7.5.6 Iref resistor (R72h)

R/W	A0	IB7	IB6	IB5	IB4	IB3	IB2	B1	IB0
W	1	0	0	0	IREF (1)	0	0	0	0

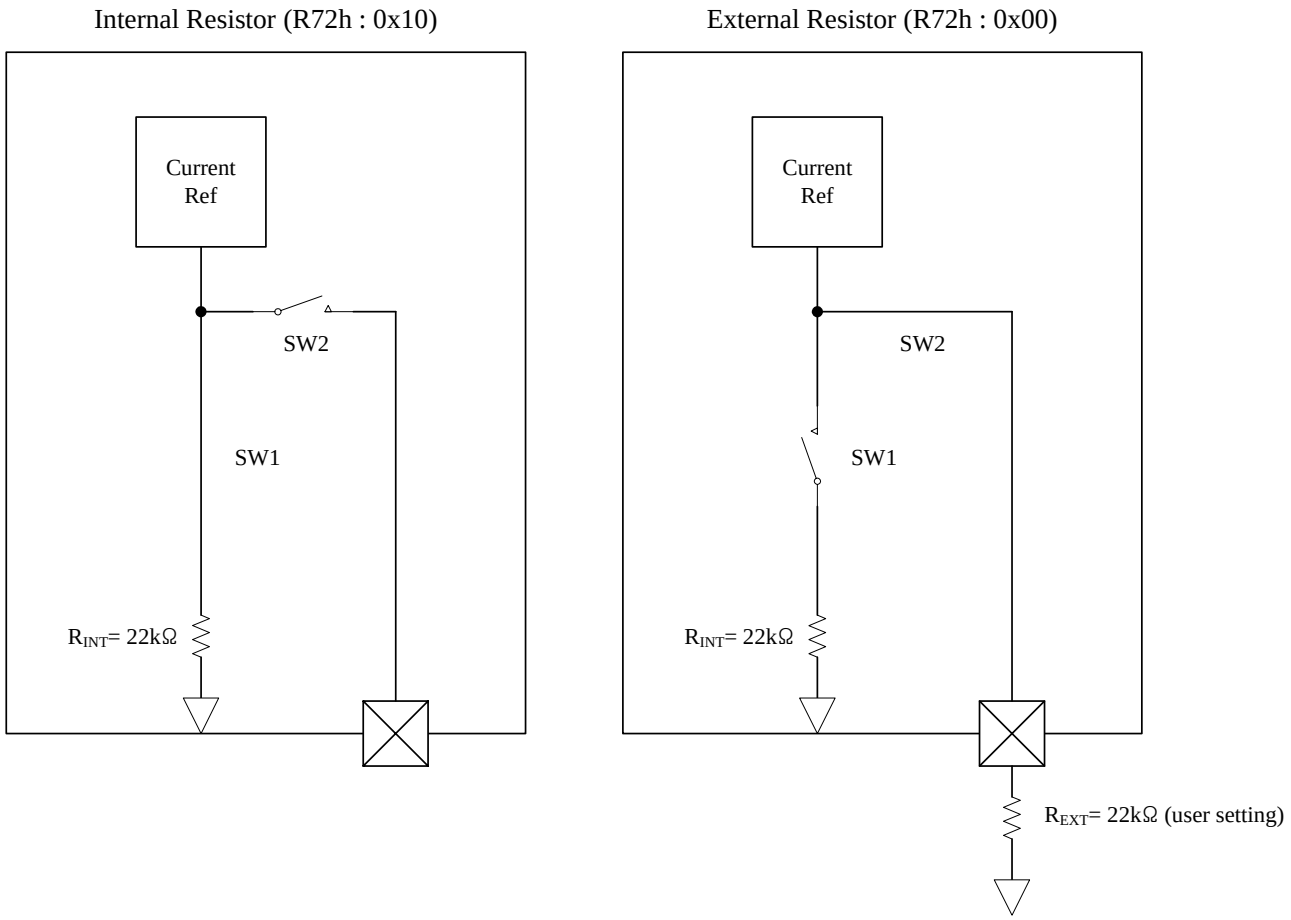


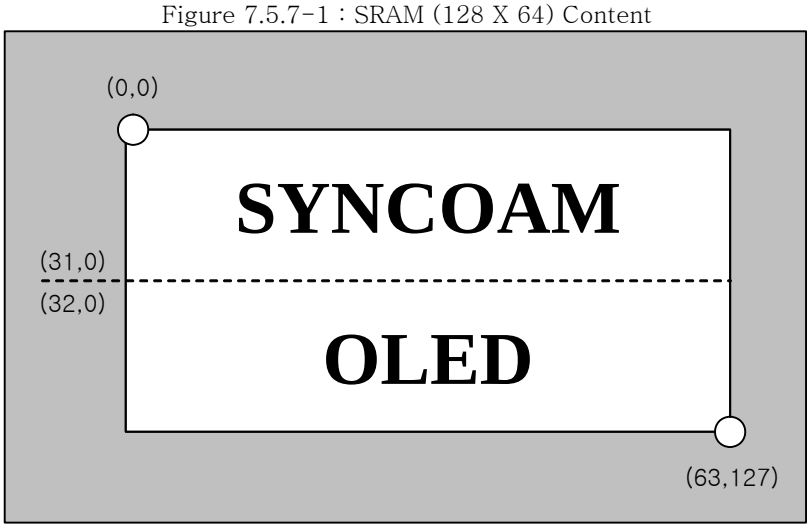
Figure 7.5.6-1 : Iref resistor Selection by register R72h

7.5.7 Display Control Register Setting and SRAM Content

Figure 7.5.6-1 : Display Control Register Setting

SM (Bin)	GS (Bin)	SS (Bin)	SCN (Hex)	NL (Hex)	SS1 (Hex)	SE1 (Hex)
0	1	0	00	3F	00	3F

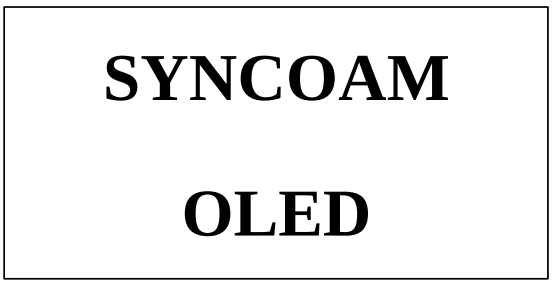
Figure 7.5.7-1 : SRAM (128 X 64) Content



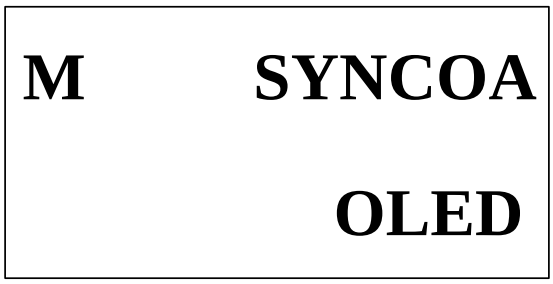
7.5.8 Horizontal Moving (Right Panning)

SSLP (Bin)	SSON (Bin)	SSST (Hex)	SSUT (Hex)	SSUD (Bin)	SSLR (Bin)	SSSV (Hex)	SSSH (Hex)
0	1	X	5	X	1	0	20

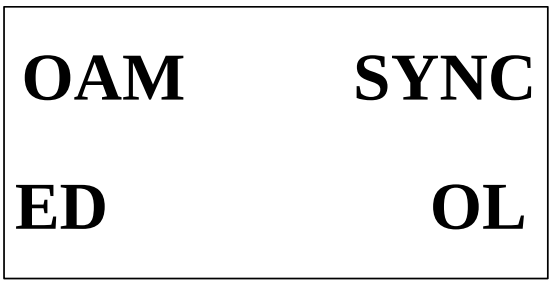
Figure 7.5.8-1 : Screen Saver Mode Register Setting



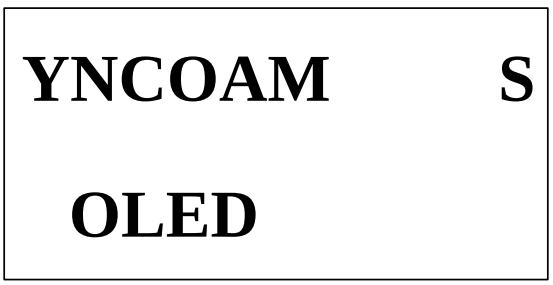
VSYNC = 1 Frame



VSYNC = 7 Frame



VSYNC = 13 Frame



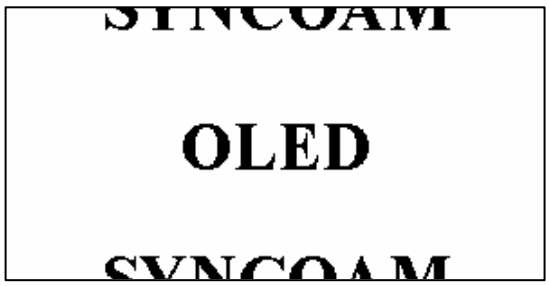
VSYNC = 19 Frame

7.5.9 Vertical Moving (Up Scroll)

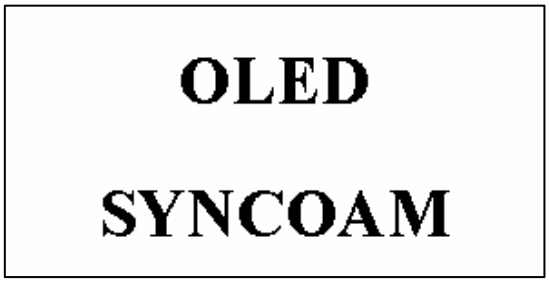
SSLP (Bin)	SSON (Bin)	SSST (Hex)	SSUT (Hex)	SSUD (Bin)	SSLR (Bin)	SSSV (Hex)	SSSH (Hex)
0	1	X	5	0	X	10	0

Figure 7.5.9-1 : Screen Saver Mode Register Setting

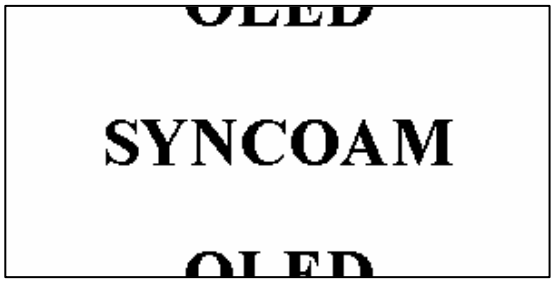
VSYNC = 1 Frame



VSYNC = 7 Frame



VSYNC = 13 Frame

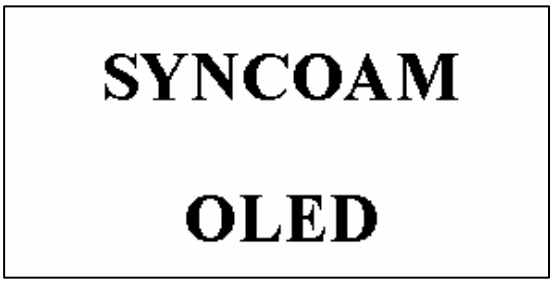


VSYNC = 19 Frame

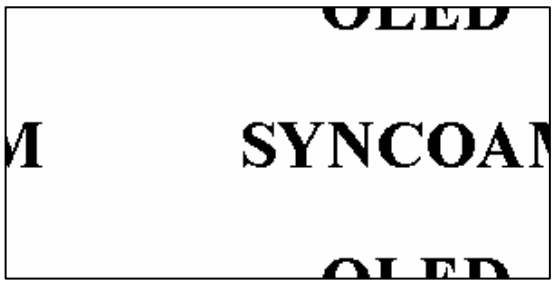
7.5.10 Horizontal and Vertical Moving (Right Panning and Down Scroll)

SSLP (Bin)	SSON (Bin)	SSST (Hex)	SSUT (Hex)	SSUD (Bin)	SSLR (Bin)	SSSV (Hex)	SSSH (Hex)
0	1	X	5	1	1	10	20

Figure 7.5.10-1 : Screen Saver Mode Register Setting

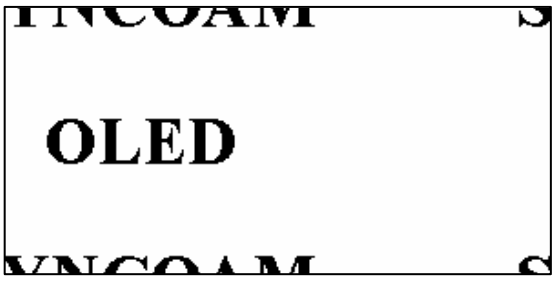


VSYNC = 1 Frame



VSYNC = 7 Frame

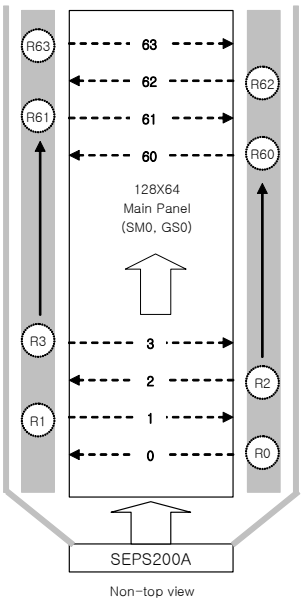
VSYNC = 13 Frame

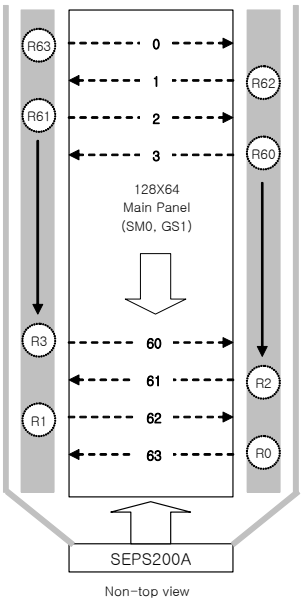


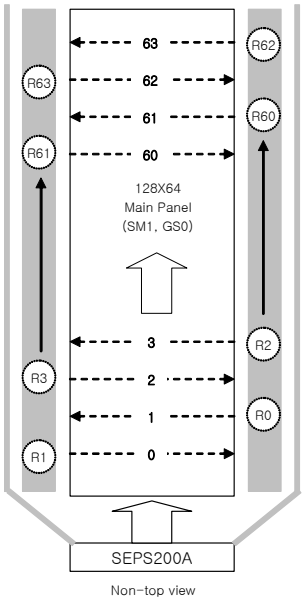
VSYNC = 19 Frame

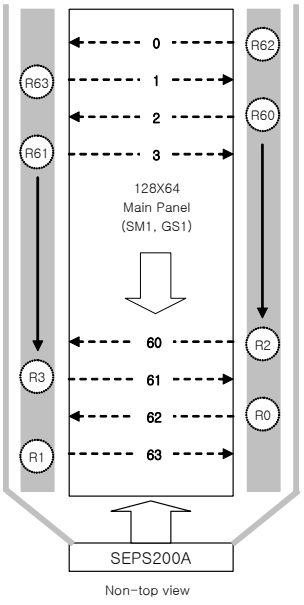
8. Graphic Command Setting

8.1 Scan Mode Setting (GS, SM)

<table>
<tr><th></th><th>GS = ‘0’</th><th>GS = ‘1’</th></tr>
<tr><td>SM = ‘0’</td><td> 

Scan order (Gate line NO.)
R0 => R1 => R2 => R3 => …
R60 => R61 => R62 => R63</td><td> 

Scan order (Gate line NO.)
R63 => R62 => R61 => R60 => …
R3 => R2 => R1 => R0</td></tr>
<tr><td>SM = ‘1’</td><td> 

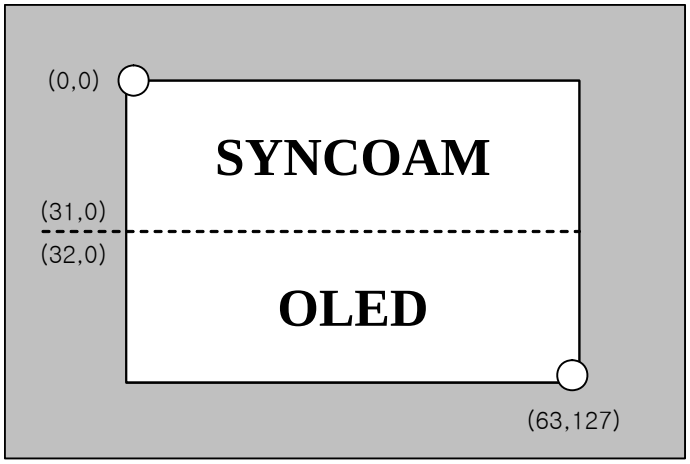
Scan order (Gate line NO.)
R1 => R0 => R3 => R2 => …
R61 => R60 => R63 => R62</td><td> 

Scan order (Gate line NO.)
R62 => R63 => R60 => R61 => …
R2 => R3 => R0 => RG1</td></tr>
</table>

Note : The numbers in an arrows in figure shows order of scan.

8.2 Display Control Setting (SM, GS, SS, SCN, NL, SS1, SE1, VL)

Figure 8.2-1 : SRAM (128 X 64) Content



	Sub Category	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
02h	Driver Output Control 1			NL5 (1)	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (1)	NL0 (1)
03h	Driver Output Control 2						SM (0)	GS (0)	SS (0)
30h	Row Scan Start			SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
31h	Vertical Scroll Control			VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
32h	Screen Start Drive Position			SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)
33h	Screen End Drive Position			SE15 (1)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)

8.2.1 Set Window Area

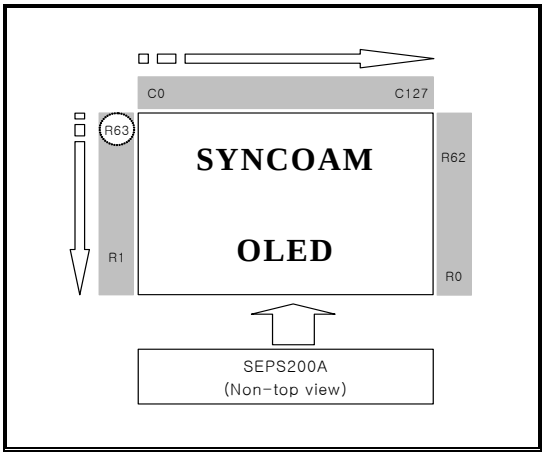


Figure 8.2.1-1 : Full Screen Mode

Example1 : Setting full screen

SM (Bin)	GS (Bin)	SS (Bin)	SCN (Hex)	NL (Hex)	SS1 (Hex)	SE1 (Hex)
0	1	0	00	3F	00	3F

Support 128 x 64 dot MONO matrix panel
Row direction order : R63, R62 ... R1, R0
Column direction order : C0, C1 ... C126, C127

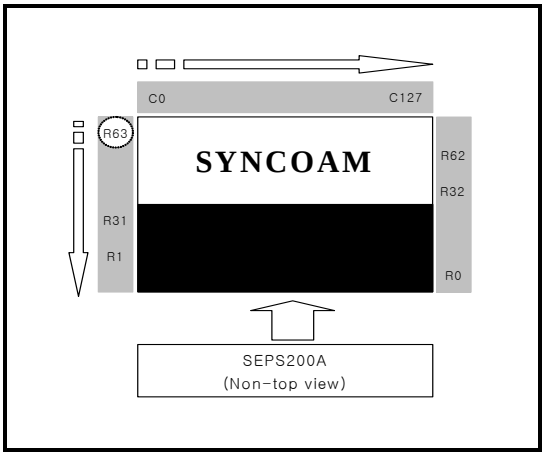


Figure 8.2.1-2 : Setting Screen range

Example2 : Setting position of start and end lines for screen

SM (Bin)	GS (Bin)	SS (Bin)	SCN (Hex)	NL (Hex)	SS1 (Hex)	SE1 (Hex)
0	1	0	00	3F	00	1F

Support 128 x 64 dot MONO matrix panel
Row direction order : R63, R62 ... R1, R0
Column direction order : C0, C1 ... C126, C127

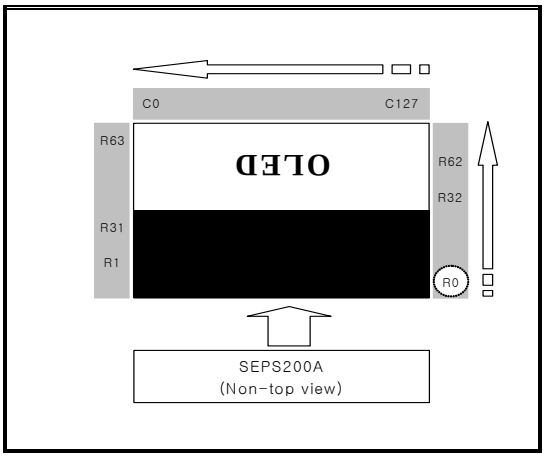


Figure 8.2.1-3 : Setting Screen range

Example3 : Setting position of start and end lines for screen

SM (Bin)	GS (Bin)	SS (Bin)	SCN (Hex)	NL (Hex)	SS1 (Hex)	SE1 (Hex)
0	0	1	00	3F	20	3F

Support 128 x 64 dot MONO matrix panel
Row direction order : R0, R1 ... R62, R63
Column direction order : C127, C126 ... C1, C0

8.2.2 Set Gate Scan Position

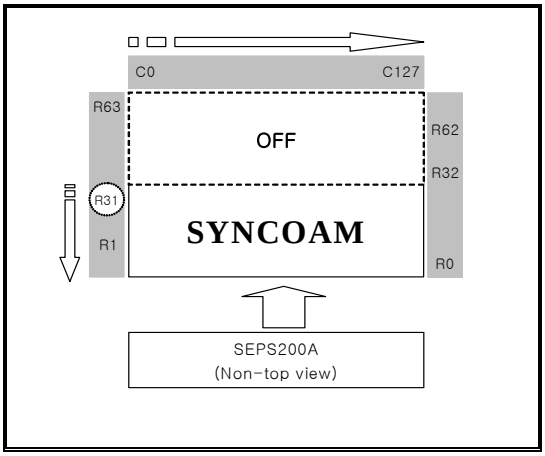


Figure 8.2.2-1 : Setting Gate Scan Position

Example1 : Setting position of start line for gate scan

SM (Bin)	GS (Bin)	SS (Bin)	SCN (Hex)	NL (Hex)	SS1 (Hex)	SE1 (Hex)
0	1	0	20	1F	00	1F

Support 128 x 32 dot MONO matrix panel
Row direction order : R31, R30 ... R1, R0
Column direction order : C0, C1 ... C126, C127

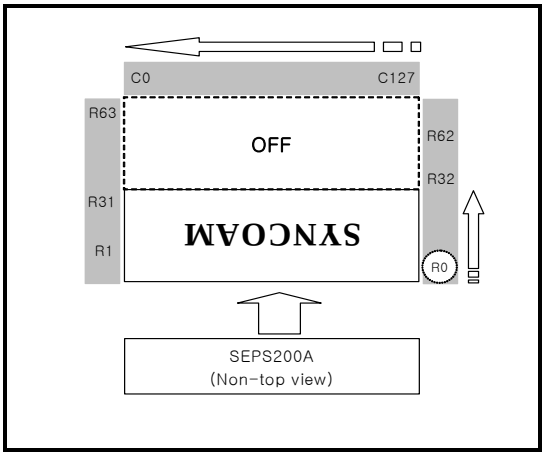


Figure 8.2.2-2 : Setting Gate Scan Position

Example2 : Setting position of start line for gate scan

SM (Bin)	GS (Bin)	SS (Bin)	SCN (Hex)	NL (Hex)	SS1 (Hex)	SE1 (Hex)
0	0	1	00	1F	00	1F

Support 128 x 32 dot MONO matrix panel
Row direction order : R0, R1 ... R30, R31
Column direction order : C127, C126 ... C1, C0

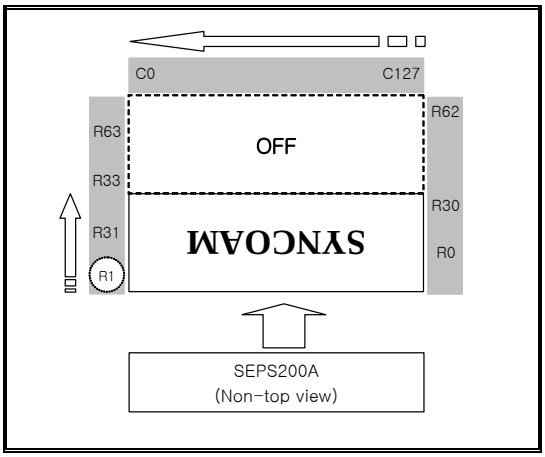


Figure 8.2.2-3 : Setting Gate Scan Position

Example3 : Setting position of start line for gate scan

SM (Bin)	GS (Bin)	SS (Bin)	SCN (Hex)	NL (Hex)	SS1 (Hex)	SE1 (Hex)
1	0	1	00	1F	00	1F

Support 128 x 32 dot MONO matrix panel
Row direction order : R1, R0 ... R31, R30
Column direction order : C127, C126 ... C1, C0

8.2.3 Set Vertical Scroll Area

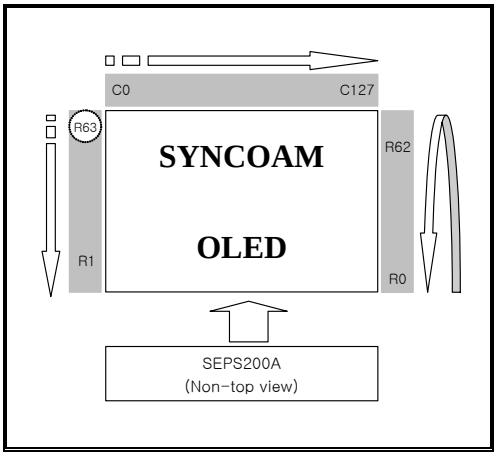


Figure 8.2.3-1 : Before Scrolling

Example1 : Display before vertical scrolling start

SM (Bin)	GS (Bin)	SS (Bin)	SCN (Hex)	NL (Hex)	SS1 (Hex)	SE1 (Hex)	VL (Hex)
0	0	1	00	1F	00	1F	00

Support 128 x 64 dot MONO matrix panel
Row direction order : R63 => R62 ... R1 => R0
Column direction order : C0 => C1 ... C126 => C127

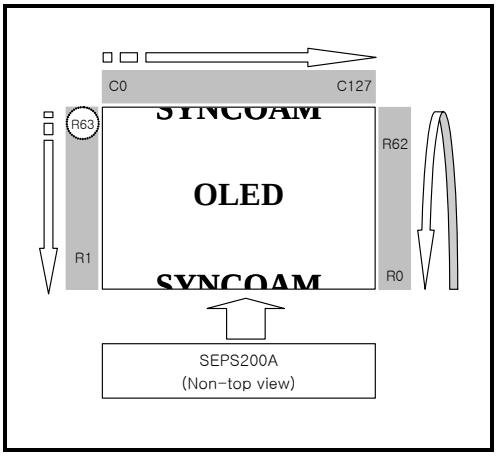


Figure 8.2.3-2 : Vertical Scrolling 16

Example2 : Full screen vertical scrolling 16 row up

SM (Bin)	GS (Bin)	SS (Bin)	SCN (Hex)	NL (Hex)	SS1 (Hex)	SE1 (Hex)	VL (Hex)
0	0	1	00	1F	00	1F	10

Support 128 x 64 dot MONO matrix panel
Row direction order : R63 => R62 ... R1 => R0
Column direction order : C0 => C1 ... C126 => C127

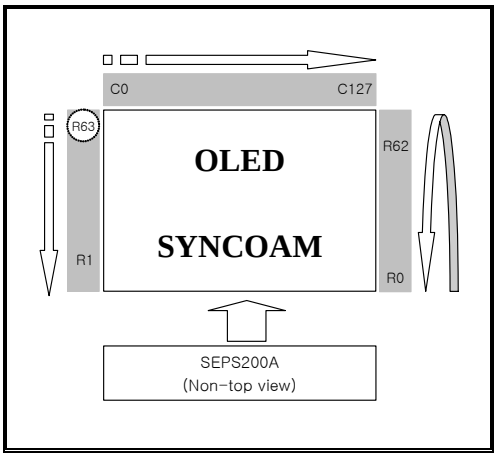


Figure 8.2.3-3 : Vertical Scrolling 32

Example3 : Full screen vertical scrolling 32 row up

SM (Bin)	GS (Bin)	SS (Bin)	SCN (Hex)	NL (Hex)	SS1 (Hex)	SE1 (Hex)	VL (Hex)
0	0	1	00	1F	00	1F	20

Support 128 x 64 dot MONO matrix panel
Row direction order : R63 => R62 ... R1 => R0
Column direction order : C0 => C1 ... C126 => C127

9. DC CHARACTERISTICS

9.1 Absolute Maximum Rating

ITEM	SYMBOL	PORT	RATINGS	UNIT
Supply voltage	VDD	VDD	- 0.3 ~ + 4.0	V
	VCC	VCC	0 ~ 18	V
Input voltage	V_{IN}	*1	- 0.3 ~ + VDD+ 0.3	V
Storage temperature	Tstg		- 65 ~ + 150	℃

*1: DB[7:0], IM[2:0], CSB, A0, RDB, WRB, RSTB.

9.2 Recommended Operation Conditions

ITEM	SYMBOL	PORT	MIN	TYP	MAX	UNIT	REMARK
Supply voltage	VDD	VDD	1.6	2.8	3.6	V	
	VCC	VCC	7.0	16	18.0	V	
Operation temperature	Topr				125	℃	

9.3 DC Characteristics

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	PORT
High level input voltage	VIH		0.8XVDD		VDD	V	
Low level input voltage	VIL		0		0.2xVDD	V	
High level output voltage	VOH	IOH = -0.1mA	0.8XVDD			V	
Low level output voltage	VOL	IOL = -0.1mA	0		0.2xVDD	V	
Input leakage current	ILI	VI = VSS or VDD	-1		1	uA	
Output leakage current	ILO	VI = VSS or VDD	-1		1	uA	
Standby	ISB	VDD = 2.8V, VCC = 16V Ta = 25℃, Power save mode			5	uA	
Operating current	IVDD	VDD = 2.8V, VCC = 16V Idrv = 255 uA,Ipre = 1020uA Without Panel, 20kΩ load, display on		TBD	500	uA	
	IVCC			TBD	37	mA	
Oscillator frequency	FSOCE	VDD = 2.8V, Ta = 25℃		470		KHz	
Oscillator frequency match	FOSCV	VDD = 2.8V, Ta = 25℃		±5		%	
Frame scan rate	Frame	VDD = 2.8V, Ta = 25℃	65	90	120	Hz	
Column output current range	IDC	4 < VDC < VCC -2V	0		255	uA	
Column output current uniformity	Within chip	VDD = 2.8V, VCC = 16V Idrv = 100 uA, Ipre = 100uA Without Panel, 20kΩ load, display on	-4.0		+ 4.0	%	
	Pin to pin		-2.0		+ 2.0	%	
Row switch on current sink	IDR	Common is on Idrv = 255uA		33		mA	
Row switch on resistance	Ron	Common is on IFM = 33mA		52		Ω	

10. AC CHARACTERISTICS

10.1 System BUS Read/Write Timing (80 series CPU interface)

10.1.1 Write Cycle

Figure 10.1.1-1 : 8080-Series Parallel Interface Characteristics

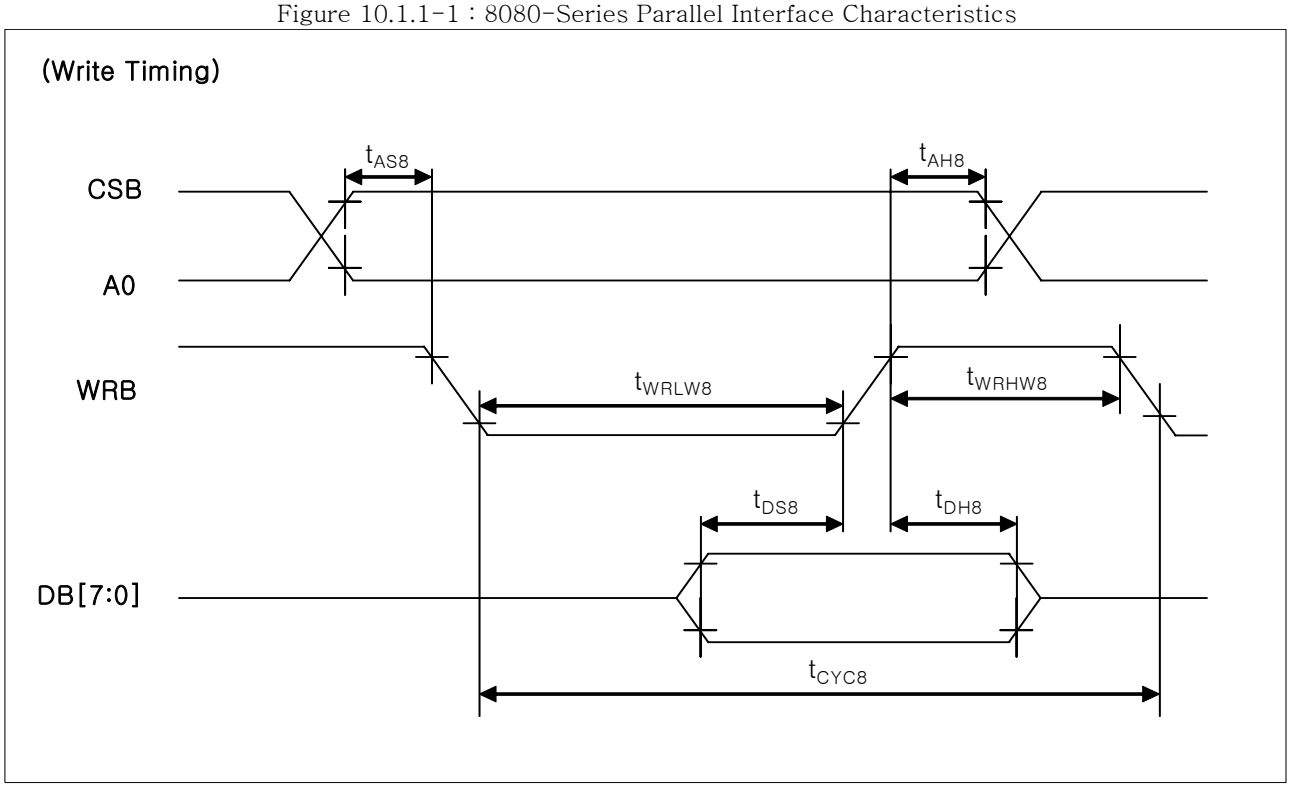


Table 10.1.1-1 : 8080-Series MCU Parallel Interface Timing Characteristics

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold time	t_{AH8}	-	5	-	ns	CSB
Address setup time	t_{AS8}		5		ns	A0
System cycle time	t_{CYC8}	-	100	-	ns	WRB
Write "L" pulse width	t_{WRLW8}		45		ns	
Write "H" pulse width	t_{WRHW8}		45		ns	
Data setup time	t_{DS8}	-	30	-	ns	DB[7:0]
Data hold time	t_{DH8}		10		ns	

(VDD = 2.8V, Ta = 25℃)

10.1.2 Read Cycle

Figure 10.1.2-1 : 8080-Series Parallel Interface Characteristics

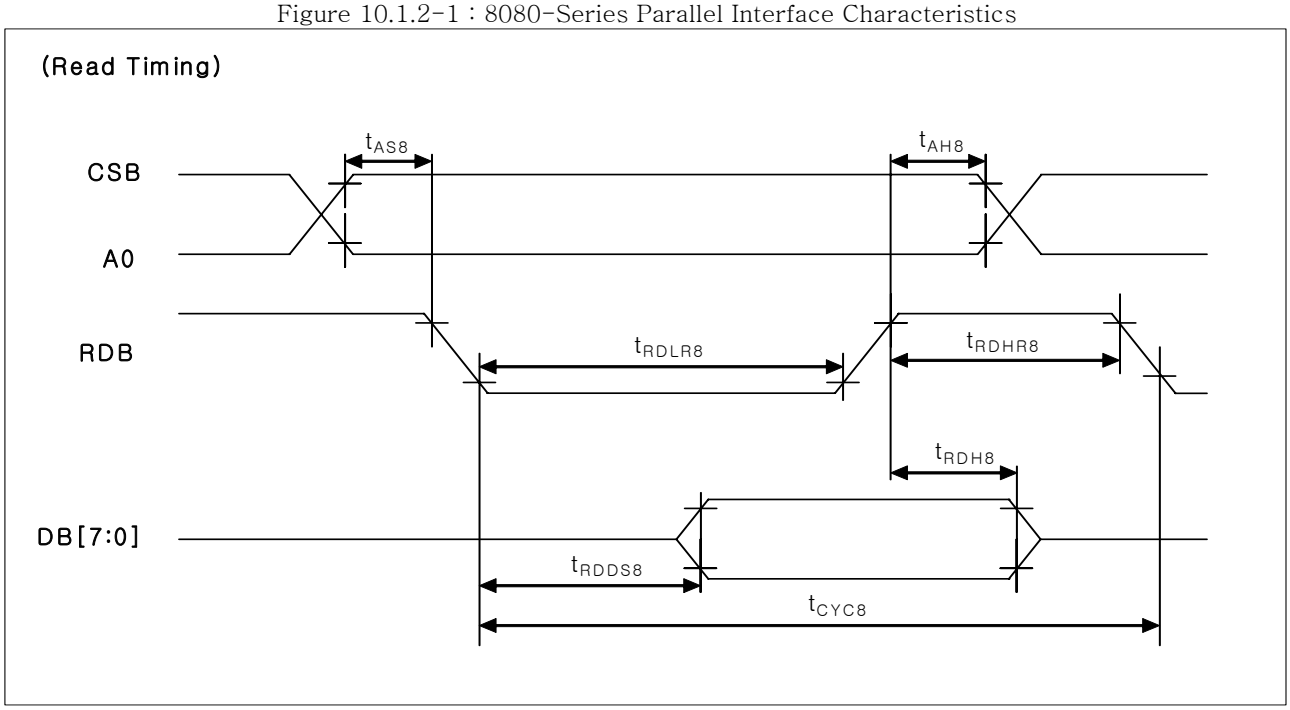


Table 10.1.2-1 : 8080-Series MCU Parallel Interface Timing Characteristics

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold time Address setup time	t_{AH8} t_{AS8}	-	5 5	-	ns ns	CSB A0
System cycle time Read “L” pulse width Read “H” pulse width	t_{CYC8} t_{RDLR8} t_{RDHR8}	-	200 90 90	-	ns ns ns	RDB
Output data delay time Data hold time	t_{RDD8} t_{RDH8}	CL = 15 pF	- 20	80 -	ns ns	DB[7:0]

(VDD = 2.8V, Ta = 25℃)

10.2 System BUS Read/Write Timing (68 series CPU interface)

10.2.1 Write Cycle

Figure 10.2.1-1 : 6800-Series Parallel Interface Characteristics:

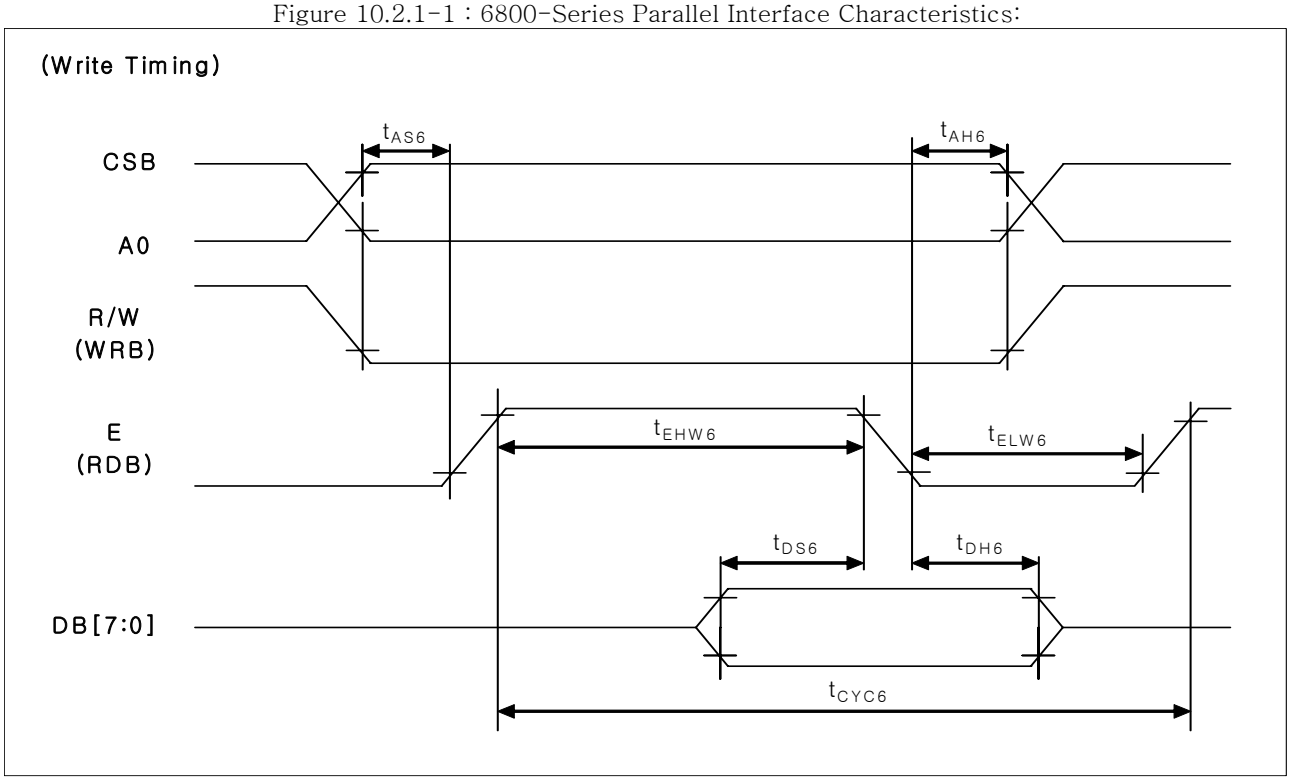


Table 10.2.1-1 : 6800-Series MCU Parallel Interface Timing Characteristics

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold time Address setup time	t_{AH6} t_{AS6}	-	5 5	-	ns ns	CSB RS
System cycle time Write "L" pulse width Write "H" pulse width	t_{CYC6} t_{ELW6} t_{EHW6}	-	100 45 45	-	ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}	-	30 10	-	ns ns	DB[7:0]

(VDD = 2.8V, Ta = 25℃)

10.2.2 Read Cycle

Figure 10.2.2-1 : 6800-Series Parallel Interface Characteristics

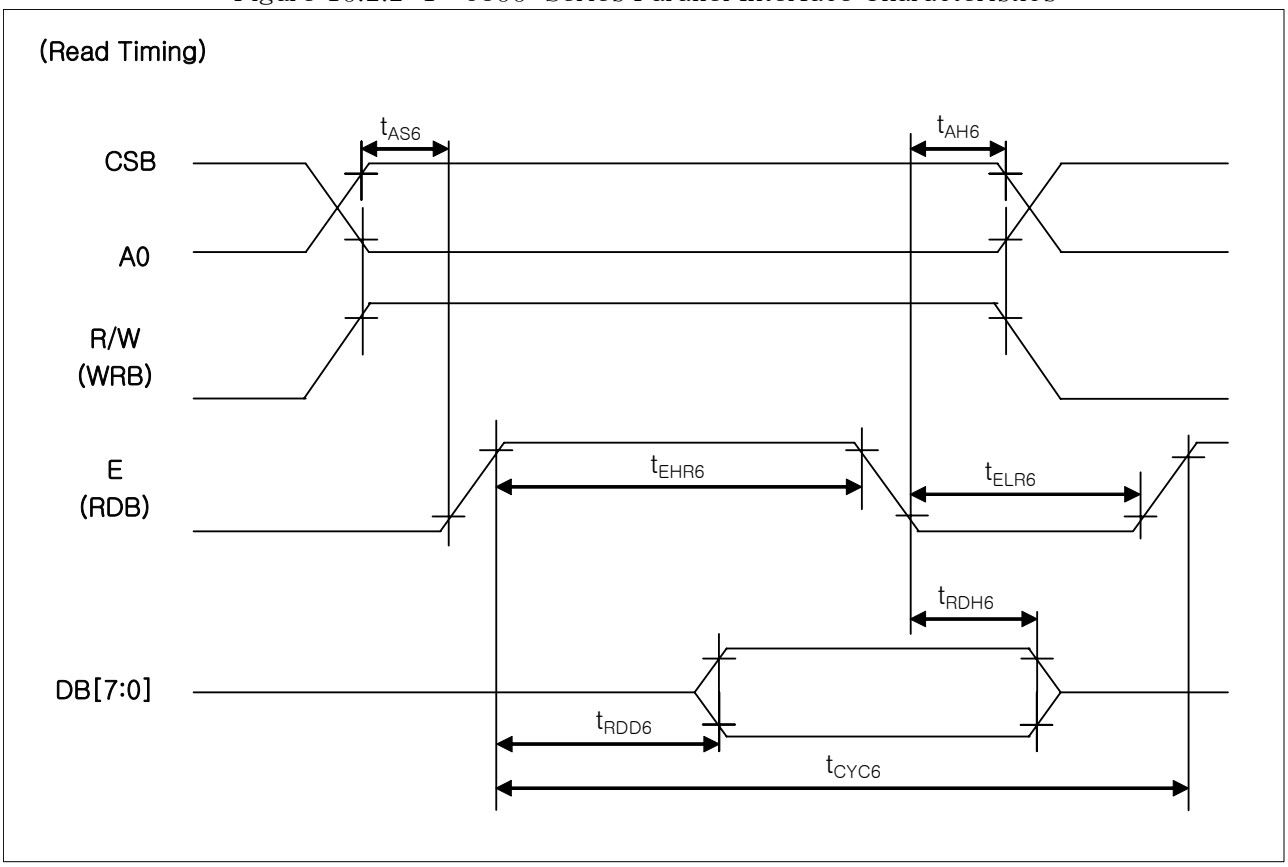


Table 10.2.2-1 : 6800-Series MCU Parallel Interface Timing Characteristics

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold time Address setup time	t_{AH6} t_{AS6}	-	10 10	-	ns ns	CSB A0
System cycle time Read “L” pulse width Read “H” pulse width	t_{CYC6} t_{ELR6} t_{EHR6}	-	200 90 90	-	ns ns ns	E
Output data delay time Data hold time	t_{RDD6} t_{RDH6}	CL = 15 pF	- 20	80 -	ns ns	DB[7:0]

(VDD = 2.8V, Ta = 25℃)

10.3 Serial Peripheral Interface Timing

Figure 10.3-1 : Serial Interface Characteristics

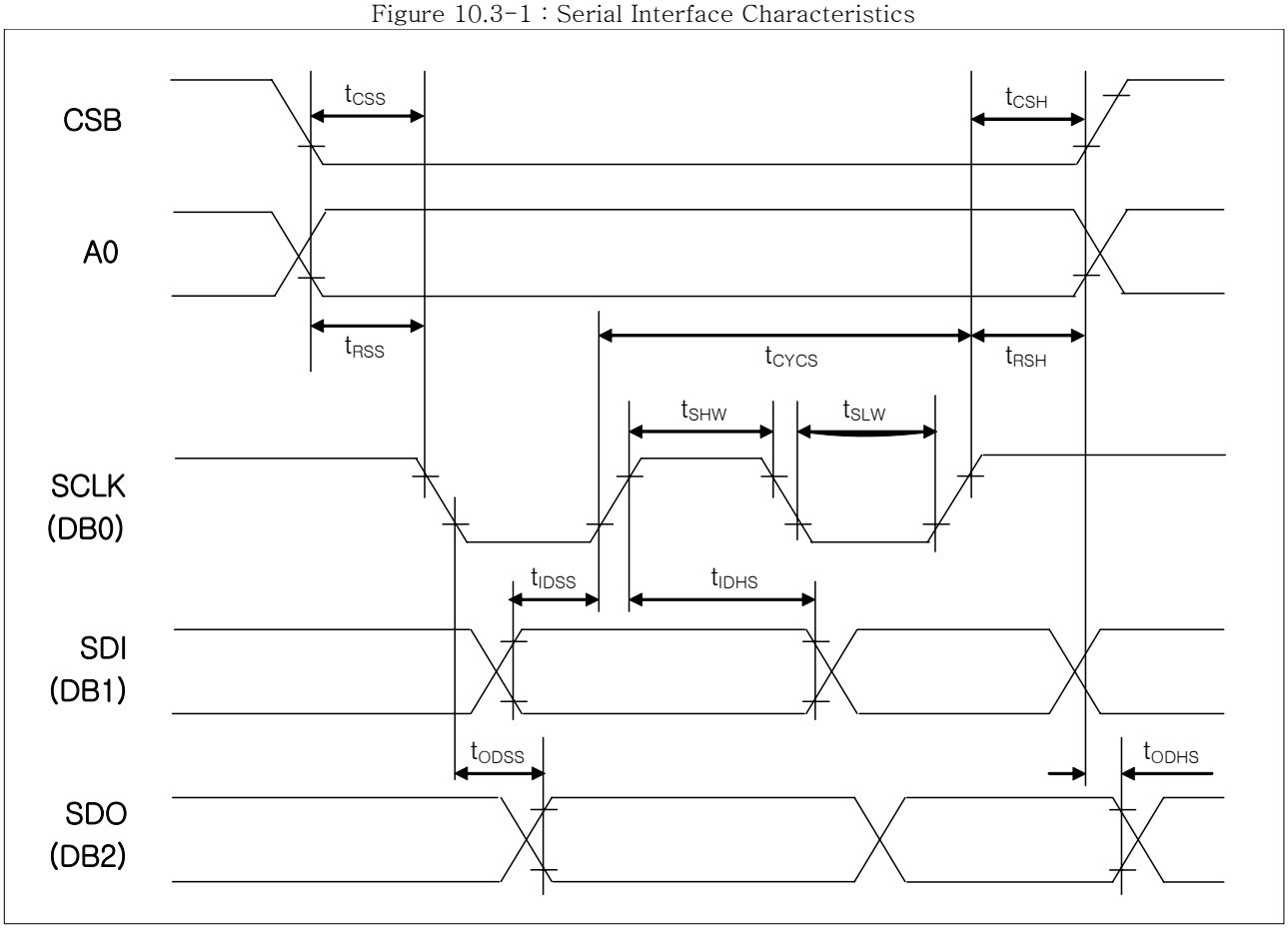


Table 10.3-1 : Serial Interface Timing Characteristics

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
CSB-setup time CSB-hold time	t_{CSS} t_{CSH}	-	5 5	-	ns ns	CSB
A0-setup time A0-hold time	T_{RSS} T_{RSH}	-	5 5	-	ns ns	A0
Serial clock cycle SCL “L” pulse width SCL “H” pulse width	t_{CYCS} t_{SLW} t_{SHW}	-	200 90 90	-	ns ns ns	SCLK (DB0)
Input data setup time Input data hold time	t_{IDSS} t_{IDHS}	-	5 5	-	ns ns	SDI (DB1)
Output data delay time Output data hold time	t_{ODSS} t_{ODHS}	-	5 5	-	ns ns	SDO (DB2)

(VDD = 2.8V, Ta = 25℃)

10.4 I²C Interface Timing

Figure 10.4-1 : I²C Interface Characteristics

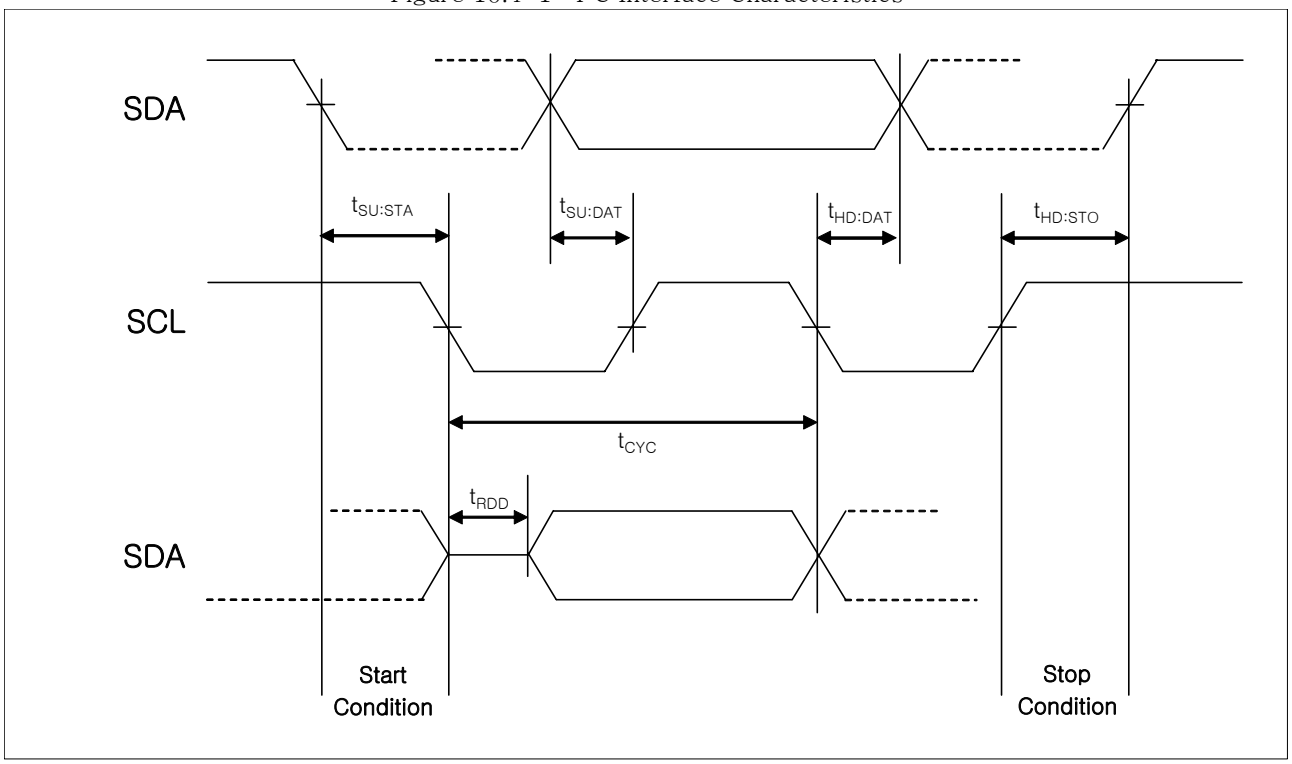


Table 10.4-1 : I²C Interface Timing Characteristics

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
I²C clock cycle	t_{CYC}	-	-	400	kHz	SCL
Stop condition setup time Start condition hold time	$t_{SU:STO}$ $t_{HD:STA}$	-	600 600	- -	ns ns	SDA
Input data setup time Input data hold time	$t_{SU:DAT}$ $t_{HD:DAT}$	-	100 -	- 900	ns ns	SDA(IN)
Output data delay time	t_{RDD}	-	50	-	ns	SDA(OUT)

(VDD = 2.8V, Ta = 25℃)

10.5 Reset Input Timing

Figure 10.5-1 : Reset Input Characteristics

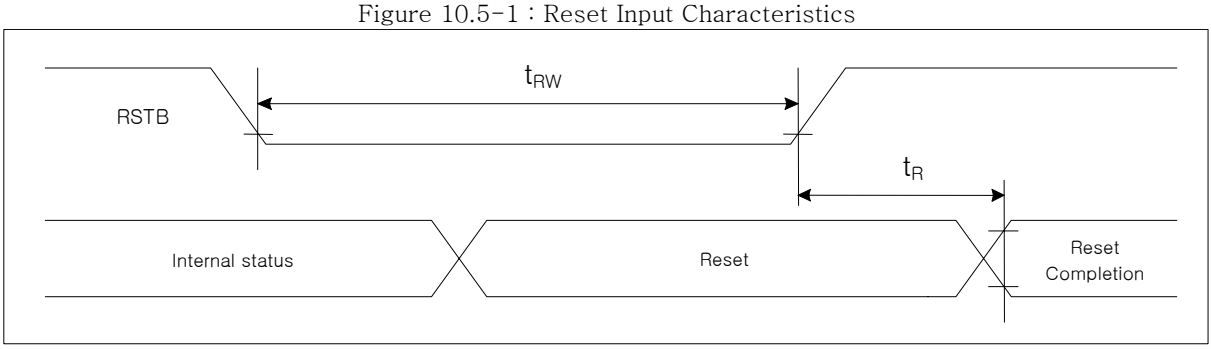


Table 10.5-1 : Reset Input Timing Characteristics

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Reset time	t_R			1.5	us	
RSTB "L" pulse width	t_{RW}		5		us	RSTB

(VDD = 2.8V, Ta = 25℃)

11. Data Sheet Revision History

Version	Content	Date
0.9	First issue	2008.07.15
1.0	1. Change pin name : RES -> RSTB 2. Command Description : R05h, R06h, R14h 3. OSC information	2008.08.28
1.1	1. Change Pin Description (page 3) (DB, OSC1, OSC2, IREF, VSS, VSSL, VSSH) 2. Change Block Diagram (VDD, VSS, VSSL) 3. Add New page - Graphic Display Data RAM (page 14) - Power On and OFF sequence (page 15) - Stand BY Mode ON/OFF sequence (page 16)	2008.11.17
1.11	1. Saver Mode (page 40) - SSUD and SSLR Change	2009.01.06
1.2	1. Read Cycle 6800-system (page 55) - Figure 10.2.2-1 modify 2. Serial Peripheral Interface Timing (page 56) - Figure 10.3-1 modify 3. Add New Page - I2C Interface(page 57) 4. Power On and OFF sequence (page 15) 5. Iref Resistor Selection (page 42)	2009.03.02