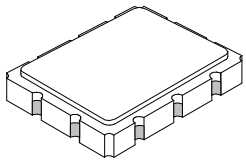
SF1082A

125.000 MHz SAW Filter

- ***Designed for GSM BTS Transmitter Applications***
- ***Low Insertion Loss***
- ***9.1 x 7.1 mm Surface-Mount Case***
- ***Unbalanced Input and Output***
- ***Complies with Directive 2002/95/EC (RoHS)***



SM9171-10

Absolute Maximum Ratings

Rating	Value	Units
Maximum Incident Power in Passband	+10	dBm
Max. DC voltage between any 2 terminals	30	VDC
Storage Temperature Range	-40 to +85	°C
Suitable for lead-free soldering - Max Soldering Profile	260°C for 30 s	

Electrical Characteristics

Characteristic		Sym	Notes	Min	Typ	Max	Units
Nominal Center Frequency		f_C	1		125.000		MHz
Passband	Insertion Loss at fc	IL			6.0	8.0	dB
	3 dB Passband	BW_3	1, 2	±275	±440		kHz
	Amplitude Ripple over fc ±75 kHz					0.3	dB_{P-P}
	Group Delay Variation over fc±75 kHz	GDV				100	ns_{P-P}
Rejection	fc-7.5 to fc-6.0 and fc+6.0 to fc+7.5 MHz		1, 2, 3	20	40		dB
	Ultimate				>40		
Operating Temperature Range		T_A	1	-40		+85	°C

Impedance Matching to 50 Ω unbalanced	External L-C
Case Style	SM9171-10 9.1 x 7.1 mm Nominal Footprint
Lid Symbolization (XX = 2 character date code)	RFM SF1082A XX

Electrical Connections

Connection	Terminals
Port 1 Hot	1
Port 1 Gnd Return	4
Port 2 Hot	6
Port 2 Gnd Return	9
Case Ground	All others

Notes:

1. Unless noted otherwise, all specitication apply over the operating temperature range with filter soldered to the specified demonstration board with impedanced matching to 50 Ω network analyzer.
2. Unless noted otherwise, all frequency specitications are referenced to the nominal center frequency, fc.
3. Rejection is measured as attenuation below the minimum IL point in the passband. Rejection in final user application is dependent on PCB layout and external impedance matching design. See Application Note No. 42 for details.
4. "LRIP" or "L" after the part number indicates "low rate initial production" and "ENG" or "E" indicates "engineering prototypes."
5. The design, manufacturing process, and specifications of this filter are subject to change.
6. Either Port 1 or Port 2 may be used for either input or output in the design. However, impedances and impedance matching may vary between Port 1 and Port 2, so that the filter must always be installed in one direction per the circuit design.
7. US and international patents may apply.
8. RFM, stylized RFM logo, and RF Monolithics, Inc. are registered trademarks of RF Monolithics, Inc.
9. Electrostatic Sensitive Device. Observe precautions for handling.

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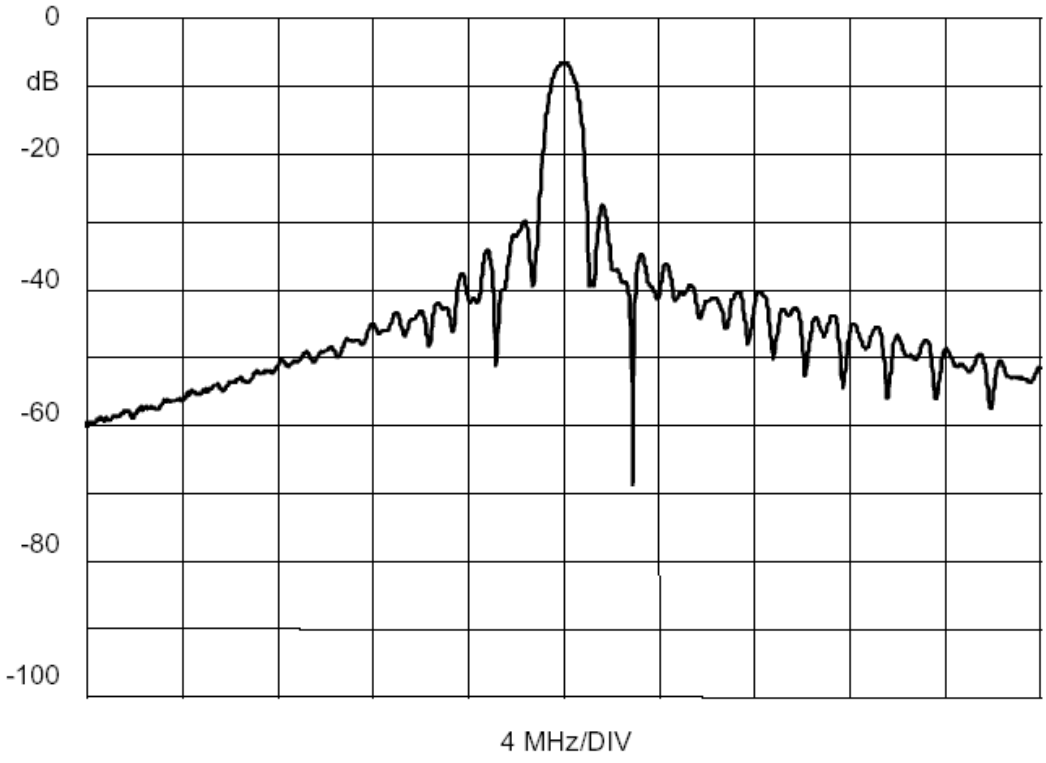
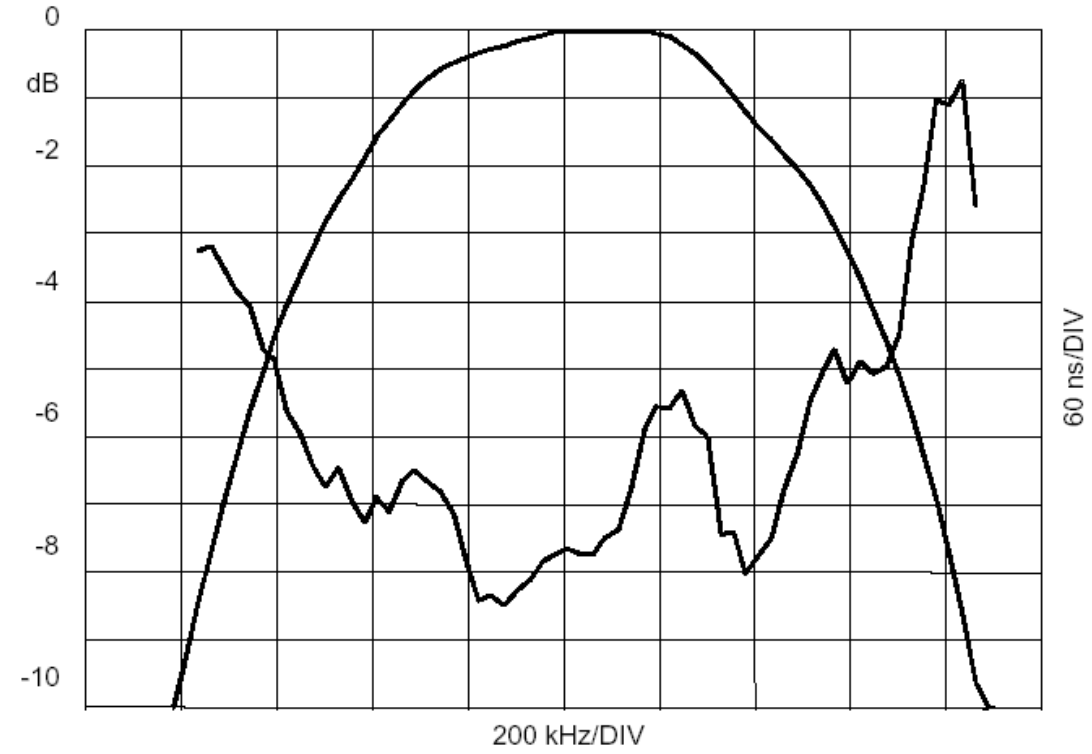
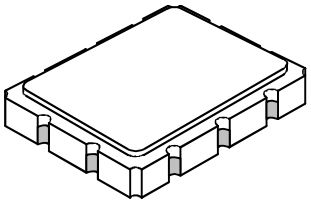




SM9171-10 Case

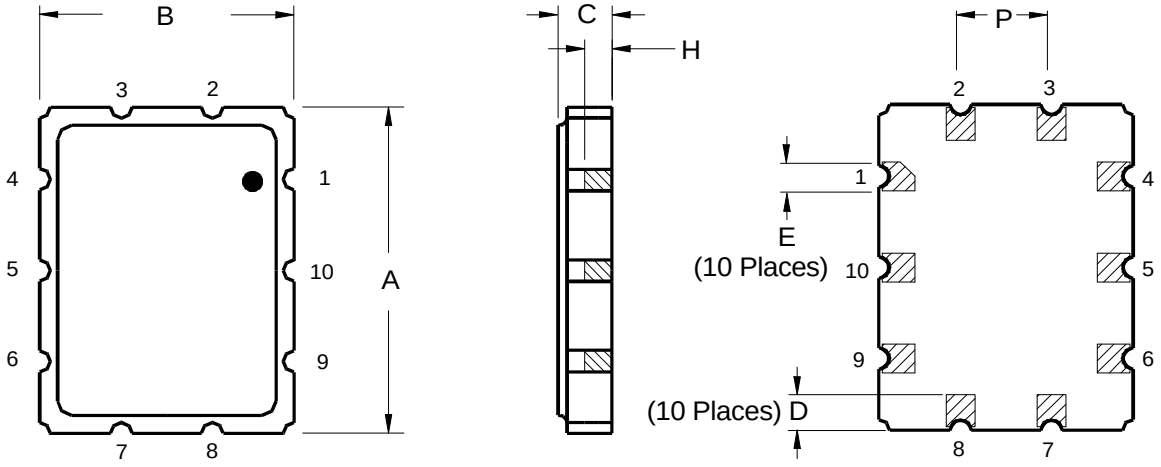
10-Terminal Ceramic Surface-Mount Case
9.1 x 7.1 mm Nominal Footprint



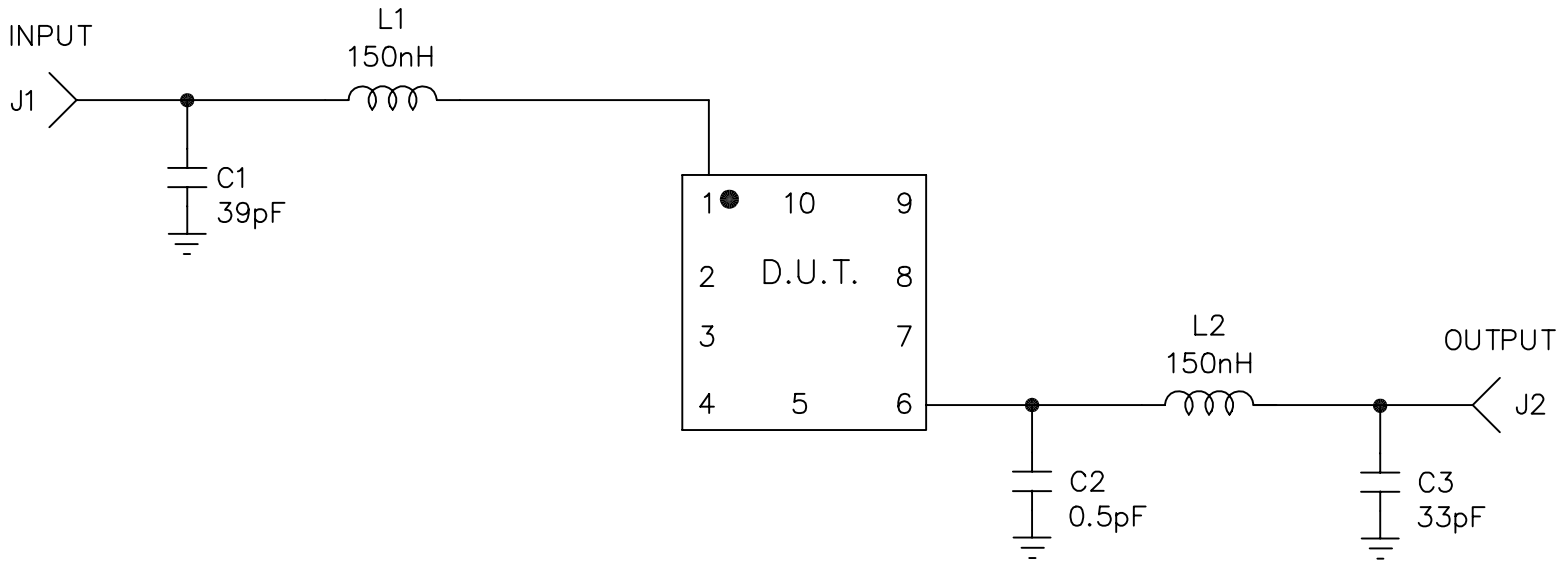
Case Dimensions						
Dimension	mm			Inches		
	Min	Nom	Max	Min	Nom	Max
A	8.86	9.09	9.40	0.349	0.358	0.370
B	6.88	7.11	7.40	0.271	0.280	0.291
C		1.91	2.00		0.075	0.079
D		0.99			0.039	
E		0.79			0.031	
H		1.0			0.039	
P		2.54			0.100	

Materials	
Solder Pad Termination	Au plating 30 - 60 µinches (76.2-152 µm) over 80-200 µinches (203-508 µm) Ni.
Lid	Fe-Ni-Co Alloy Electroless Nickel Plate (8-11% Phosphorus) 100-200 µinches Thick
Body	Al_2O_3 Ceramic
Pb Free	

Electrical Connections		
Connection		Terminals
Port 1	Input or Return	6
	Return or Input	5
Port 2	Output or Return	1
	Return or Output	10
Ground		All others
Single Ended Operation		**Return is ground**
Differential Operation		**Return is hot**



REV	ECN NO.	DESCRIPTION	APP/DATE
A	6254	INITIAL RELEASE	



DRAWN BY/DATE: J.J. LAYTON 01/15/98			TITLE: ASSY DIAGRAM, SF1082A-DEMO					
RF Monolithics, Inc. DALLAS, TEXAS 75244	CHECKED/APPROVED		SIZE **A**	CODE IDENT **2U874**	DWG. NO. SF1082A-000		REV A	SHEET 1/3

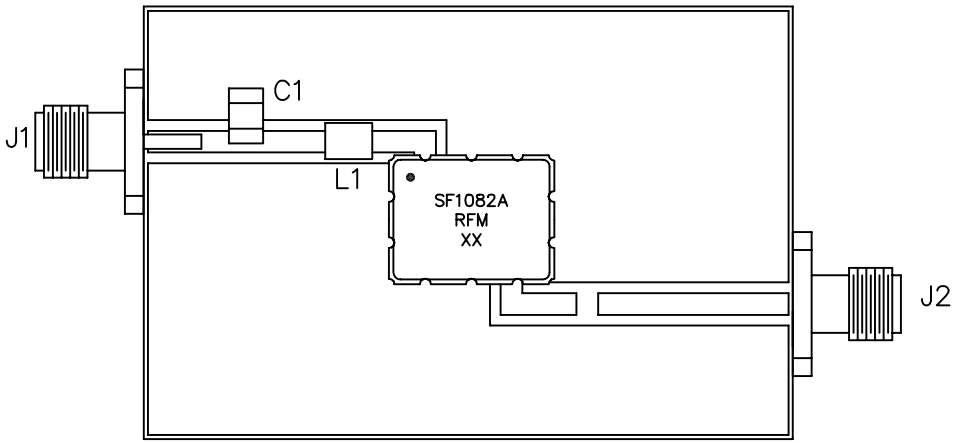
NOTES:

1. SOLDER MOUNT COMPONENTS TO PCB.

2. NOTE PROPER ORIENTATION OF INDUCTORS IS 90° TO EACH OTHER.

3. COMPONENT VALUES MAY NEED TO BE TRADED FOR SLIGHTLY HIGHER OR LOWER VALUES DUE TO TOLERANCE LEVELS OF EACH INDIVIDUAL COMPONENT.

TOP



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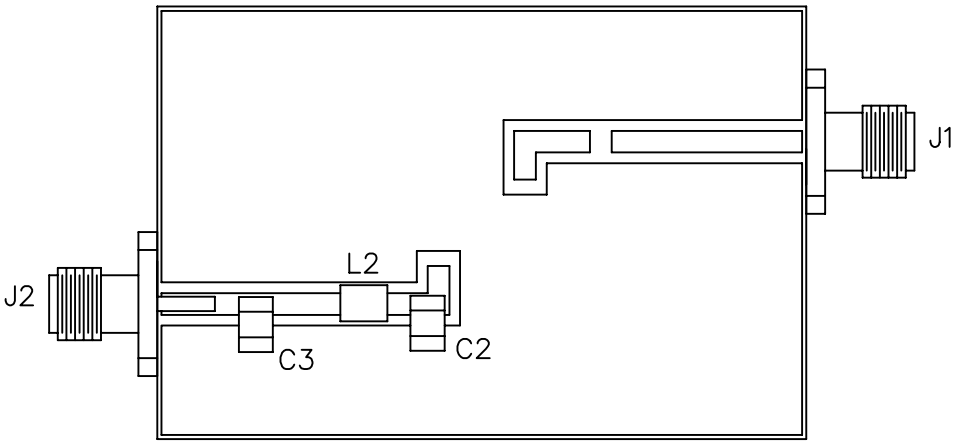
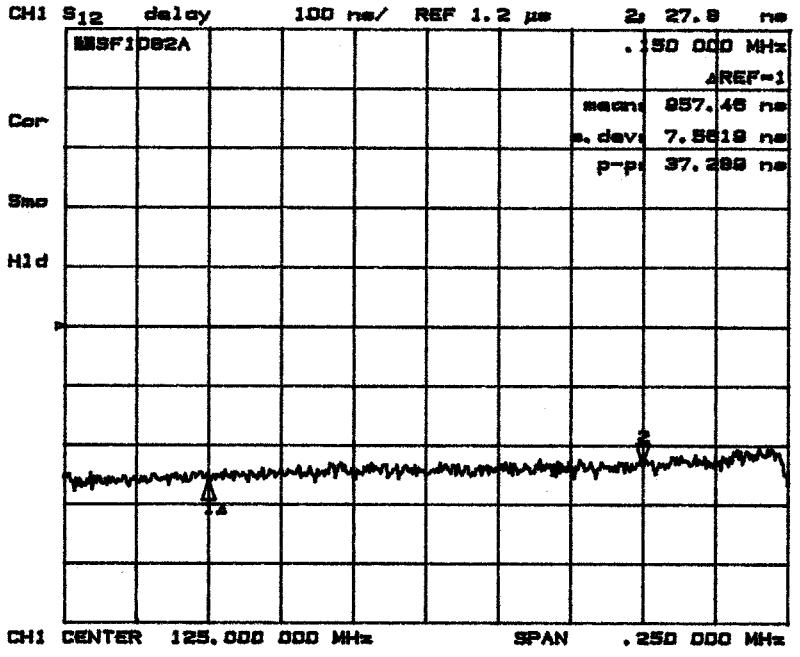
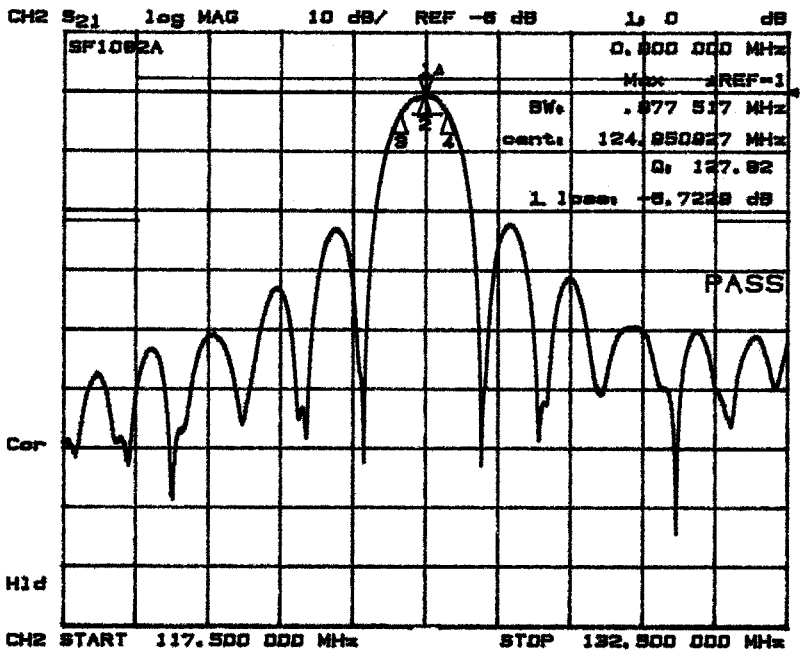
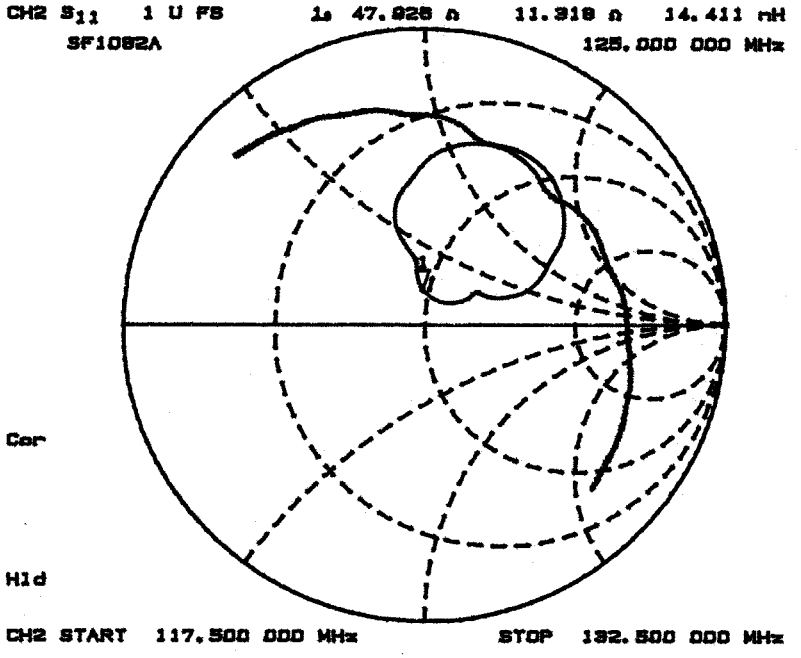


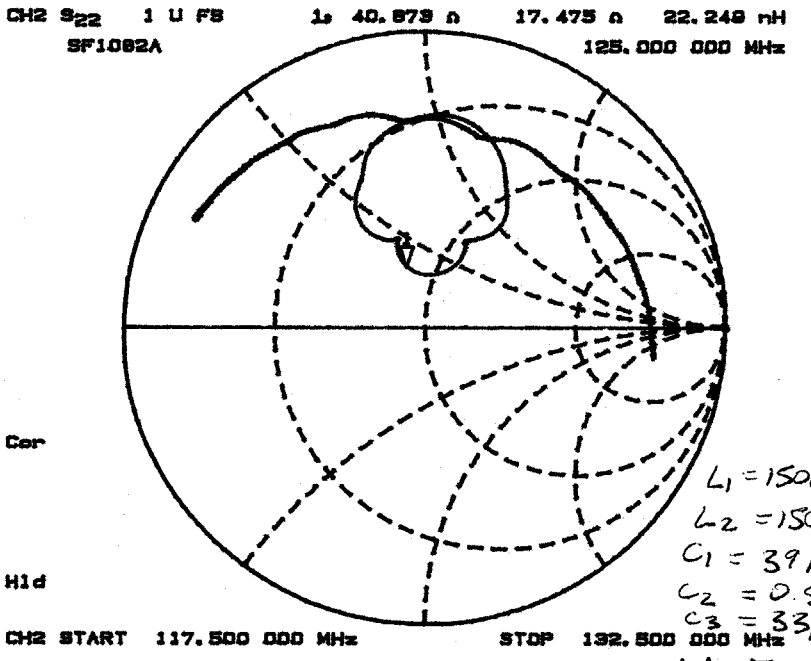
RF Monolithics, Inc. DALLAS, TEXAS 75244		SIZE A	CODE IDENT 2U874	DWG. NO. SF1082A-000	REV A	SHEET 2

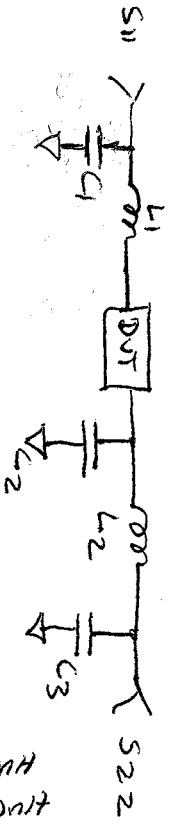
SF1082A:
DEMO
E-3230
Wafer #4
11-12-97
R.CH











$L_1 = 150nH$
$L_2 = 150nH$
$C_1 = 39pF$
$C_2 = 0.5pF$
$C_3 = 33pF$

SF1082-000 REV:A Sht 3 of 3
~~SF1082A(DEMO)~~

BILL OF MATERIALS

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	QTY/ASSY	REFERENCE DESCRIPTION
SF1082A-DEMO	DEMO BOARD,SF1082A			
SF1082A-000	ASSY DIAGRAM,DEMO BOARD,	SF1082A	0	
400-1389-001	PCB,DEMO BD,9 X 7		1.0000	CHAS1
500-0003-390	CAP,CHIP,NPO,39(J),STD		1.0000	C 1
500-0013-005	CAP,CHIP,NPO,0.5(E),STD	0805	1.0000	C 2
500-0003-330	CAP,CHIP,NPO,33(J),STD		1.0000	C 3
500-0583-151	IND,CHIP,0805CS,150NH		2.0000	L 1,2

RFMI	SIZE A	FSCM NO. 2U874	DWG NO. SF1082A-DEMO	
SCALE NONE	W/O or ECN 6254	REV A	SHEET 1 OF 2	

REV HISTORY

REV	ECN	DATE	DESCRIPTION
A	6254	12/17/97	INITIAL RELEASE

FRFM	SIZE A	FSCM NO. 2U874	DWG NO. SF1082A-DEMO	
SCALE NONE	W/O or ECN 6254	REV A	SHEET 2 OF 2	