# High Performance PWM Power Switch Programmable Fsw

## FEATURES

- **Built-in 600V Power MOSFET**
- **Proprietary "Zero OCP/OPP Recovery Gap" Control**
- **Programmable Switching Frequency**
- **Built-in Soft Start Function**
- **All Pins Floating Protection**
- **Very Low Startup Current**
- **High Voltage CMOS Process with Excellent ESD Protection**
- **Frequency Reduction and Burst Mode Control for Energy Saving**
- **Current Mode Control**
- **Built-in Frequency Shuffling**
- **Programmable Switching Frequency**
- **Built-in Synchronous Slope Compensation**
- **Cycle-by-Cycle Current Limiting**
- **Built-in Leading Edge Blanking (LEB)**
- **Constant Power Limiting**
- **Audio Noise Free Operation**
- **VDD OVP & Clamp**
- **VDD Under Voltage Lockout (UVLO)**

## APPLICATIONS

**Offline AC/DC Flyback Converter for**

- **AC/DC Adaptors**
- **Open-frame SMPS**
- **Set-Top Box Power Supplies**
- **ATX Standby Power**

## GENERAL DESCRIPTION

SF1538 is a high performance, low cost, highly integrated current mode PWM power switch for offline flyback converter applications.

In SF1538, PWM switching frequency with shuffling can be externally programmable, which can ease system design greatly. When the output power demands decrease, the IC automatically decreases switching frequency for high power conversion efficiency. When the current set-point falls below a given value, e.g. the output power demand diminishes, the IC enters into burst mode and provides excellent efficiency without audio noise.

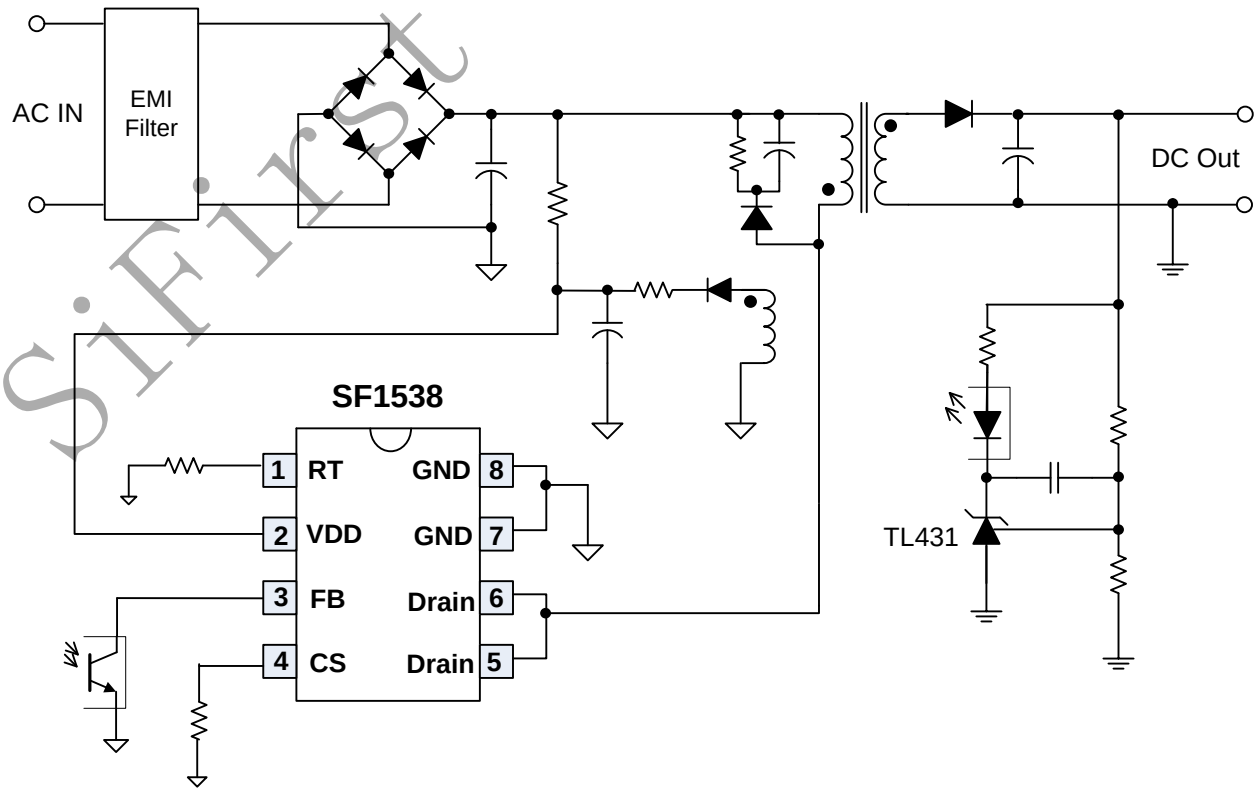
The IC can achieve "***Zero OCP/OPP Recovery Gap***" using SiFirst's proprietary control algorithm. Meanwhile, the OCP/OPP variation versus universal line input is compensated.

The IC has built-in synchronized slope compensation to prevent sub-harmonic oscillation at high PWM duty output. The IC also has built-in soft start function to soften the stress on the MOSFET during power on period.

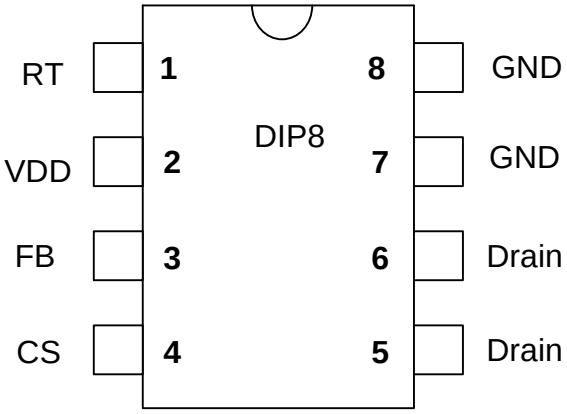
SF1538 integrates functions and protections of Under Voltage Lockout (UVLO), VCC Over Voltage Protection (OVP), Cycle-by-cycle Current Limiting (OCP), All Pins Floating Protection, Over Load Protection (OLP), RT Pin Short-to-GND Protection, VCC Clamping, Leading Edge Blanking (LEB).

SF1538 is available in DIP8 packages.

## TYPICAL APPLICATION



## Pin Configuration




## Ordering Information

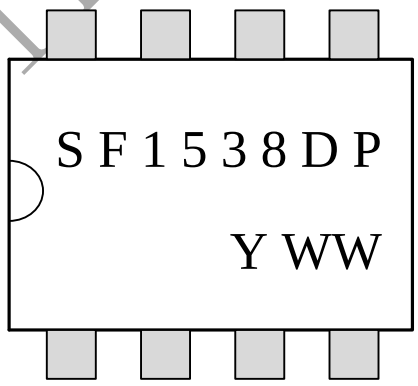
| Part Number | Top Mark | Package | | Tape & Reel |
|---|---|---|---|---|
| SF1538DP | SF1538DP | DIP8 | RoHs | |

## Output Power Table[1]

| Part Number | 230VAC ± 15%[2] | | 85-265VAC | |
|---|---|---|---|---|
| | Adapter[3] | Open Frame[4] | Adapter[3] | Open Frame[4] |
| **SF1538DP** | 18W | 26W | 15W | 18W |

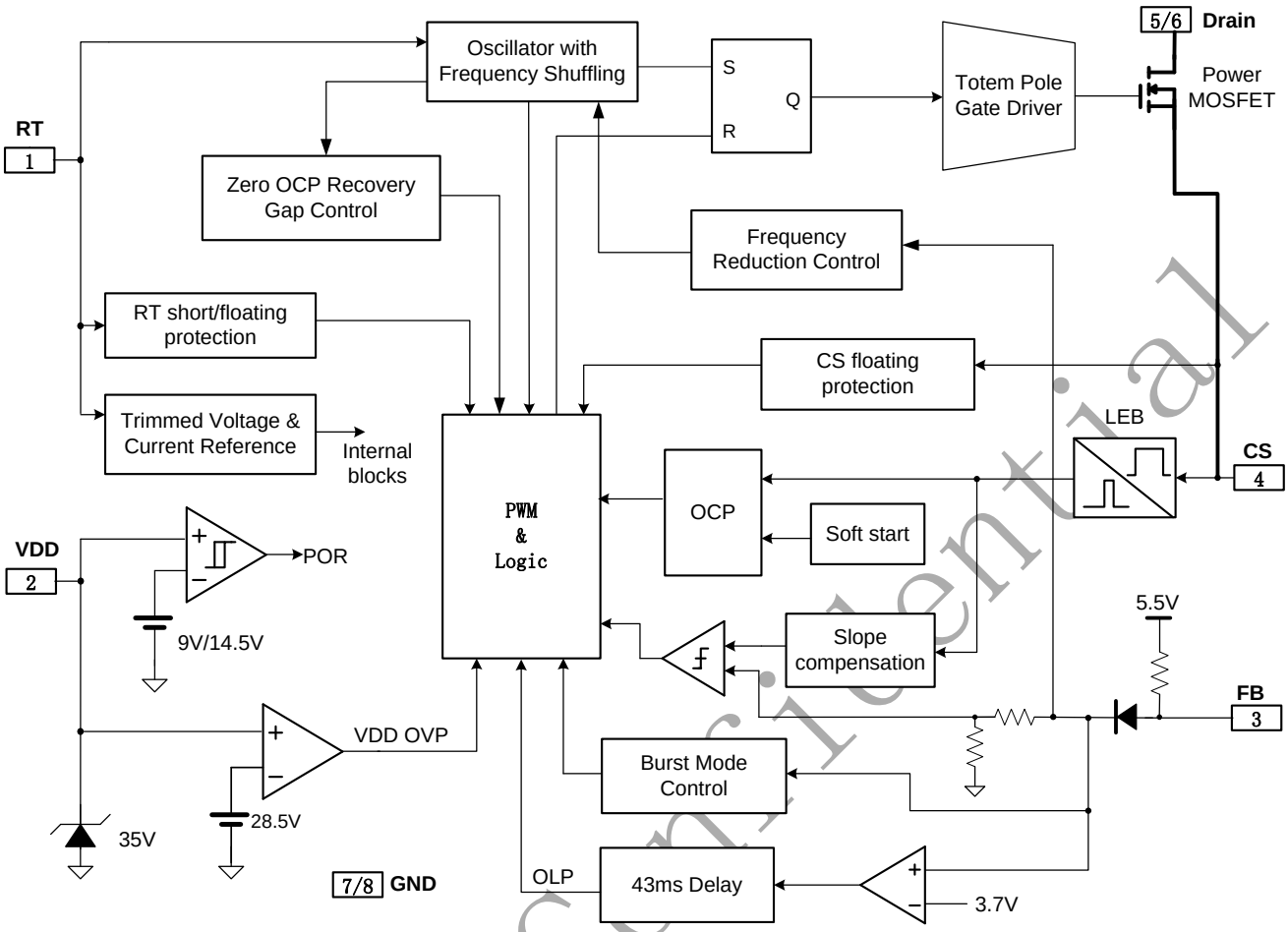
**Note 1.** The Max. output power is limited by junction temperature
**Note 2.** 230VAC or 100/115VAC with doublers
**Note 3.** Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50 °C ambient.
**Note 4.** Max. practical continuous power in a open-frame design with sufficient drain pattern as a heat sink at 50 °C ambient.

## Marking Information




YWW: Year&Week code

## Block Diagram




## Pin Description

| Pin Num | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | RT | I | Set the switching frequency by connecting a resistor between RT and GND. This pin has floating/short-to-GND protection. |
| 2 | VDD | P | IC power supply pin. |
| 3 | FB | I | Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 4. |
| 4 | CS | I | Current sense input pin. |
| 5-6 | Drain | P | High voltage power MOSFET drain connection. |
| 7-8 | GND | P | Ground. |

## Absolute Maximum Ratings (Note 5)

| Parameter | Value | Unit |
|---|---|---|
| VDD DC Supply Voltage | 35 | V |
| VCC DC Clamp Current | 10 | mA |
| Drain pin | -0.3 to 600 | V |
| FB, RT, CS voltage range | -0.3 to 7 | V |
| Package Thermal Resistance (DIP-8) | 84 | °C/W |
| Maximum Junction Temperature | 150 | °C |
| Operating Temperature Range | -40 to 85 | °C |
| Storage Temperature Range | -65 to 150 | °C |
| Lead Temperature (Soldering, 10sec.) | 260 | °C |
| ESD Capability, HBM (Human Body Model) | 3 | kV |
| ESD Capability, MM (Machine Model) | 250 | V |

## Recommended Operation Conditions (Note 6)

| Parameter | Value | Unit |
|---|---|---|
| Supply Voltage, VDD | 11 to 25 | V |
| Operating Frequency | 50 to 130 | kHz |
| Operating Ambient Temperature | -40 to 85 | $^{o}$C |

## ELECTRICAL CHARACTERISTICS

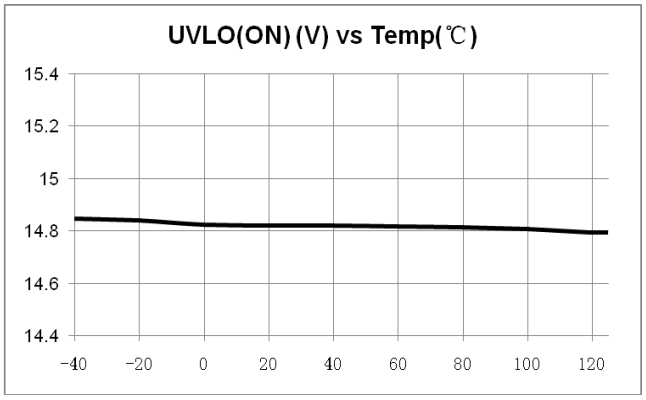
($T_A$ = 25$^{O}$C, RT=100K ohm, VDD=18V, if not otherwise noted)

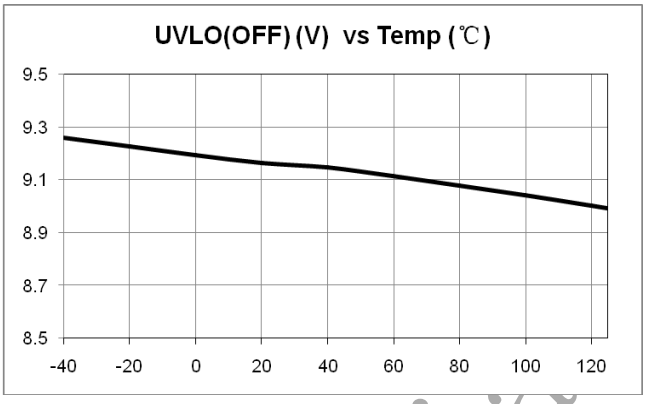
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage Section (VDD Pin)** | | | | | | |
| UVLO(ON) | VDD Under Voltage Lockout Exit (Startup) | | 13.5 | 14.5 | 15.5 | V |
| UVLO(OFF) | VDD Under Voltage Lockout Enter | | 8 | 9 | 9.8 | V |
| I_Startup | VDD Start up Current | VDD =12.5V, Measure current into VDD | | 5 | 20 | uA |
| I_VDD_Op | Operation Current | $V_{FB}$=3V | | 2.0 | 3.5 | mA |
| VDD_OVP | VDD Over Voltage Protection trigger | | | 28.5 | | V |
| $V_{DD}$_Clamp | VDD Zener Clamp Voltage | I($V_{DD}$) = 15 mA | | 35 | | V |
| T_Softstart | Soft Start Time | | | 3 | | mSec |
| **Feedback Input Section(FB Pin)** | | | | | | |
| $V_{FB}$_Open | FB Open Voltage | | | 5.5 | | V |
| $I_{FB}$_Short | FB short circuit current | Short FB pin to GND, measure current | | 1.05 | | mA |
| $A_{VCS}$ | PWM Input Gain | $\Delta V_{FB}/\Delta V_{cs}$ | | 2.0 | | V/V |
| VFB_min_duty | FB under voltage gate clock is off. | | | 1.0 | | V |
| $V_{TH}$_PL | Power Limiting FB Threshold Voltage | | | 3.6 | | V |
| $T_D$_PL | Power limiting Debounce Time | Note 7 | | 42 | | mSec |
| $Z_{FB}$_IN | Input Impedance | | | 5 | | Kohm |
| **Current Sense Input Section (CS Pin)** | | | | | | |
| Vth_OC_min | Internal current limiting threshold | Zero duty cycle | 0.70 | 0.75 | 0.80 | V |
| T_blanking | SENSE Input Leading Edge Blanking Time | | | 250 | | nSec |
| $T_D$_OC | Over Current Detection and Control Delay | | | 90 | | nSec |
| **Oscillator Section (RT Pin)** | | | | | | |
| $F_{OSC}$ | Normal Oscillation Frequency | | 60 | 65 | 70 | KHZ |
| RT_range | Operating RT Range | | 50 | 100 | 150 | Kohm |
| V_RT_open | RT open voltage | | | 2.0 | | V |
| ΔF(shuffle)/Fosc | Frequency shuffling range | Note 8 | -4 | | 4 | % |
| Δf_Temp | Frequency Temperature Stability | -20$^{o}$C to 100 $^{o}$C (Note 7) | | 5 | | % |
| Δf_VDD | Frequency Voltage Stability | VDD = 12-25V, | | 5 | | % |
| Duty_max | Maximum Duty cycle | | 75 | 80 | 85 | % |
| F_BM | Burst Mode Base Frequency | | | 22 | | KHZ |
| **Power MOSFET Section**[8] | | | | | | |

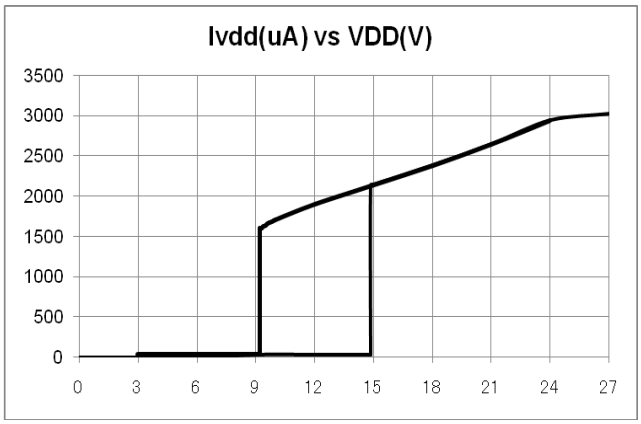
| | | | | | | |
|---|---|---|---|---|---|---|
| BVdss | Power MOSFET Drain Source Breakdown Voltage | | 600 | | | V |
| Rdson | Static Drain-Source On Resistance | I(Drain)=1A | | 4 | 5 | Ω |
| Idss | Zero Gate Voltage Drain Current | | | | 1 | uA |
| $Td_{(on)}$ | Turn-on delay time | | | 9 | | ns |
| $Td_{(off)}$ | Turn-off delay time | | | 24 | | ns |

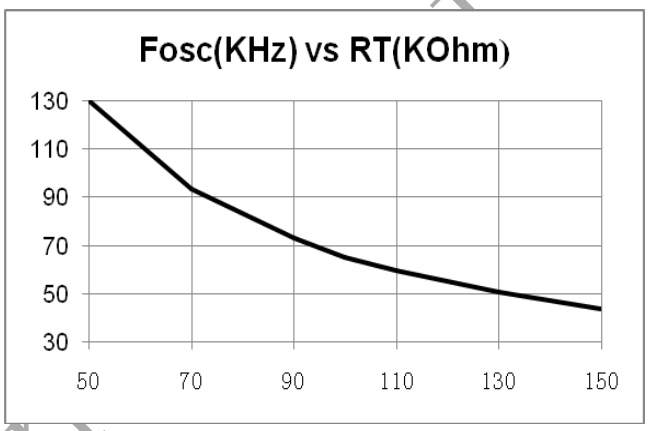
**Note 5.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
**Note 6.** The device is not guaranteed to function outside its operating conditions.
**Note 7.** Guaranteed by design.
**Note 8.** These parameters, although guaranteed, are not 100% tested in production

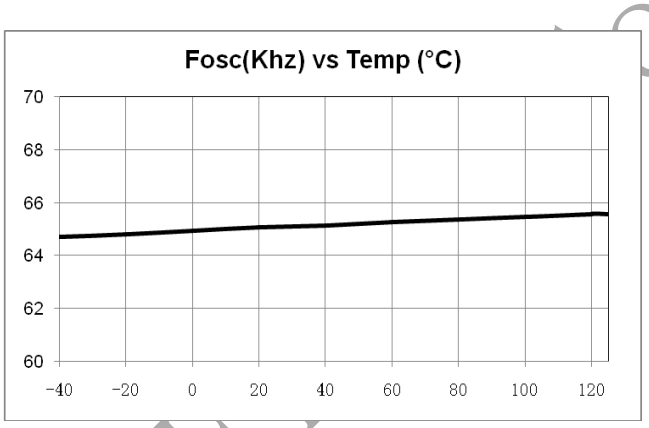
## CHARACTERIZATION PLOTS

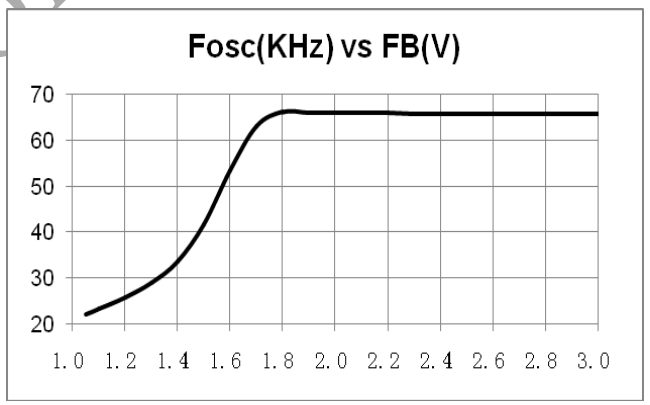


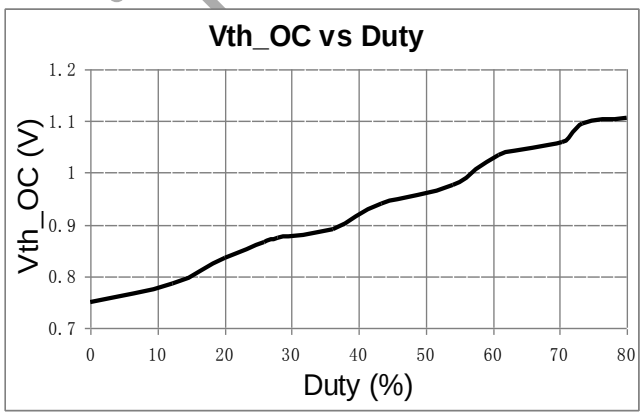



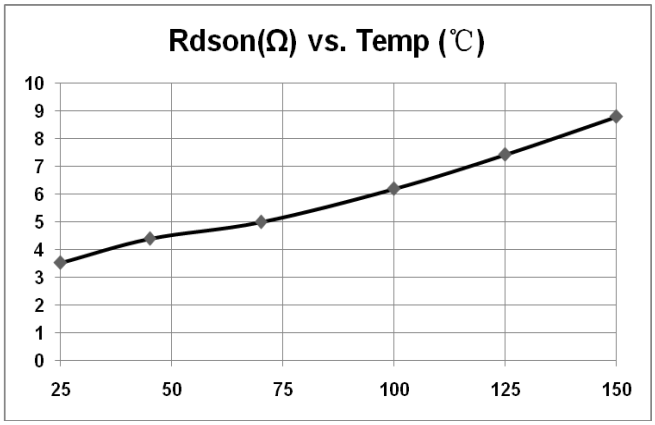



## OPERATION DESCRIPTION

SF1538 is a high performance, low cost, highly integrated current mode PWM power switch for offline flyback converter applications. The built-in advanced energy saving with high level protection features improves the SMPS reliability and performance without increasing the system cost.

### ◆ UVLO and Startup Operation

Fig.1 shows a typical startup circuitn. Before the IC begins switching operation, it consumes only startup current (typically 5uA) and current supplied through the startup resistor Rst charges the VDD hold-up capacitor Cdd. When VDD reaches UVLO turn-on voltage of 14.5V(typical), SF1538 begins switching and the IC current consumed increased to 2mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 9V). The selection of Rst and Cdd should be a trade off between the power loss and startup time.

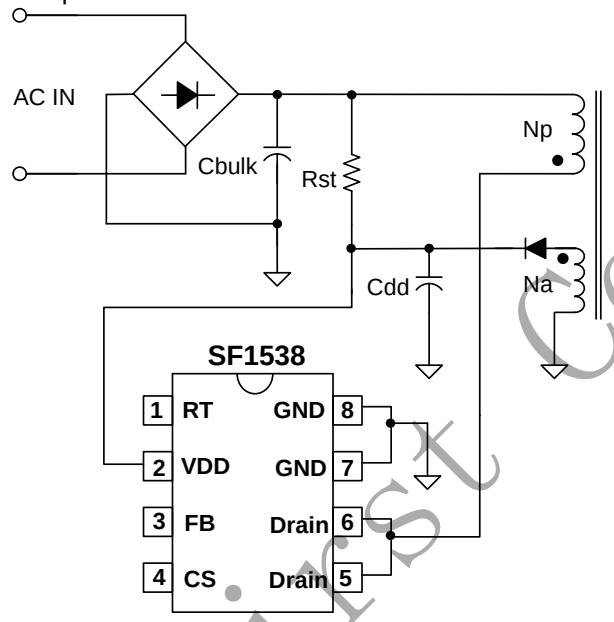



Fig.1

### ◆ Low Operating Current

The operating current in SF1538 is as small as 1.3mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

### ◆ Soft Start

SF1538 features an internal 3ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

### ◆ "Zero OCP/OPP Recovery Gap" Control

The definition of OCP or OPP recovery gap of a power adaptor is illustrated in Fig.2. At T0, assuming an adaptor is at full loading mode. If the loading keeps increasing, then the system will output maximum power P_opp, which will trigger OPP protection at the same time. After the OPP protection is triggered, usually the system will enter into the auto-recovery mode, in burst manner. If the system power demand decreases below P_recovery, then system will enter into normal mode again, as shown in Fig.2. The difference between P_opp and P_recovery is defined as "***OPP Recovery Gap***", which can cause system startup failure especially in 90VAC full load startup.

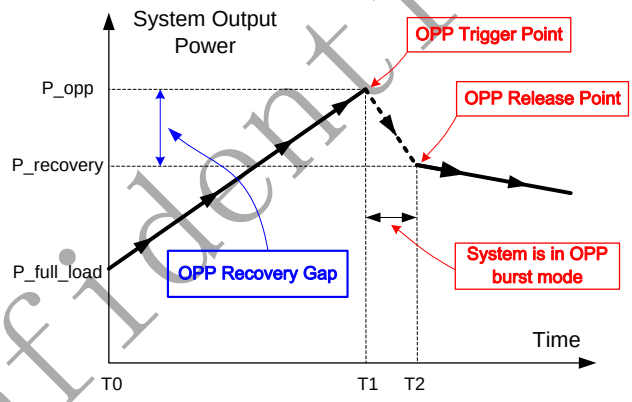



Fig.2

SF1538 can achieve "***Zero OCP/OPP Recovery Gap***" in the whole universal AC input range using SiFirst's proprietary control algorithm.

### ◆ Programmable Switching Frequency

Connecting a resistor from RT pin to GND according to the equation below to program the normal switching frequency:

$$F_{OSC}(KHz) = \frac{6500}{RT(K\Omega)}$$

It can typically operate between 50kHz to 130kHz. To improve system EMI performance, SF1538 operates the system with ±4% frequency shuffling around setting frequency.

### ◆ Synchronous Slope Compensation

InSF1538, the synchronous slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

### ◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse,

an internal leading edge blanking circuit is built in. During this blanking period (350ns, typical), the PWM comparator is disabled and cannot switch off the gate driver. Thus, external RC filter with a small time constant is enough for current sensing.

### ◆ Frequency Reduction for Green Mode Operation

When the loading is light, the IC will automatically reduce the PWM switching frequency to achieve high efficiency. In the whole frequency reduction process, there is no audio noise generated.

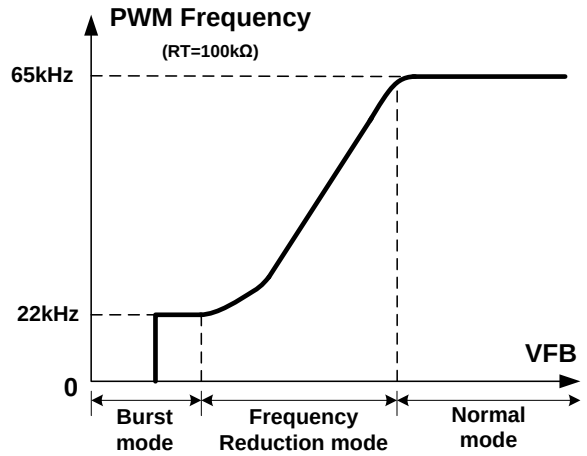



Fig.3

### ◆ Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below Vskip, SF1538 will stop switching and output voltage starts to drop, which causes the VFB to rise. Once VFB rises above Vskip, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

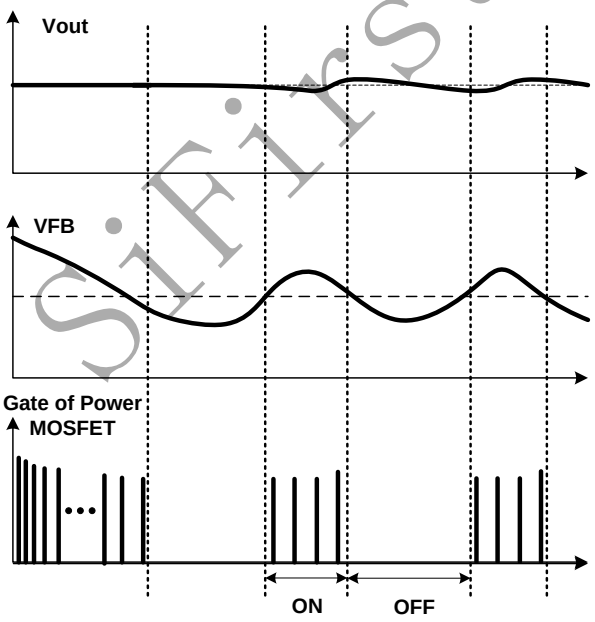



Fig.4

### ◆ Auto Recovery Mode Protection

As shown in Fig.5, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to UVLO(off) (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.4. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

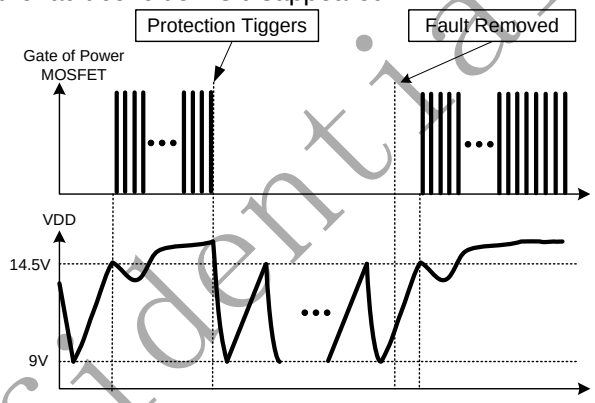



Fig.5

### ◆ VDD OVP(Over Voltage Protection)

VDD OVP (Over Voltage Protection) is implemented in SF1538 and it is a protection of auto-recovery mode.

### ◆ Over Load Protection (OLP)

When over load occurs, a fault is detected. If this fault is present for more than 43ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above. The 43mS delay time is to prevent the false trigger from the power-on and turn-off transient

### ◆ All Pins Floating Protection and RT Pin Short-to-GND Protection

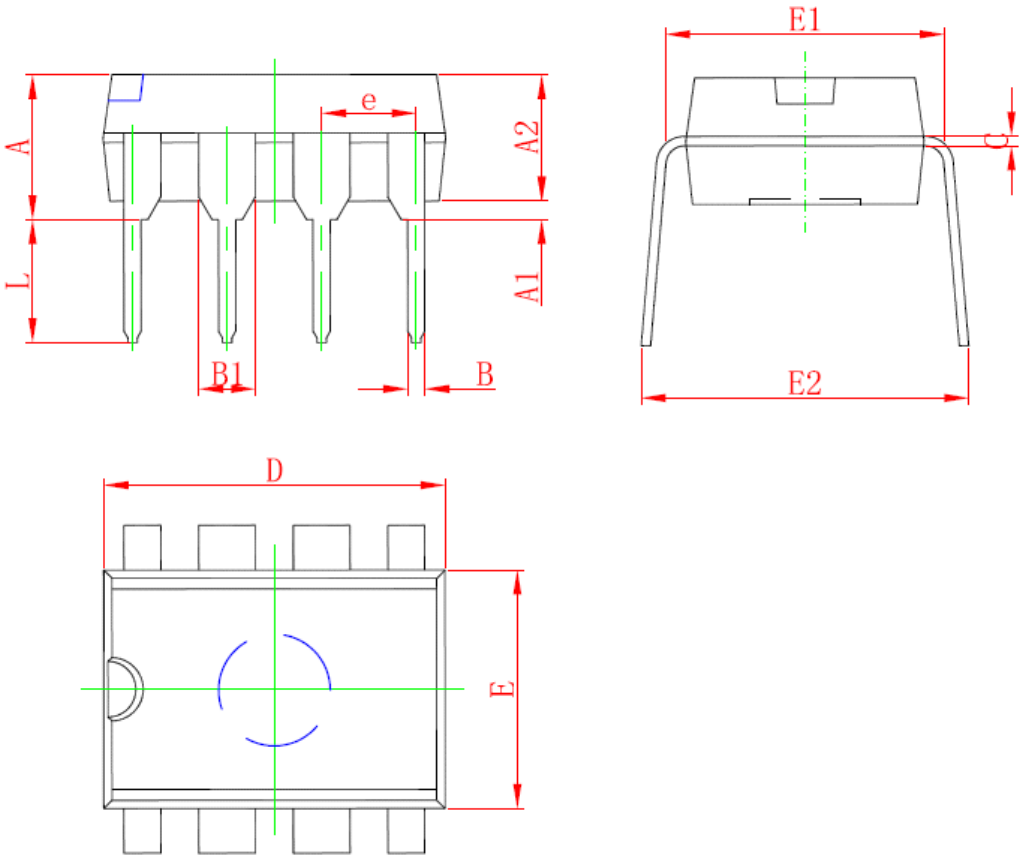
In SF1538, if pin floating situation or RT pin short-to-GND occurs, the protection is triggered immediately and the system will experience the process of auto-recovery mode protection.

### ◆ Soft Gate Drive

The driving stage of SF1538 is a soft totem-pole gate driver to minimize EMI. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability.

## PACKAGE MECHANICAL DATA

### DIP8 PACKAGE OUTLINE DIMENSIONS




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 3.710 | 5.334 | 0.146 | 0.210 |
| A1 | 0.381 | | 0.015 | |
| A2 | 3.175 | 3.600 | 0.125 | 0.142 |
| B | 0.350 | 0.650 | 0.014 | 0.026 |
| B1 | 1.524 (BSC) | | 0.06 (BSC) | |
| C | 0.200 | 0.360 | 0.008 | 0.014 |
| D | 9.000 | 10.160 | 0.354 | 0.400 |
| E | 6.200 | 6.600 | 0.244 | 0.260 |
| E1 | 7.320 | 7.920 | 0.288 | 0.312 |
| e | 2.540 (BSC) | | 0.1 (BSC) | |
| L | 2.921 | 3.810 | 0.115 | 0.150 |
| E2 | 8.200 | 9.525 | 0.323 | 0.375 |

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