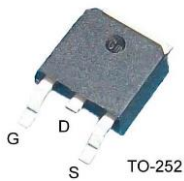
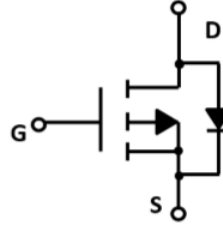


<p><b>Features</b></p> <ul style="list-style-type: none"> <li>• -60V, -13A</li> <li>• <math>R_{DS(ON)} = 90m\Omega</math> (Max.) @ <math>V_{GS} = -10V, I_D = -10A</math></li> <li>• Green Device Available</li> <li>• Super Low Gate Charge</li> <li>• Excellent CdV/dt effect decline</li> <li>• Advanced high cell density Trench technology</li> </ul>	<p><b>Application</b></p> <ul style="list-style-type: none"> <li>• Power switching application</li> <li>• Hard switched and high frequency circuits</li> <li>• Uninterruptible Power Supply</li> </ul>
<p><b>Package</b></p> <div style="display: flex; justify-content: space-around; align-items: center;">   </div> <p style="text-align: center;"><b>SFD6113AT</b></p>	

**Absolute Maximum Ratings**  $T_C=25^\circ C$  unless otherwise specified

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	-60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current <sup>note1</sup>	$T_C = 25^\circ C$	-13 A
		$T_C = 100^\circ C$	-8.3 A
$I_{DM}$	Pulsed Drain Current <sup>note2</sup>	-26	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note3</sup>	29.8	mJ
$P_D$	Power Dissipation <sup>note4</sup>	$T_C = 25^\circ C$ 31.1	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ C$

\*Drain current limited by maximum junction temperature

**Electrical Characteristics**  $T_C=25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-60	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -48V, V_{GS} = 0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-	-2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance <sup>note2</sup>	$V_{GS} = -10V, I_D = -10A$	-	-	90	m $\Omega$
		$V_{GS} = -4.5V, I_D = -5A$	-	-	132	
$g_{FS}$	Forward Transconductance	$V_{DS} = -10V, I_D = -5A$	-	8.7	-	S
$R_g$	Gate Resistance	$V_{DS} = V_{GS}=0V, f = 1.0MHz$	-	15	-	$\Omega$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1.0MHz$	-	1080	-	pF
$C_{oss}$	Output Capacitance		-	73	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	50	-	pF
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS} = -12V, I_D = -6A,$ $V_{GS} = -4.5V$	-	11.8	-	nC
$Q_{gs}$	Gate-Source Charge		-	1.9	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	6.5	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15V, I_D = -1A$ $R_G = 3.3\Omega, V_{GS} = -10V$	-	8.8	-	ns
$t_r$	Turn-On Rise Time		-	19.6	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	47.2	-	ns
$t_f$	Turn-Off Fall Time		-	9.6	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current <sup>note1,5</sup>		-	-	-13	A
$I_{SM}$	Pulsed Source Current <sup>note2,5</sup>		-	-	-26	A
$V_{SD}$	Drain to Source Diode Forward Voltage <sup>note2</sup>	$V_{GS} = 0V, I_S = -1A$	-	-	-1	V

Notes:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is  $V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-24.4A$
4. The power dissipation is limited by 150 $^{\circ}\text{C}$  junction temperature
5. The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation

### Typical Performance Characteristics

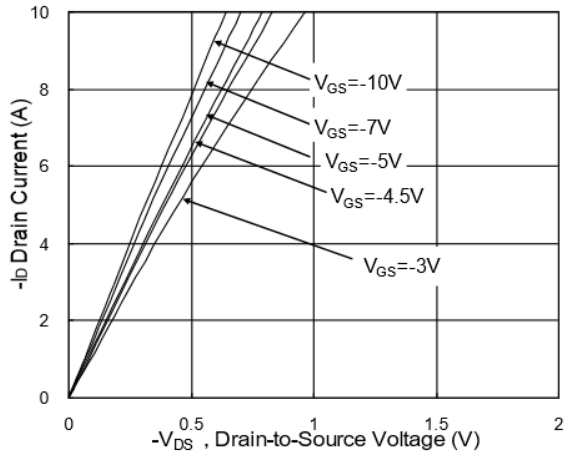


Figure 1. Output Characteristics

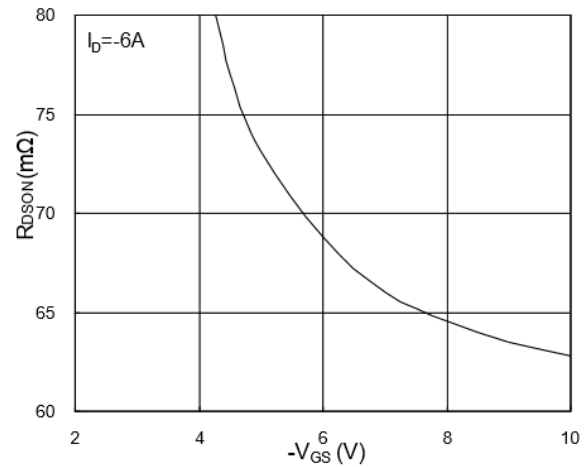


Figure 2. On-Resistance v.s Gate-Source

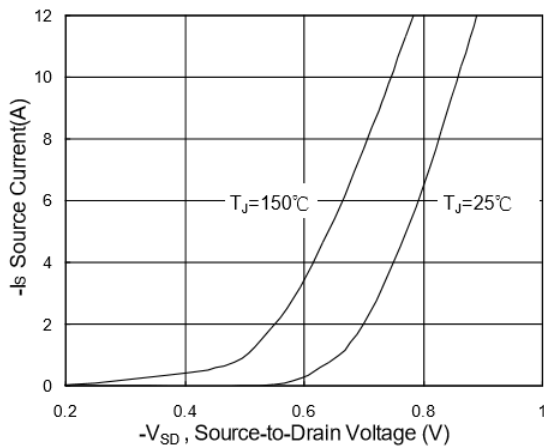


Figure 3. Forward Characteristics of Reverse

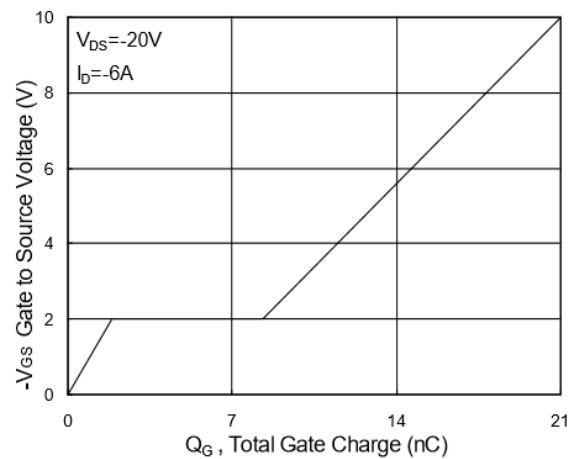


Figure 4. Gate-Charge Characteristics

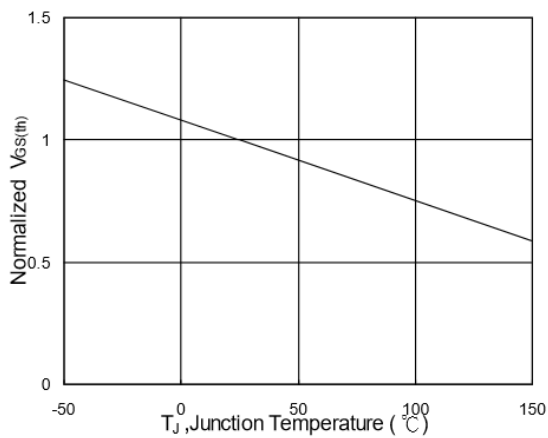


Figure 5. Normalized  $V_{GS(th)}$  v.s  $T_J$

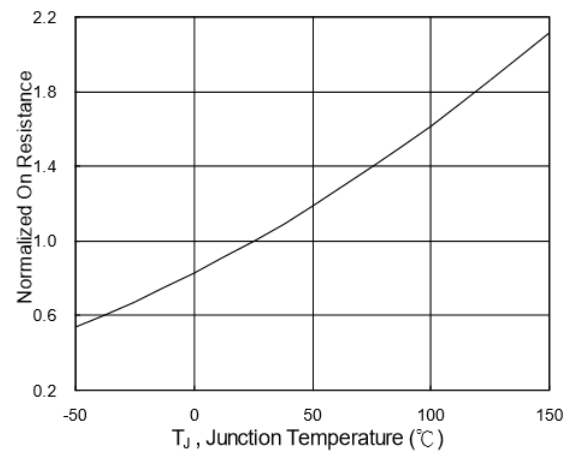


Figure 6. Normalized  $R_{DS(on)}$  v.s  $T_J$

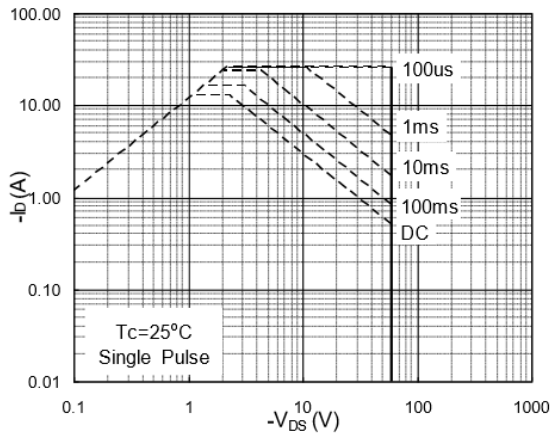


Figure 7. Maximum Safe Operating Area

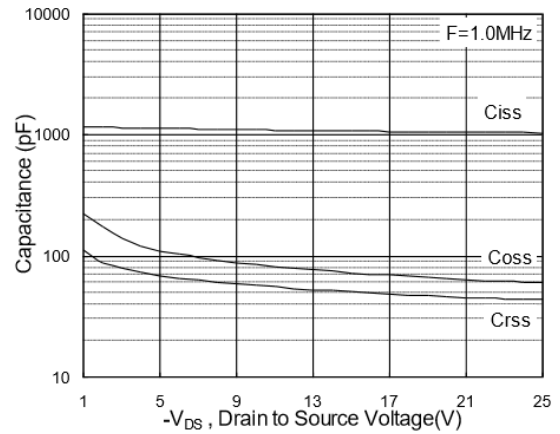


Figure 8. Typical Capacitance Characteristics

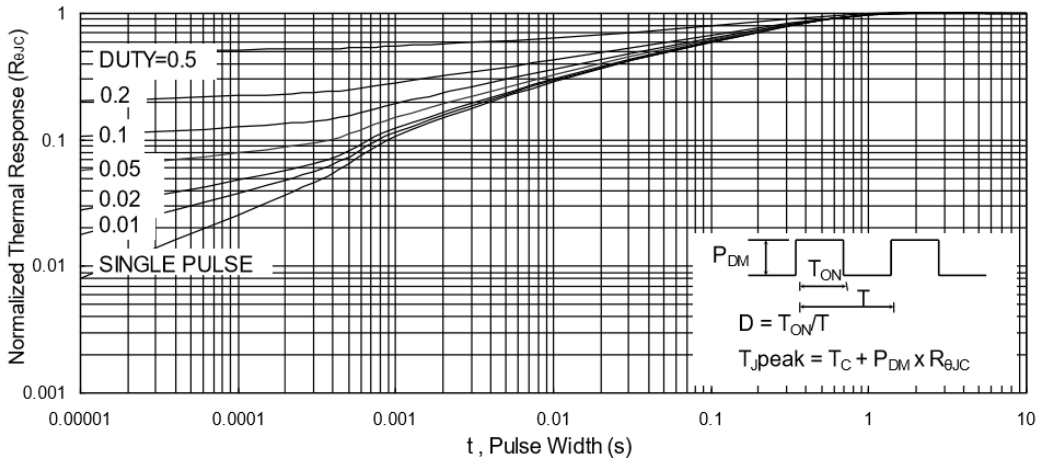


Figure 9 Effective Transient Thermal Impedance

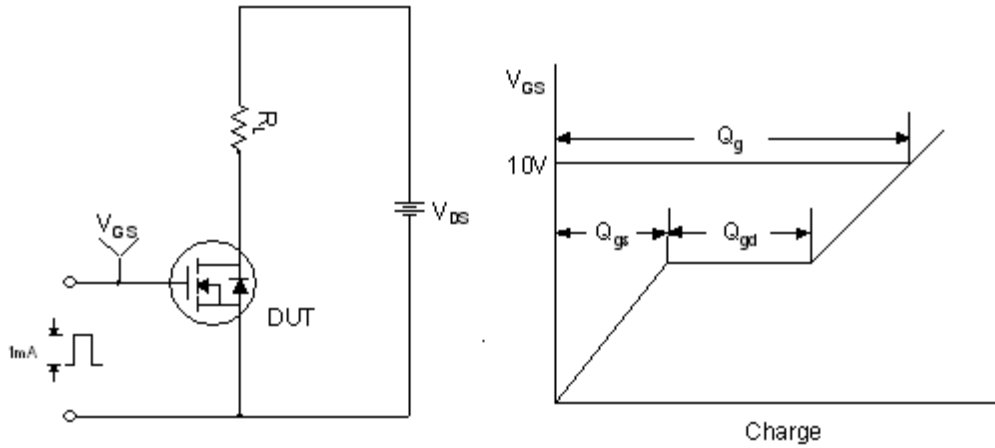


Figure 10. Gate Charge Test Circuit & Waveform

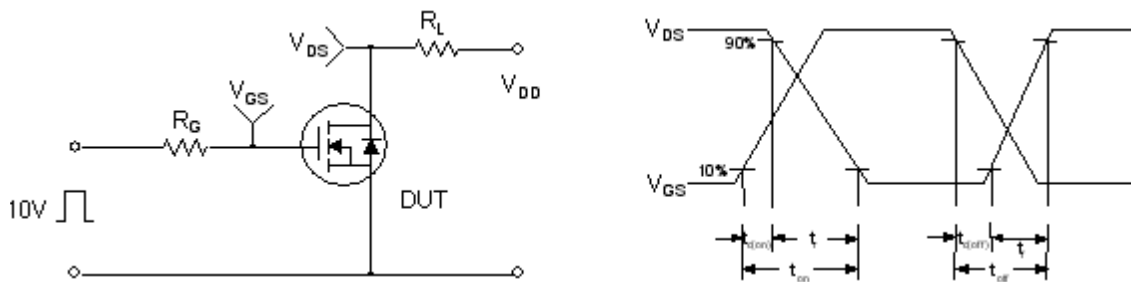


Figure 11. Resistive Switching Test Circuit & Waveforms

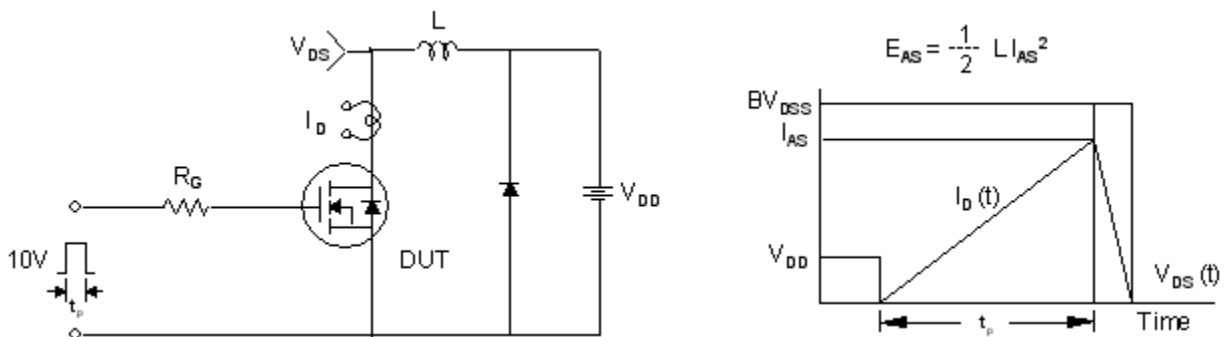


Figure 12. Unclamped Inductive Switching Test Circuit & Waveforms

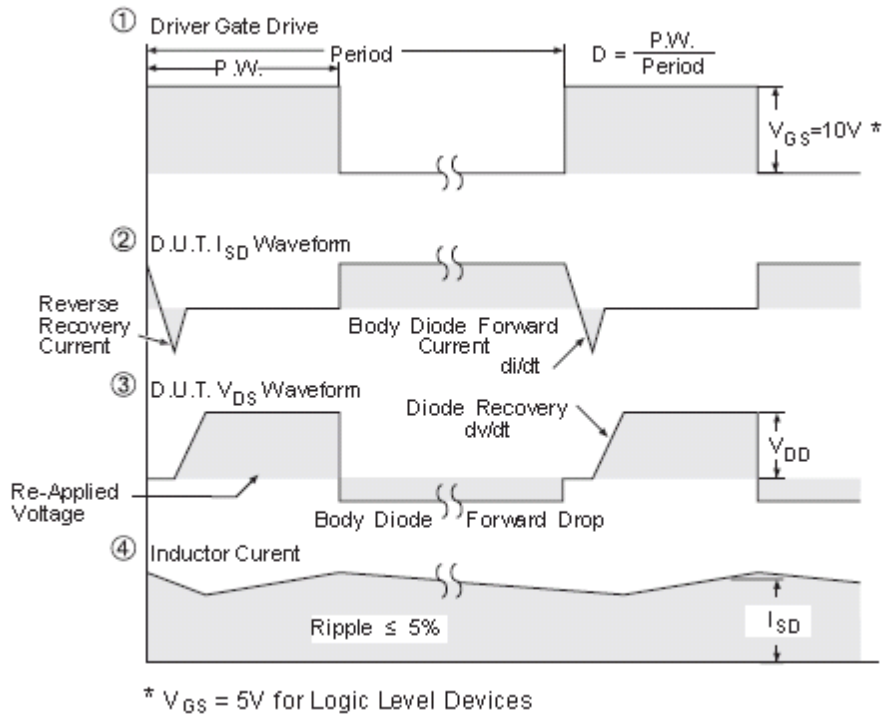
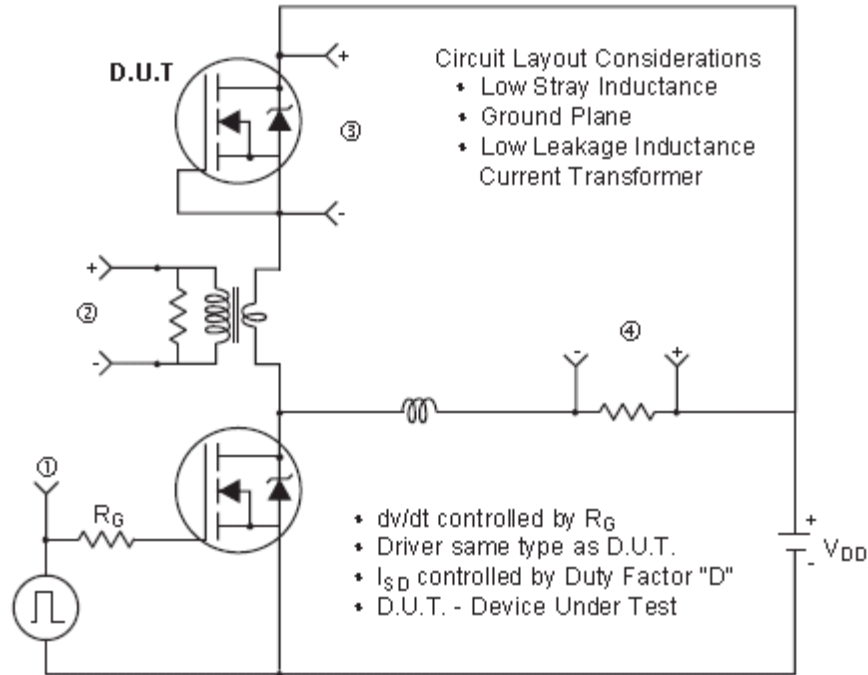
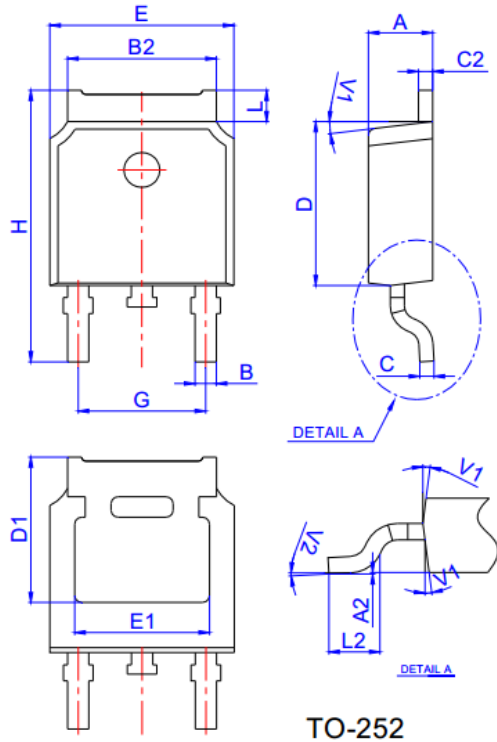


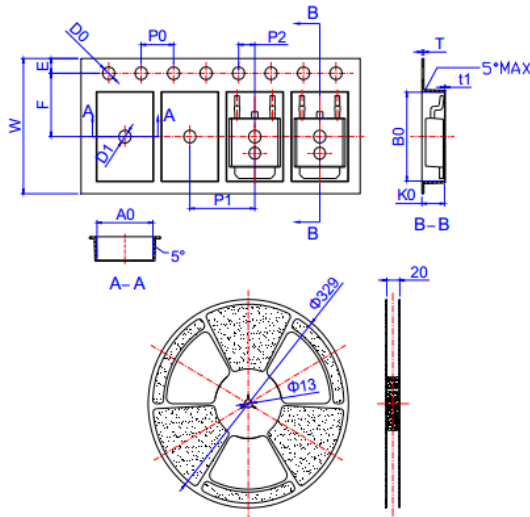
Figure 13. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms (For N-channel)

**Package Mechanical Data**



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

**Reel Specification-TO-252**



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

OUTLINE	REEL (PCS)	PER CARTON (PCS)	TAPE & REEL
TAPING	2,500	25,000	13inch

## SFD6113AT Product Description

Silicon P-Channel MOSFET



### NOTE:

1. We strongly recommend customers check carefully on the trademark when buying our product, if there is any question, please don't be hesitate to contact us.
2. Please do not exceed the absolute maximum ratings of the device when circuit designing.
3. Winsemi Microelectronics Co., Ltd reserved the right to make changes in this specification sheet and is subject to change without prior notice.

### CONTACT:

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